MP5424

5V PMIC with Four 4.5A/2.5A/4.5A/2A Buck Converters, 3 LDOs, 1 Load Switch, and Flexible System Settings via I²C and MTP

DESCRIPTION

The MP5424 is a complete power management solution that integrates four high-efficiency step-down DC/DC converters, three low-dropout (LDO) regulators, one load switch, and a flexible logic interface.

Constant-on-time (COT) control in the DC/DC converter provides fast transient response. The 1.1MHz default switching frequency (f_{SW}) during continuous conduction mode (CCM) greatly reduces the external inductance and capacitance. Full protection features include under-voltage lockout (UVLO) protection, over-current protection (OCP), over-voltage protection (OVP), and thermal shutdown.

The output voltage (V_{OUT}) can be adjusted via the I²C bus or preset by the multiple-time programmable (MTP) interface. The start-up/shutdown sequence can also be configured via the MTP and controlled via the I²C bus.

The MP5424 requires a minimal number of external components, and is available in a small QFN-26 (3.5mmx4.5mm) package.

FEATURES

- **High-Efficiency Step-Down Converters:**
  - Buck 1: 4.5A DC/DC Converter
  - Buck 2: 2.5A DC/DC Converter
  - Buck 3: 4.5A DC/DC Converter
  - Buck 4: 2A DC/DC Converter
  - Buck 1 and Buck 3 Can Work in Parallel
  - Buck 2 and Buck 4 Can Work in Parallel
  - 2.7V to 5.5V Operating V_{IN} Range
  - Buck 1, Buck 2, and Buck 3 Selectable V_{OUT} Range: 0.4V to 2.2V/7.4mV Step or 0.4V to 3.58V V_{OUT}/12.5mV Step
  - Buck 4 V_{OUT} Range: 0.4V to 3.58V V_{OUT}/12.5mV Step
  - Adjustable Switching Frequency (f_{SW})
  - Adjustable Soft-Start Time (t_{SS})
  - Adjustable Phase Delay
  - Configurable Forced PWM (FPWM) Mode or Auto-PFM/PWM Mode
  - Output OCP and OVP
- **Low-Dropout (LDO) Regulators:**
  - Three 300mA, Low-Noise LDOs
  - Two Separate Input Power Supplies
  - 50mV Dropout at 300mA Load
- **Load Switch:**
  - 2.7V to 5.5V/3A Load Switch
  - 50mΩ On Resistance at V_{IN} = 5V
  - On/Off Control via the I²C and Programmable Sequence
  - Configurable Output Discharge Function via the I²C (Default: On)
- **System:**
  - I²C Bus and User-Programmable MTP
  - Two-Time Programmable MTP (1)
  - Start-Up/Shutdown Control
  - Enable Pin (EN1) for Sleep Mode Entry and Recovery Control
  - Start-Up Reset Output
  - Flexible Start-Up/Shutdown Sequence via MTP (0.5ms, 2ms, 8ms, or 16ms Selectable Time Slot)
  - Available in a QFN-26 (3.5mmx4.5mm) Package

MPL Optimized Performance with MPS Inductor MPL-AL6050 Series

Note:

1) The two-time programmable MTP is only for the standard version of the MP5424GRM-0000.

APPLICATIONS

- General Consumer
- Camera Modules
- 3.3V/5V Powered Systems
- Space-Limited Systems

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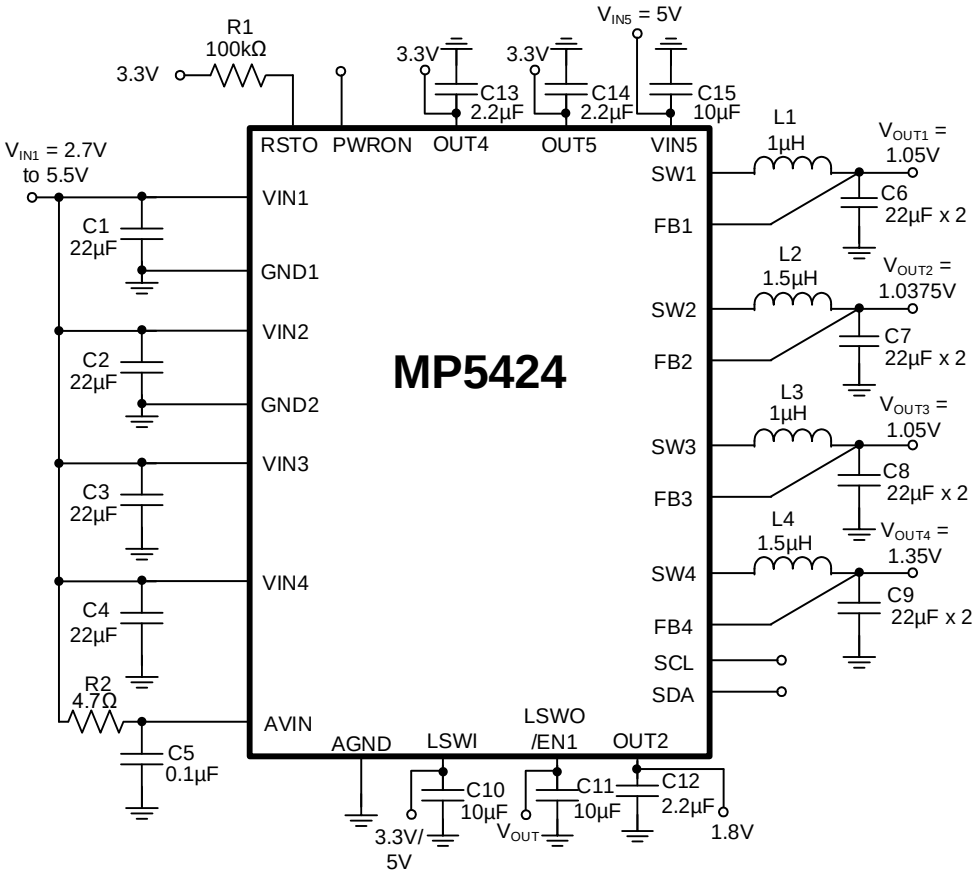
TYPICAL APPLICATION



MTP-EFUSE SELECTED TABLE BY DEFAULT (MP5424GRM-0000)

MTP Items	Buck 1	Buck 2	Buck 3	Buck 4	LSWO (2)	LDO 2	LDO 4	LDO 5
Output voltage	1.05V	1.0375V	1.05V	1.35V	3.3V/5V	1.8V	3.3V	3.3V
Initial on/off	On	On	On	On	On	On	On	On
Mode	FPWM	FPWM	FPWM	FPWM	N/A			
Start-up delay	1.5ms	1ms	1.5ms	0.5ms	2ms	0ms	5ms	5.5ms
Soft-start time (t_{SS})	300µs	300µs	300µs	300µs	N/A			
Switching frequency (f_{SW})	1.1MHz							
PWRON MODE	0 (level trigger)							
RSTODELAY	50ms							
Buck 1 peak current limit	7.6A							
Buck 2 peak current limit	3.9A							
Buck 3 peak current limit	7.6A							
Buck 4 peak current limit	3.9A							
I²C slave address	0x69							
MTP configuration code	0000							

Note:

2) The load switch supply is on the LSWI pin. The supply voltage range is between 2.7V and 5.5V.

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL
MP5424GRM-xxxx**	QFN-26 (3.5mmx4.5mm)	*See Below*	1
MP5424GRM-0000	QFN-26 (3.5mmx4.5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP5424GRM-0000-Z, MP5424GRM-xxxx-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the MTP.

The default number is “0000”. Each “x” can be a hexadecimal value between 0 and F. Contact an MPS FAE to create this unique number.

TOP MARKING

MPSYW

M5424

LLLLL

MPS: MPS prefix
Y: Year code
W: Week code
M5424: Part number
LLLLL: Lot number

EVALUATION KIT EVKT-MP5424

EVKT-MP5424 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV5424-R-00A	MP5424GRM evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I²C communication interface device, one USB cable, and one ribbon cable	1
3	MP5424-0000	MP5424 IC which can be used for MTP programming	2

Order direct from MonolithicPower.com or our distributors.

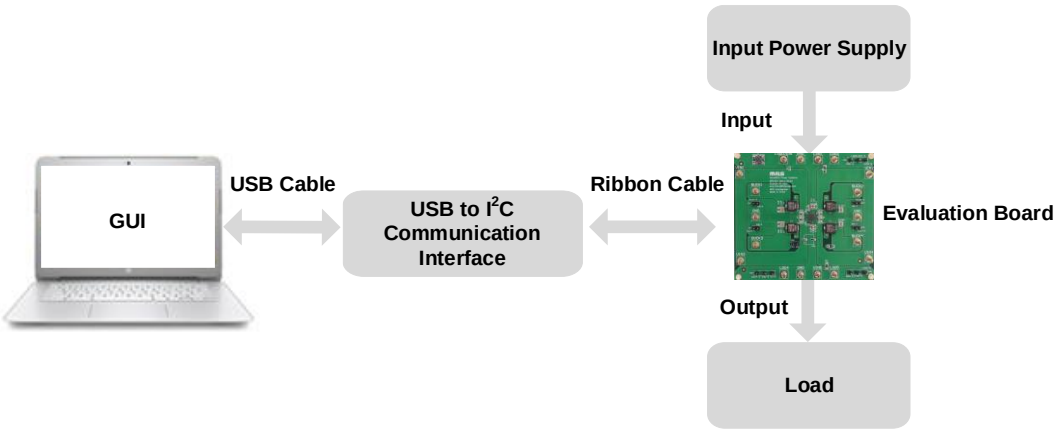

Figure 1: EVKT-MP5424 Evaluation Kit Set-Up

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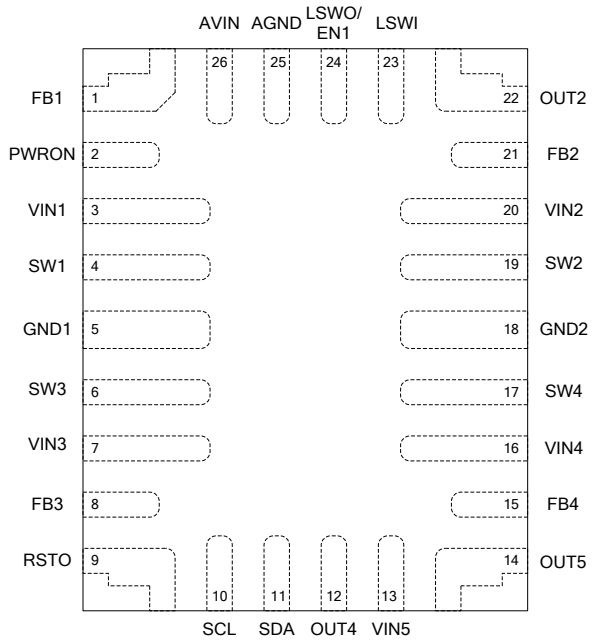
PACKAGE REFERENCE

TOP VIEW



QFN-26 (3.5mmx4.5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	FB1	**Buck 1 feedback**. Connect buck 1's output directly to the FB1 pin.
2	PWRON	**Start-up/shutdown input.** The PWRON pin is a logic input pin that can start up or shut down the device. PWRON has a weak internal pull-up current.
3	VIN1	**Buck 1 supply voltage input.** The MP5424 operates from a 2.7V to 5.5V input rail. Use a ceramic decoupling capacitor to decouple the input rail. Use a wide PCB trace for VIN1 path. VIN1, VIN2, VIN3, VIN4, and AVIN should be connected to the same bus voltage (V_{BUS}).
4	SW1	**Buck 1 switch output.** Use a wide PCB trace for SW1 path.
5	GND1	**Buck 1 and buck 3 power ground.** The GND1 pin requires special consideration during PCB layout. Connect GND1 to ground using copper traces and vias.
6	SW3	**Buck 3 switch output.** Use a wide PCB trace for SW3 path.
7	VIN3	**Buck 3 supply voltage input.** The MP5424 operates from a 2.7V to 5.5V input rail. Use a ceramic decoupling capacitor to decouple the input rail. Use a wide PCB trace for VIN3 path. VIN1, VIN2, VIN3, VIN4, and AVIN should be connected to the same V_{BUS}.
8	FB3	**Feedback of buck3**. Connect buck 3's output directly to the FB3 pin.
9	RSTO	**Reset output from the PMIC to CPU.** The RSTO pin is an open-drain output. RSTO requires an external pull-up resistor.
10	SCL	**I²C clock signal input.**
11	SDA	**I²C data pin.**
12	OUT4	**LDO4 output.** The LDO4 pin is powered by VIN5.
13	VIN5	**LDO4 and LDO5 power input pin.** This VIN5 pin operates from a 2.7V to 5.5V input voltage (V_{IN}). Connect the VIN5 and VIN1 pins if LDO4 and LDO5 are not used.
15	FB4	**Buck 4 feedback.** Connect buck 4's output directly to the FB4 pin.
16	VIN4	**Buck 4 supply voltage input.** The MP5424 operates from a 2.7V to 5.5V input rail. Use a ceramic decoupling capacitor to decouple the input rail. Use a wide PCB trace for VIN4 path. VIN1, VIN2, VIN3, VIN4, and AVIN should be connected to the same V_{BUS}.
17	SW4	**Buck 4 switch output.** Use a wide PCB trace for SW4 path
18	GND2	**Buck 2 and buck 4 power ground.** The GND2 pin requires special consideration during PCB layout. Connect GND2 to ground using copper traces and vias.
19	SW2	**Buck 2 switch output.** Use a wide PCB trace for SW2 path
20	VIN2	**Buck 2 supply voltage input.** The MP5424 operates from a 2.7V to 5.5V input rail. Use a ceramic decoupling capacitor to decouple the input rail. Use a wide PCB trace for VIN2 path. VIN1, VIN2, VIN3, VIN4, and AVIN must be connected to the same bus voltage.
21	FB2	**Buck 2 feedback.** Connect buck 2's output directly to the FB2 pin.
22	OUT2	**LDO 2 output.** LDO 2 is powered by VIN2. If the OUT2 pin is configured as EN1, then OUT2 acts as an input pin. Pull EN1 high to turn on the PMIC; pull EN1 low to turn it off.
23	LSWI	**Load switch input.**
24	LSWO/ EN1	**Load switch output or EN1.** If the LSWO/EN1 pin is configured as EN1, then LSWO/EN1 acts as an input pin.
25	AGND	**Analog ground.** Connect the AGND pin to the GND1 and GND2 pins.
26	AVIN	**Power supply input for logic circuitry.** Use a 0.1µF ceramic capacitor to bypass the AVIN pin to AGND. Connect AVIN to the system input via a 4.7Ω resistor. VIN1, VIN2, VIN3, VIN4, and AVIN should be connected to the same V_{BUS}.

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ABSOLUTE MAXIMUM RATINGS (3)

V_{IN1}, V_{IN2}, V_{IN3}, V_{IN4}, V_{IN5}, V_{AVIN} .....
.....-0.3V to +6.5V (6.8V for 300ms)
V_{SWx} .....
-0.6V (-5V for <10ns) to V_{INx} + 0.3V (7V for <10ns)
All other pins..... -0.3V to +6.25V
Continuous power dissipation (T_A = 25°C) (4) (8)
QFN-26 (3.5mmx4.5mm) 6.25W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings (5) (6)

Human body model (HBM) .....± 2kV
Charged device model (CDM).....± 750V

Recommended Operating Conditions (7)

Step-down converter (V_{INx})..... 2.7V to 5.5V
Step-down converter (V_{OUTx}).....
.....0.4V to 3.58V or V_{INx}
LDO regulator output (V_{LDOx}).....
.....0.65V to 3.58V or V_{INx}
Load switch output (V_{OUT_LSW}) ..... 2.7V to 5.5V
Operating junction temp (T_J) ....-40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-26 (3.5mmx4.5mm)			
EV5424-R-00A (8)	20	5	°C/W
JESD51-7 (9) (10)	44	9	°C/W

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) HBM is measured in accordance with JEDEC specification JESD22-A114. JEDEC document JEP155 states that a 500V HBM allows for safe manufacturing with a standard ESD control process.
6) CDM is measured in accordance with JEDEC specification JESD22-C101. JEDEC document JEP157 states that a 250V CDM allows for safe manufacturing with a standard ESD control process.
7) The device is not guaranteed to function outside of its operating conditions.
8) Measured on EV5424-R-00A, 4-layer PCB.
9) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes.
10) These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = V_{AVIN} = 5V, T_J = -40°C to +125°C (11), typical values are tested at T_J = 25°C, unless otherwise noted. (12)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown current	I_{SD}	RSTO_MODE = 01/11, PWRON = 0, T_J = 25°C		25	60	μA
Supply current	I_{IN}	FBx is high, no switching, T_J = 25°C		220	450	μA
Default switching frequency	f_{SW}		0.8	1.1	1.4	MHz
Thermal shutdown entry threshold (13)	T_{SD_ENTRY}			153		°C
Thermal shutdown recovery threshold (13)	$T_{SD\_RECOVERY}$			130		°C
Step-Down Regulator						
V_{AVIN} under-voltage lockout (UVLO) rising threshold	$V_{AVIN\_UVLO\_RISING}$		2.4	2.55	2.7	V
V_{AVIN} UVLO hysteresis	$V_{AVIN\_UVLO\_HYS}$			300		mV
V_{IN1} UVLO rising threshold	$V_{IN1\_UVLO\_RISING}$		2.3	2.45	2.6	V
V_{IN1} UVLO hysteresis	$V_{IN1\_UVLO\_HYS}$			300		mV
V_{IN2} UVLO rising threshold	$V_{IN2\_UVLO\_RISING}$		2.3	2.45	2.6	V
V_{IN2} UVLO hysteresis	$V_{IN2\_UVLO\_HYS}$			300		mV
V_{IN3} UVLO rising threshold	$V_{IN3\_UVLO\_RISING}$		2.3	2.45	2.6	V
V_{IN3} UVLO hysteresis	$V_{IN3\_UVLO\_HYS}$			300		mV
V_{IN4} UVLO rising threshold	$V_{IN4\_UVLO\_RISING}$		2.3	2.45	2.6	V
V_{IN4} UVLO hysteresis	$V_{IN4\_UVLO\_HYS}$			300		mV
V_{IN5} UVLO rising threshold	$V_{IN5\_UVLO\_RISING}$		2.3	2.45	2.6	V
V_{IN5} UVLO hysteresis	$V_{IN5\_UVLO\_HYS}$			300		mV
Feedback voltage	V_{FB1}	Buck 1 default output	1.029	1.05	1.071	V
	V_{FB2}	Buck 2 default output	1.01675	1.0375	1.0583	V
	V_{FB3}	Buck 3 default output	1.029	1.05	1.071	V
	V_{FB4}	Buck 4 default output	1.323	1.35	1.377	V
Maximum duty cycle (13)	D_{MAX}	Buck 1 to Buck 4		100		%
Buck 1 and Buck 3 (4.5A/4.5A)						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS1}$ / $R_{DS(ON)\_HS3}$	500mA, T_J = 25°C		25	35	mΩ
	$R_{DS(ON)\_HS1}$ / $R_{DS(ON)\_HS3}$	500mA, T_J = -40°C to +125°C		25	45	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS1}$ / $R_{DS(ON)\_LS3}$	500mA, T_J = 25°C		12	16	mΩ
	$R_{DS(ON)\_LS1}$ / $R_{DS(ON)\_LS3}$	500mA, T_J = -40°C to +125°C		12	20	mΩ
HS-FET switch leakage	I_{SWLK_HS1} / I_{SWLK_HS3}	Shutdown, V_{INx} = 5.5V, V_{SWx} = 0V or 5.5V, T_J = 25°C		0	1	μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = V_{AVIN} = 5V, T_J = -40°C to +125°C (11), typical values are tested at T_J = 25°C, unless otherwise noted. (12)

Parameter	Symbol	Condition	Min	Typ	Max	Units
LS-FET switch leakage	I_{SWLK_LS1} / I_{SWLK_LS3}	Shutdown, V_{INx} = 5.5V, V_{SWx} = 0V or 5.5V, T_J = 25°C		0	1	µA
HS-FET current limit	I_{LIMIT1} / I_{LIMIT3}	20% duty cycle, T_J = 25°C	5.7	7.6	9.3	A
Minimum on time (13)	t_{ON_MIN1}			50		ns
	t_{ON_MIN3}			50		ns
Minimum off time (13)	t_{OFF_MIN1}			120		ns
	t_{OFF_MIN3}			120		ns
Output discharge resistance	R_{OUT_DIS1}		3	7	20	Ω
Soft-start time	t_{SS_B1}	V_{OUTx} = 10% to 90%	140	300	430	µs
	t_{SS_B3}	V_{OUTx} = 10% to 90%	140	300	430	µs
Output over-voltage protection (OVP) rising threshold	V_{OVP1_RISING}	Buck 1	115	120	125	% of V_{REF}
		Buck 3	115	120	125	% of V_{REF}
Output OVP falling threshold	$V_{OVP1\_FALLING}$	Buck 1	105	110	115	% of V_{REF}
		Buck 3	105	110	115	% of V_{REF}
Buck 2 and Buck 4 (2.5A/2A)						
HS-FET on resistance	$R_{DS(ON)\_HS2}$ / $R_{DS(ON)\_HS4}$	500mA, T_J = 25°C		40	55	mΩ
	$R_{DS(ON)\_HS2}$ / $R_{DS(ON)\_HS4}$	500mA, T_J = -40°C to +125°C		40	70	mΩ
LS-FET on resistance	$R_{DS(ON)\_LS2}$ / $R_{DS(ON)\_LS4}$	500mA, T_J = 25°C		40	55	mΩ
	$R_{DS(ON)\_LS2}$ / $R_{DS(ON)\_LS4}$	500mA, T_J = -40°C to +125°C		40	85	mΩ
HS-FET switch leakage	I_{SWLK_HS2} / I_{SWLK_HS4}	Shutdown, V_{INx} = 5.5V, V_{SWx} = 0V or 5.5V, T_J = 25°C		0	1	µA
LS-FET switch leakage	I_{SWLK_LS2} / I_{SWLK_LS4}	Shutdown, V_{INx} = 5.5V, V_{SWx} = 0V or 5.5V, T_J = 25°C		0	1	µA
HS-FET current limit	I_{LIMIT2} / I_{LIMIT4}	20% duty cycle, T_J = 25°C	2.8	3.9	5	A
Minimum on time (13)	t_{ON_MIN2}			50		ns
	t_{ON_MIN4}			50		ns
Minimum off time (13)	t_{OFF_MIN2}			100		ns
	t_{OFF_MIN4}			100		ns
Output discharge resistance	R_{OUT_DIS2}		3	8	20	Ω
Soft-start time	t_{SS_B2}	V_{OUT} = 10% to 90%	140	300	430	µs
	t_{SS_B4}	V_{OUT} = 10% to 90%	140	300	430	ms
Output OVP rising threshold	V_{OVP2_RISING}	Buck 2	115	120	125	% of V_{REF}
		Buck 4	115	120	125	% of V_{REF}

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = V_{AVIN} = 5V, T_J = -40°C to +125°C (11), typical values are tested at T_J = 25°C, unless otherwise noted. (12)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output OVP falling threshold	$V_{OVP2\_FALLING}$	Buck 2	105	110	115	% of V_{REF}
		Buck 4	105	110	115	% of V_{REF}
Load Switch						
Operating input voltage range	V_{IN_LSW}		2.7		5.5	V
Load switch on resistance	$R_{DS(ON)\_LSW}$	V_{LSWI} = 5V, 1A load		50		mΩ
Output discharge resistance	R_{OUT_DIS3}		3	7	20	Ω
Soft-start slew rate	t_{SS_LSW}	C_{OUT} = 10µF		1.5		mV/µs
Low Dropout (LDO) Regulators (LDO 2, LDO 4, and LDO 5)						
Output voltage	V_{LDO2}	I_{OUT} = 10mA	1.764	1.8	1.836	V
	V_{LDO4}	I_{OUT} = 10mA	3.234	3.3	3.366	V
	V_{LDO5}	I_{OUT} = 10mA	3.234	3.3	3.366	V
PSRR (13)	$PSRR_{1k}$	LDO4 and LDO5, V_{OUTx} = 1.8V		52		dB
Dropout voltage	V_{DROP1}	V_{OUTx} = 3V, I_{OUT} = 300mA		50		mV
Current limit	I_{LIMIT_LDO2}	V_{INx} = 3.3V, V_{OUTx} drops 33%	300	430	600	mA
	$I_{LIMIT\_LDO\_LS}$	LDO4 and LDO5 set ILIM bit to 0, V_{INx} = 3.3V, V_{OUTx} drops 33%	380	520	660	mA
	$I_{LIMIT\_LDO\_HS}$	LDO4 and LDO5 set ILIM bit to 1, V_{INx} = 3.3V, V_{OUTx} drops 33%	580	790	1000	mA
Output discharge resistance	R_{OUT_DIS4}		3	7	20	Ω
Soft-start time	t_{SS_B2}	V_{OUTx} = 10% to 90%, C_{OUT} = 2.2µF		50		µs
Line regulation		V_{IN2} = V_{IN5} = 2.8V to 5.5V		0.3		%/V
Load regulation		V_{IN2} = V_{IN5} = 3.3V, I_{OUT} = 10mA to 100mA		0.5		%
Logic Pins						
PWRON pull-up current	I_{PWRON}	AVIN is pulled up internally	5	9	13	µA
PWRON rising threshold	V_{PWR_RISING}		0.8	1	1.2	V
PWRON voltage hysteresis	V_{PWR_HYS}			100		mV
EN1 rising threshold	V_{PWR_RISING}		0.8	1	1.2	V
EN1 voltage hysteresis	V_{PWR_HYS}			100		mV
PG rising threshold	V_{PG_RISING}	RSTO_MODE = 01	86	90	94	% of V_{FB}
PG falling threshold	$V_{PG\_FALLING}$	RSTO_MODE = 01	76	80	84	% of V_{FB}
PFI rising threshold	V_{PFI_RISING}	RSTO_MODE = 10	3.8	4	4.2	V
PFI hysteresis	V_{PFI_HYS}			7		% of V_{PFI_RISING}
RSTO rising delay	t_{DELAY_RSTO}	Adjustable via the I²C/MTP	30	50	70	ms

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = V_{AVIN} = 5V, T_J = -40°C to +125°C (11), typical values are tested at T_J = 25°C, unless otherwise noted. (12)

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specifications (14)						
Input logic high	V_{IN_HIGH}		1.4			V
Input logic low	V_{IN_LOW}				0.4	V
Output voltage logic low	V_{OUT_LOW}	RSTO pin, 4mA sink			0.4	V
SCL clock frequency	f_{SCL}				3.4	MHz
SCL high time	t_{HIGH_SCL}		60			ns
SCL low time	t_{LOW_SCL}		160			ns
Data setup time	t_{SU_DATA}		10			ns
Data hold time	t_{HD_DATA}			70		ns
Set-up time for repeated start	$t_{SU.START}$		160			ns
Hold time for repeated start	$t_{HOLD.START}$		160			ns
Bus free time between a start and a stop condition	t_{BUS_FREE}		160			ns
Set-up time for stop condition	t_{SU_STOP}		160			ns
Rise time of SCL and SDA	t_{RISE}		10		300	ns
Fall time of SCL and SDA	t_{FALL}		10		300	ns
Suppressed spike pulse width	t_{SPIKE}		0		50	ns
Capacitance for each bus line	C_{BUS}				400	pF

Notes:

11) Guaranteed by over-temperature correlation. Not tested in production.
12) Tested with default version (MP5424GRM-0000), unless otherwise noted.
13) Guaranteed by engineering sample characterization.
14) It is recommended to use I²C function after the start-up sequence is complete (e.g. all enabled power rails have completed start up). Figure 2 shows the I²C timing diagram for reading the I²C interface specifications.

I²C TIMING DIAGRAM

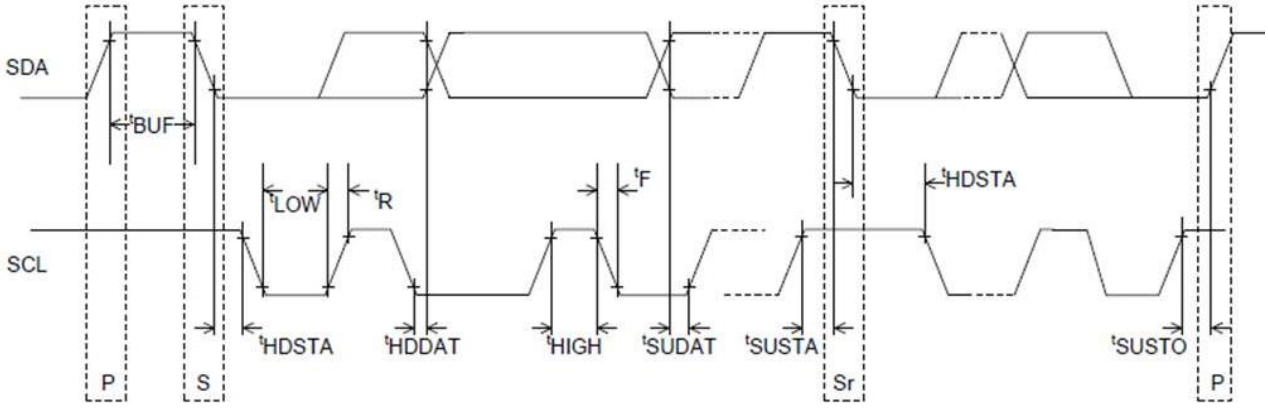

Figure 2: I²C Timing Diagram

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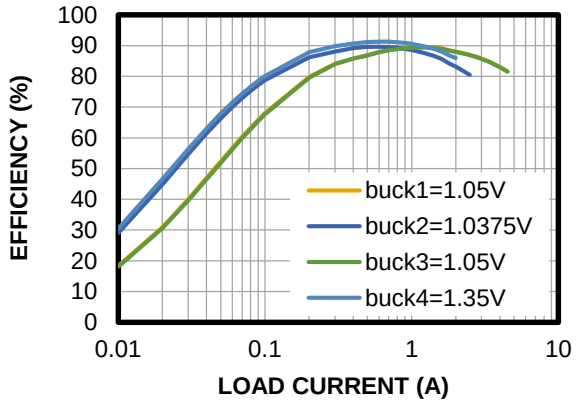
TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board, V_{IN} = 5V, T_A = 25°C, tested using default spec parts, unless otherwise noted.

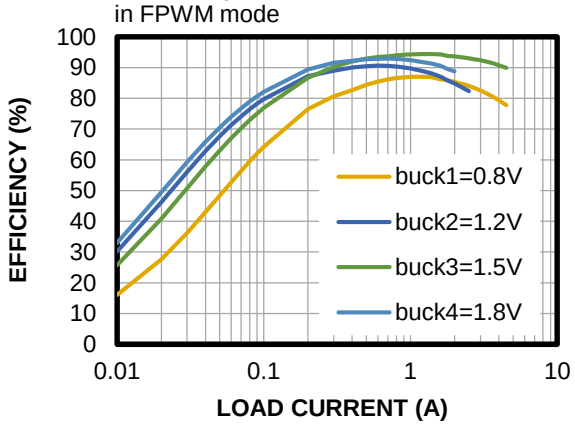
Efficiency vs. Load Current

V_{IN} = 5V, f_{SW} = 1.1MHz, all bucks operate in FPWM mode

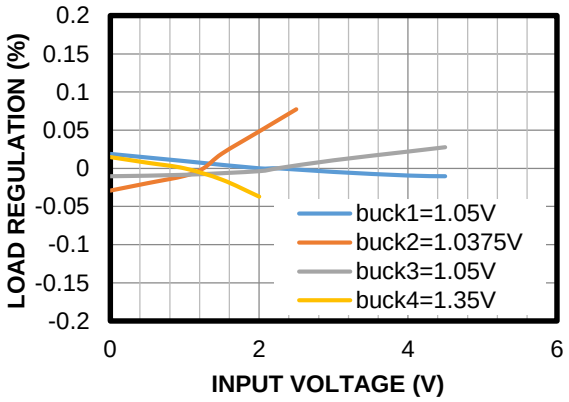


Efficiency vs. Load Current

V_{IN} = 5V, f_{SW} = 1.1MHz, all bucks operate in FPWM mode

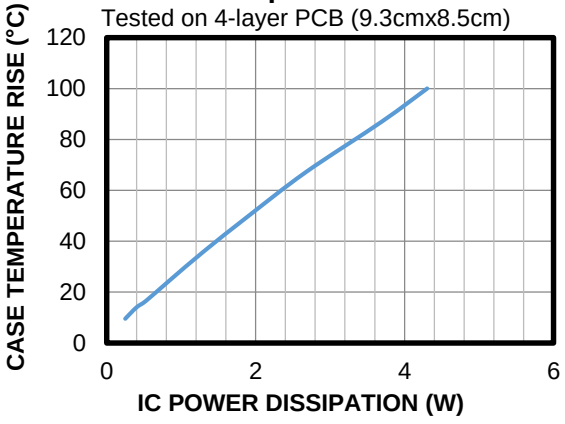


Load Regulation

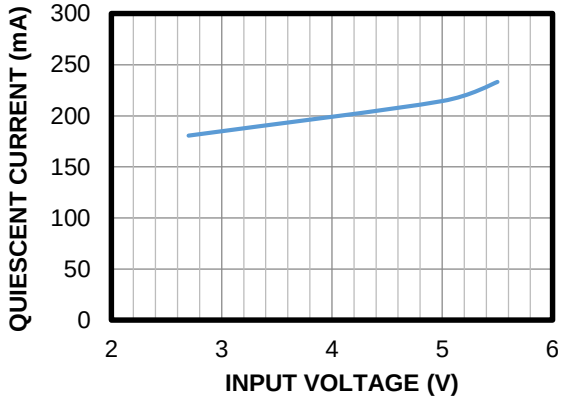


Case Temperature Rise vs. IC Power Dissipation

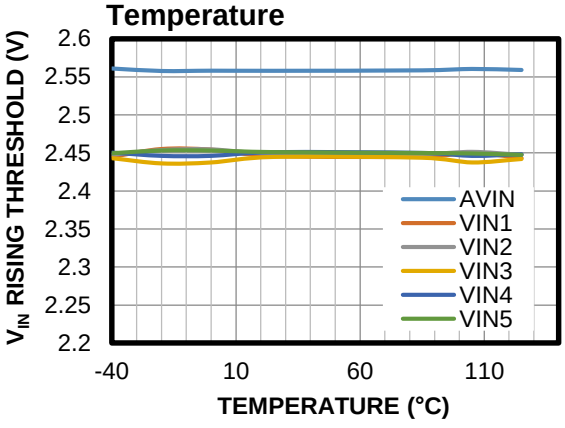
Tested on 4-layer PCB (9.3cmx8.5cm)



Quiescent Current vs. Input Voltage



V_{IN} Rising Threshold vs. Temperature



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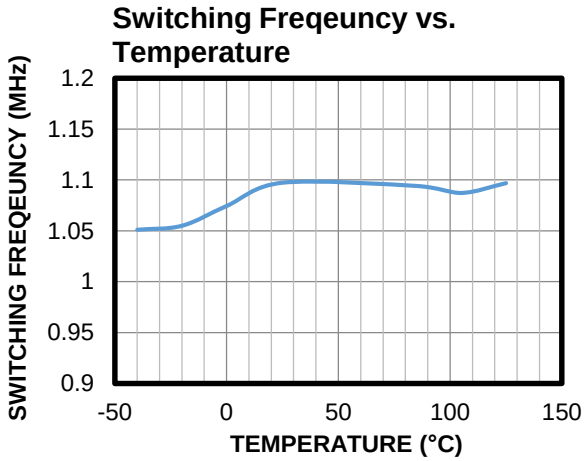
TYPICAL CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 5V, T_A = 25°C, tested using default spec parts, unless otherwise noted.



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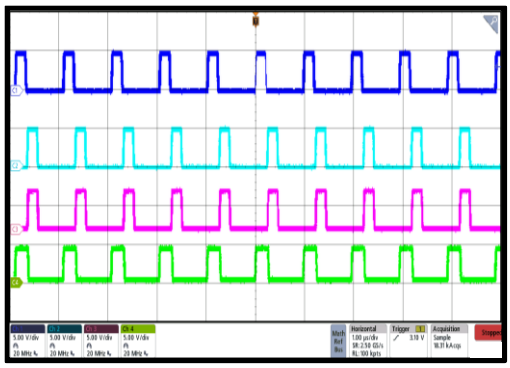
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board, V_{IN} = 5V, T_A = 25°C, tested using default spec parts, unless otherwise noted.

Steady State
All buck rails, no load

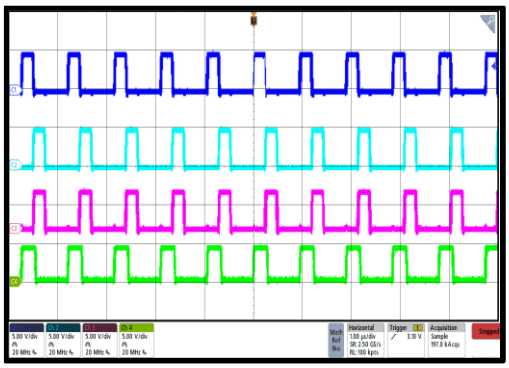
CH1: V_{SW1} 5V/div.
CH2: V_{SW2} 5V/div.
CH3: V_{SW3} 5V/div.
CH4: V_{SW4} 5V/div.



1µs/div.

Steady State
All buck rails, full load

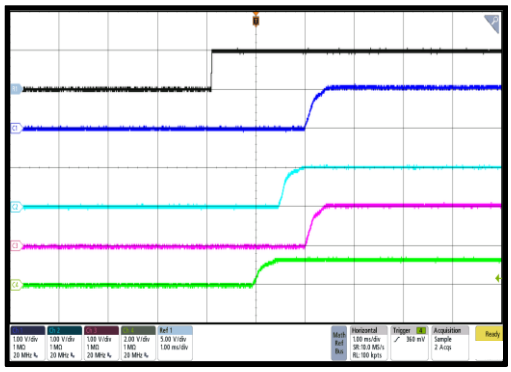
CH1: V_{SW1} 5V/div.
CH2: V_{SW2} 5V/div.
CH3: V_{SW3} 5V/div.
CH4: V_{SW4} 5V/div.



1µs/div.

Start-Up through PWRON
All buck rails, no load

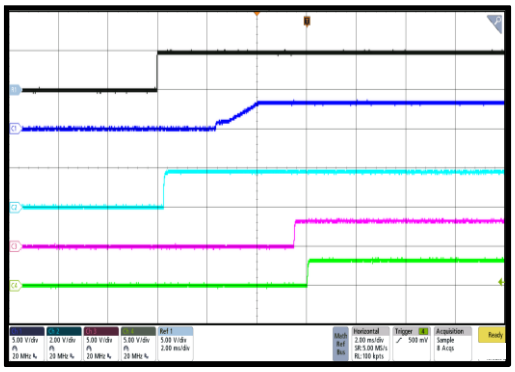
Ref: V_{PWRON} 5V/div.
CH1: Buck 1 1V/div.
CH2: Buck 2 1V/div.
CH3: Buck 3 1V/div.
CH4: Buck 4 2V/div.



1ms/div.

Start-Up through PWRON
All LDO rails, no load, V_{LSWI} = 3.3V

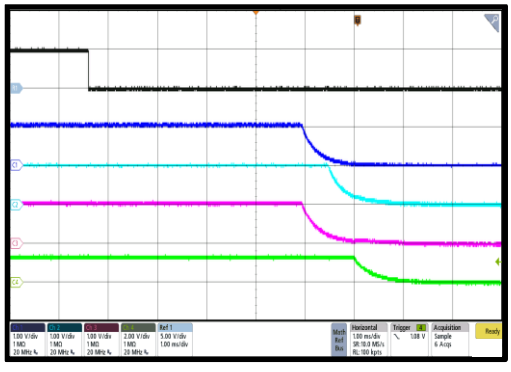
Ref: V_{PWRON} 5V/div.
CH1: V_{LSWO} 5V/div.
CH2: LDO 2 2V/div.
CH3: LDO 4 5V/div.
CH4: LDO 5 5V/div.



2ms/div.

Shutdown through PWRON
All buck rails without load

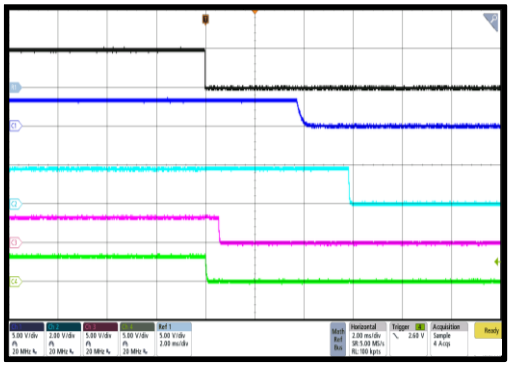
Ref: V_{PWRON} 5V/div.
CH1: Buck 1 1V/div.
CH2: Buck 2 1V/div.
CH3: Buck 3 1V/div.
CH4: Buck 4 2V/div.



1ms/div.

Shutdown through PWRON
All LDO rails, no load, V_{LSWI} = 3.3V, all buck rails disabled

Ref: V_{PWRON} 5V/div.
CH1: V_{LSWO} 5V/div.
CH2: LDO 2 2V/div.
CH3: LDO 4 5V/div.
CH4: LDO 5 5V/div.



2ms/div.

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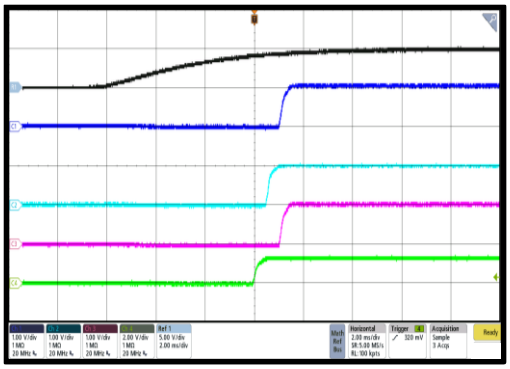
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 5V, T_A = 25°C, tested using default spec parts, unless otherwise noted.

Start-Up through VIN

All buck rails, no load

Ref: V_{IN} 5V/div.
CH1: Buck 1 1V/div.
CH2: Buck 2 1V/div.
CH3: Buck 3 1V/div.
CH4: Buck 4 2V/div.

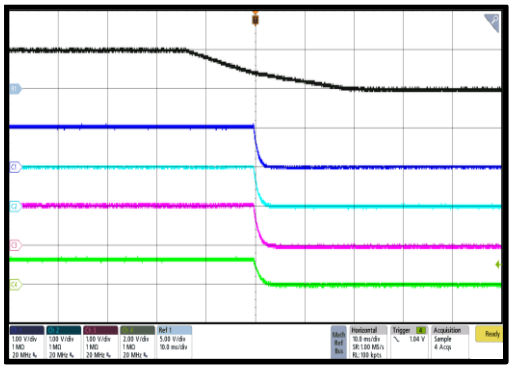


2ms/div.

Shutdown through VIN

All buck rails, no load

Ref: V_{IN} 5V/div.
CH1: Buck 1 1V/div.
CH2: Buck 2 1V/div.
CH3: Buck 3 1V/div.
CH4: Buck 4 2V/div.

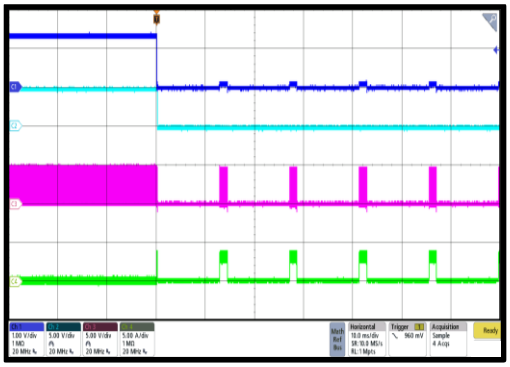


10ms/div.

SCP Entry

Buck 4 output = 1.35V, RSTO_MODE = 01

CH1: Buck 4 1V/div.
CH2: V_{RSTO} 5V/div.
CH3: V_{SW4} 5V/div.
CH4: I_{L4} 5A/div.

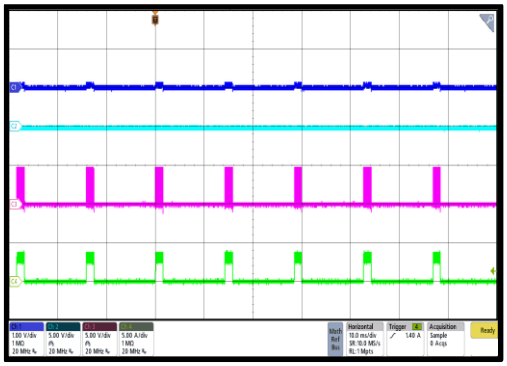


10ms/div.

SCP Steady State

Buck 4 output = 1.35V, RSTO_MODE = 01

CH1: Buck 4 1V/div.
CH2: V_{RSTO} 5V/div.
CH3: V_{SW4} 5V/div.
CH4: I_{L4} 5A/div.

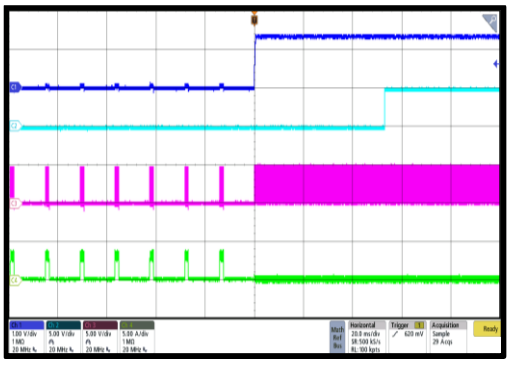


10ms/div.

SCP Recovery

Buck 4 output = 1.35V, RSTO_MODE = 01

CH1: Buck 4 1V/div.
CH2: V_{RSTO} 5V/div.
CH3: V_{SW4} 5V/div.
CH4: I_{L4} 5A/div.

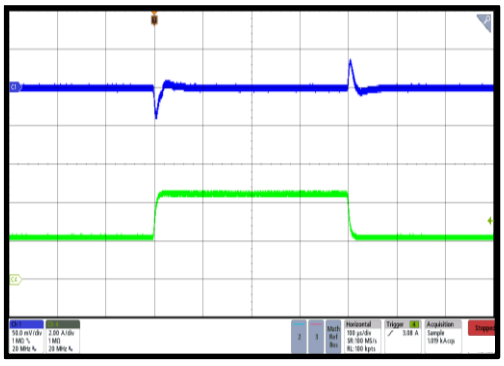


20ms/div.

Load Transient Response

I_{OUT} transient from 2.25A to 4.5A, 2.5A/µs slew rate

CH1: Buck 1/AC 50mV/div.
CH4: I_{OUT1} 2A/div.



100µs/div.

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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

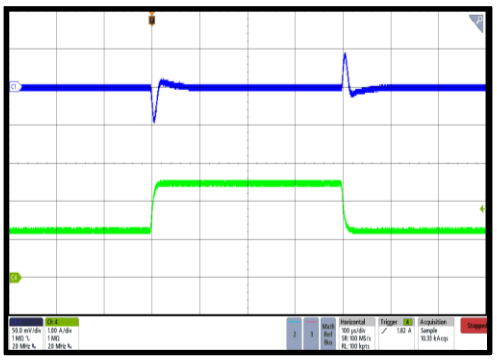
Performance waveforms are tested on the evaluation board, V_{IN} = 5V, T_A = 25°C, tested using default spec parts, unless otherwise noted.

Load Transient Response

I_{OUT} transient from 1.25A to 2.5A,
2.5A/µs slew rate

CH1:
Buck 2/AC
50mV/div.

CH4: I_{OUT2}
1A/div.



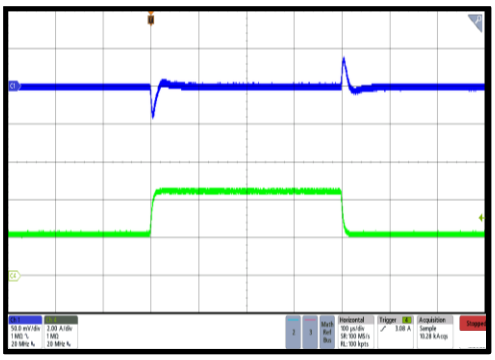
100µs/div.

Load Transient Response

I_{OUT} transient from 2.25A to 4.5A,
2.5A/µs slew rate

CH1:
Buck 3/AC
50mV/div.

CH4: I_{OUT3}
2A/div.



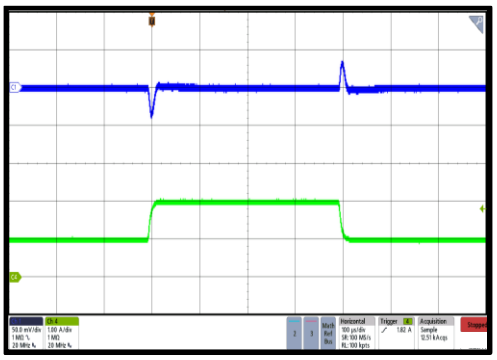
100µs/div.

Load Transient Response

I_{OUT} transient from 1A to 2A,
2.5A/µs slew rate

CH1:
Buck 4/AC
50mV/div.

CH4: I_{OUT4}
1A/div.



100µs/div.

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FUNCTIONAL BLOCK DIAGRAM

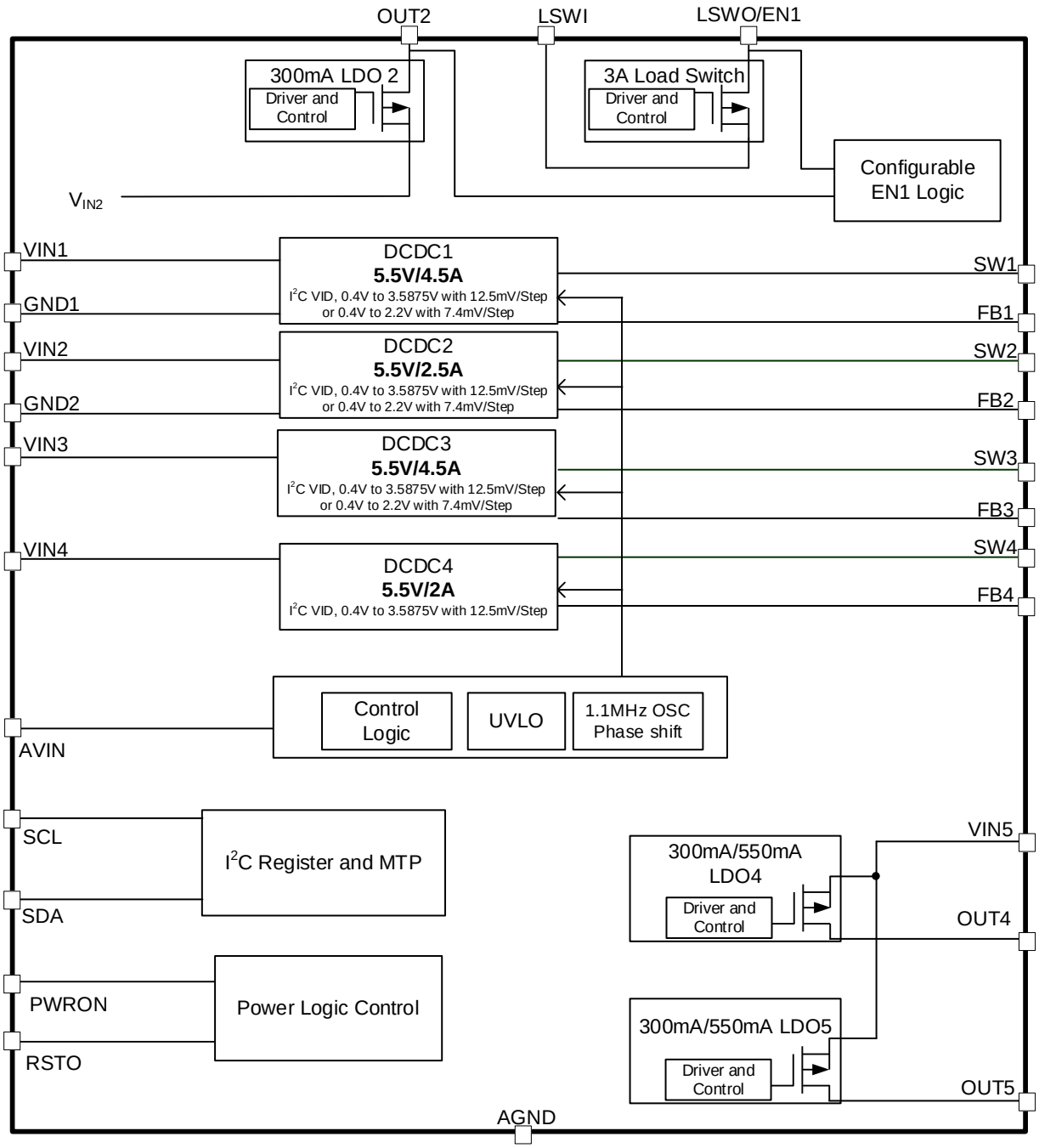

Figure 3: Functional Block Diagram

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OPERATION

The MP5424 provides a complete power management solution for 5V systems**,** such as televisions**.** It integrates four high-frequency, synchronous rectification, step-down switch-mode converters, as well as three low-dropout (LDO) regulators and one load switch. The compact QFN-26 (3.5mmx4.5mm) package reduces component count and PCB space.

The default output voltage (V_{OUT}), start-up sequence, and dynamic voltage scaling can be adjusted via the I²C and multiple-time programmable (MTP) interfaces. The I²C also provides powerful logic functions. See the I²C Register Map section on page 35 for more details**.**

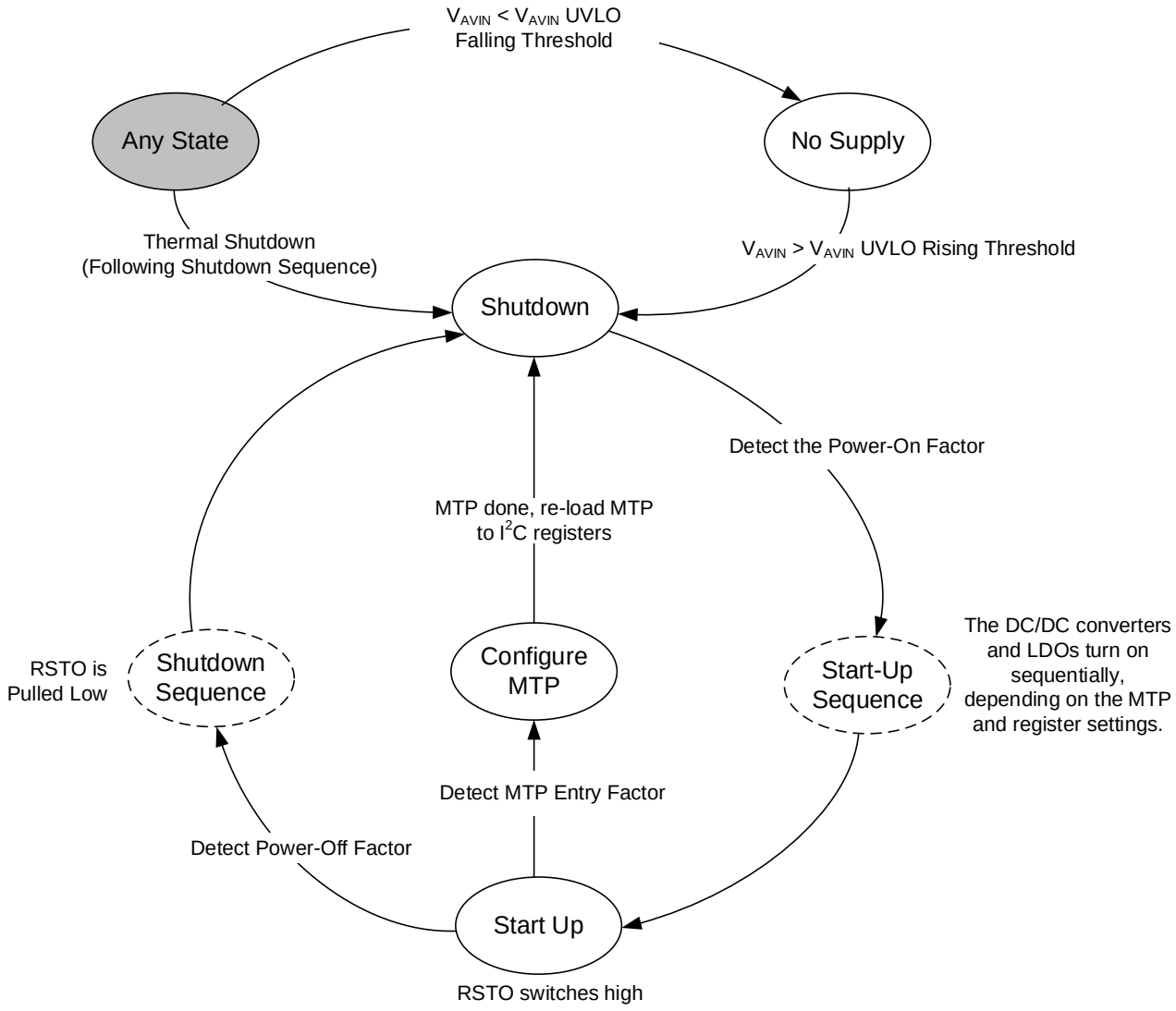

Figure 4: Power Control State Machine Diagram

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Power Control

State Machine Description

The state machine has a number of status options, including no supply, shutdown, start-up sequence, start-up, shutdown sequence, configure MTP, and shutdown event (see Figure 4 on page 17). These statuses are described below.

No Supply

The PMIC's input pin (AVIN) has a UVLO detection circuit. If the input voltage (V_{AVIN}) drops below the under-voltage lockout (UVLO) rising threshold, then all of the PMIC's functions are disabled.

Shutdown

All of the power rails turn off, and the PMIC enters the shutdown state once V_{AVIN} drops below its UVLO falling threshold. In the shutdown state, the PMIC monitors the power-on factors. Once a power-on factor is detected, the device begins the start-up sequence.

Start-Up Sequence

The DC/DC converters, LDOs, and load switch turn on sequentially according to the order configured via the MTP e-fuse.

Start-Up

The DC/DC converters, LDOs and load switch turn on, and the RSTO pin's output goes high. In the start-up state, the PMIC monitors the power-off factors and configure MTP factors.

Shutdown Sequence

If the PMIC detects the shutdown factors during a start-up state, then the PMIC enters the shutdown sequence. RSTO is pulled low. Then the DC/DC converters, LDOs, and load switch turn off sequentially according to the order configured via the MTP e-fuse.

MTP Configure

The buck converters, LDOs, and load switch turn off in the shutdown sequence when entering MTP mode. After MTP configuration is complete, the PMIC reloads the MTP to the I²C registers and monitors the power-on factors.

Shutdown Event

If the PMIC detects any of the following conditions, then it enters a no supply or shutdown state, regardless of the current state.

- If the input voltage (V_{IN}) drops below the UVLO falling threshold, then the device enters a no supply state.
- If thermal shutdown is triggered, then the device enters a shutdown state.

Power-On Factor

The PMIC has several power-on factors, including PWR_ON, thermal recovery, and EN1. These factors are described below.

PWRON_ON

If the PWRON pin is pulled to logic high (PWRON_MODE = 0) or there is a falling edge on the PWRON pin (PWRON_MODE = 1), then the PMIC enters the start-up sequence. See the PWRON Functions section on page 21 for more details.

Thermal Recovery

If the die temperature exceeds the thermal shutdown threshold, then the PMIC enters the shutdown state. Once the die temperature drops below the threshold, the PMIC enters the start-up sequence.

EN1

If the EN1 function is enabled, and EN1 is pulled high (EN1_INV defines EN1's active high) or EN1 is pulled low (EN1_INV defines EN1's active low), then the power rails controlled by EN1 enter the start-up sequence. See the EN1 Functions section on page 22 for more details.

Start-Up Sequence

There are 16 selectable time slots for the start-up sequence. All of the DC/DC converters, LDOs, and load switch can be configured between 0 and 15 time slots by the MTP e-fuse. The delay time between each time slot can be adjusted via the MTP TIME_SLOT bits. The time does not change with the switching frequency (f_{SW}).

RSTO goes high with the RSTO_DELAY time once the start-up sequence is complete. The DC/DC converter, LDOs, and load switch start-up sequences are set by POWER_ON_SLOT_

NO and PWR_ON_TIME_SLOT_MODE. See the MTP E-Fuse Description on page 28 for more details.

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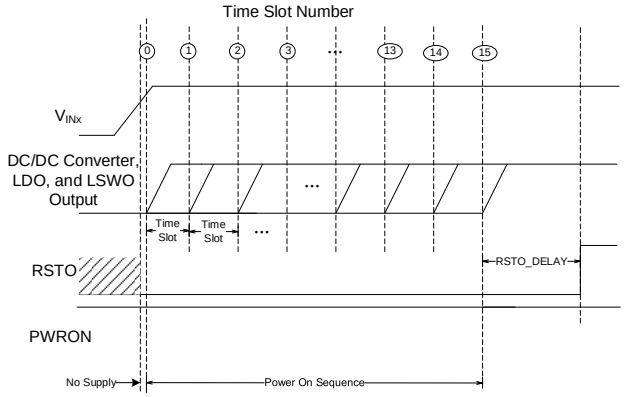

Figure 5: Start-Up Sequence

Buck Regulators, LDOs, and Load Switch On

The MP5424 provides a configurable start-up sequence. See the MTP E-Fuse Configuration Table on page 26 for details on which bits set the time slot number for each channel.

Shutdown Factor

The PMIC shutdown factors are PWRON_OFF and EN1. They are described below.

PWRON_OFF

If the PWRON pin is pulled low (PWRON_MODE = 0) or if there is a falling edge on PWRON (PWRON_MODE = 1), then the PMIC enters the shutdown sequence. See the PWRON Functions section on page 21 for more details.

EN1

If the EN1 function is enabled, and EN1 is pulled low (EN1_INV defines EN1 as active high) or EN1 is pulled high (EN1_INV defines EN1 as active low), then the power rails controlled by EN1 enter the shutdown sequence. See the EN1 Functions section on page 22 for more details.

Shutdown Sequence

There are 16 selectable time slots for the shutdown sequence. All of the DC/DC converters, LDOs, and load switch can be configured between 0 and 15 time slots by the MTP e-fuse. The delay time between each time slot can be adjusted via the MTP TIME_SLOT bits. The time does not change with f_{SW}.

RSTO is pulled low prior to when the DC/DC converters, LDOs, and load switch turn off. The DC/DC converter and LDO shutdown sequences are set by POWER_OFF_SLOT_NO and POWER_OFF_SLOT_MODE. See the MTP E-Fuse Configuration Table on page 26 for more details.

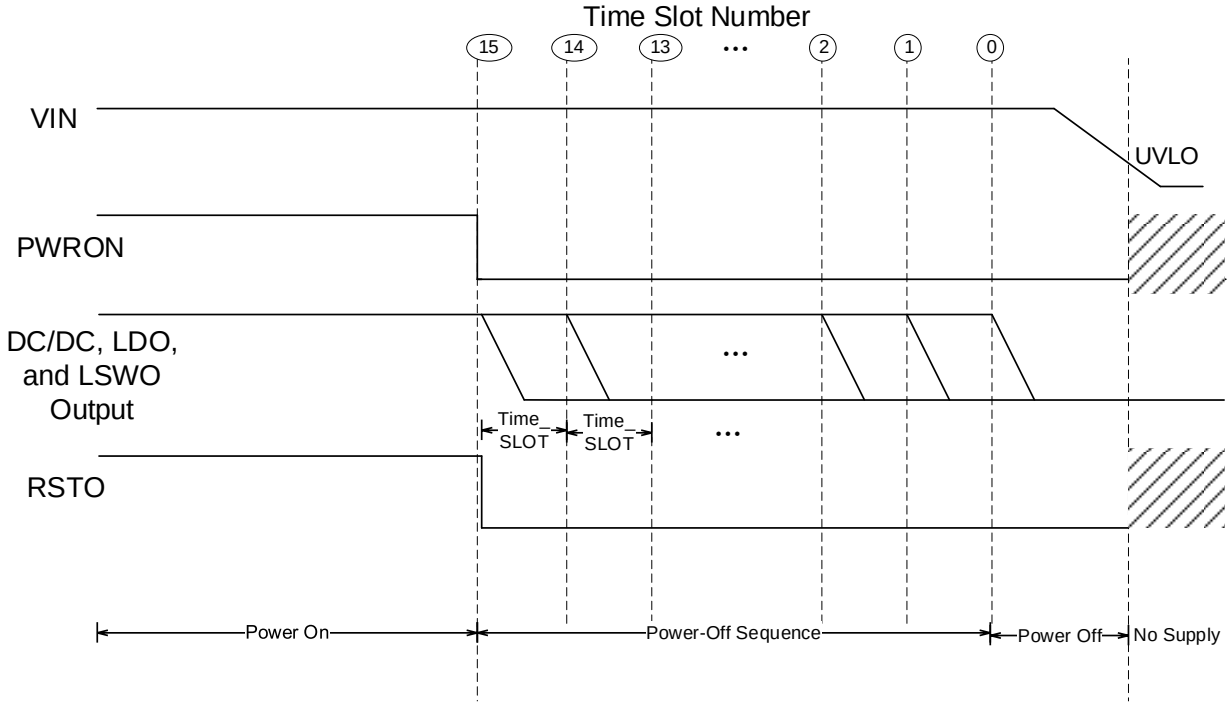

Figure 6: Shutdown Sequence (PWRON_MODE = 0)

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Configurable MTP

Follow the steps below to configure the MTP e-fuse via the I²C interface:

1. Before configuring the e-fuse, ensure that all of the buck converters and LDOs have no load.
2. Write the correct MTP program password to register 0x26.
3. Set ENTER_MTP_MODE to 1 to enter MTP configure mode. All bucks and LDOs are turned off in this mode.
4. Write the desired content to the I²C registers.
5. Set V_{IN1} and V_{AVIN} between 6.4V and 6.5V, with a minimum 150mA current capability.
6. Set PROGRAM_MTP to 1 to start the MTP e-fuse program.
7. The PMIC calculates the sum of all the related I²C registers to be burned to the MTP register. The checksum result is also written to the MTP register.
8. After the MTP write operation is complete (typically 100ms), the PMIC sets the PROGRAM_MTP bit to 0, and the I²C register write protection is unlocked. ENTER_MTP_MODE is also set to 0.
9. After MTP configuration, the PMIC reloads the MTP to the related I²C registers and the PWRON pin function is re-enabled. Then the bucks, LDOs, and load switch then start-up based on their power-on factors. I²C communication is enabled after the start-up sequence is complete.
10. Decrease V_{IN1} and V_{AVIN} below 5.5V, then restart the power supply to resume normal operation.

Before loading the MTP data into the I²C register during a start-up through VIN, the PMIC does a checksum calculation for all of the related MTP registers, and compares the checksum calculation to the checksum byte. If they match, then the MTP data is loaded into the I²C register. If they do not match, then the I²C register uses the hard-coded default value. There is an I²C register flag bit to indicate a checksum error.

Shutdown Sequence

If the V_{INx} drops below its UVLO falling threshold or if thermal shutdown is triggered, then the PMIC enters the shutdown sequence. All of the DC/DC converters, LDO regulators, and load switch turn off at the same time.

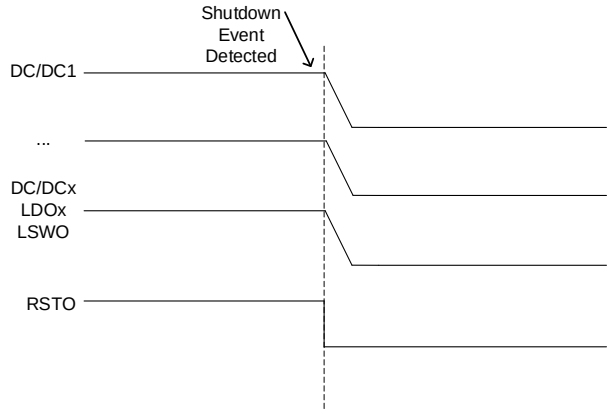

Figure 7: Shutdown Sequence

High-Efficiency Buck Converter

Buck 1, buck 2, buck 3, and buck 4 are synchronous, step-down DC/DC converters that have built-in UVLO protection, soft start (SS), compensation, and over-current protection (OCP) with hiccup mode. Constant-on-time (COT) control with fixed frequency provides fast transient response. The switching clock is phase-shifted from buck 1 to buck 4 during continuous conduction mode (CCM). All of the buck converters can support a 100% duty cycle.

Power Supply and Under-Voltage Lockout (UVLO) Protection

VIN1 is the power supply for buck 1. VIN2 is the power supply for buck 2, LDO2. VIN3 is the power supply for buck 3. VIN4 is the power supply for buck 4. VIN5 is the power supply for LDO 4 and LDO 5. LSWI is the power supply for load switch. AVIN is the power input to bias the internal logic blocks.

VIN1, VIN2, VIN3, VIN4, VIN5, and AVIN have their own UVLO thresholds with hysteresis. Once V_{AVIN} exceeds its UVLO rising threshold, the PWRON logic is enabled and ready to accept start-up and shutdown commands.

Internal Soft Start (SS)

SS is implemented to prevent the PMIC V_{OUT} from overshooting during start-up. As the PMIC starts up, the internal circuitry of each power rail generates a soft-start voltage (V_{SS}) that ramps up from 0V. The soft-start time (t_{SS}) lasts until V_{SS}

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exceeds the reference voltage (V_{REF}). Once V_{SS} exceeds V_{REF}, then V_{REF} takes over as the reference. The four buck outputs' t_{SS} are adjustable via the MTP. For the LDO2 through LDO5 outputs, t_{SS} is fixed internally at 50µs. For the load switch, the soft-start slew rate is consistent at 1.5mV/µs.

Output Discharge

In order to discharge the output capacitor (C_{OUT}) during the shutdown sequence, there is a passive discharge path from the DC/DC converter outputs, LDO outputs, and load switch output to ground. The discharge path turns on once the corresponding channel is disabled. The typical discharge resistance is 7Ω. The discharge function can be enabled or disabled through the I²C interface.

Over-Voltage Protection (OVP)

The MP5424 monitors the feedback voltage (V_{FB}) to detect possible over-voltage (OV) conditions. If V_{FB} exceeds 120% of the target voltage, then both the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) turn off, and the discharge path is turned on. The part exits this regulation period once V_{FB} drops below 110% of V_{REF}.

Over-Current Protection (OCP)

If the peak inductor current (I_{L_PEAK}) reaches its set limit and the HS-FET is on, then OCP is triggered. The LS-FET turns on until the inductor current (I_L) drops to the valley current limit (I_{LIMIT_VALLEY}). Once I_L reaches I_{LIMIT_VALLEY}, then the HS-FET turns on. The part does not exit OCP unless I_{L_PEAK} drops below its set limit. If the OCP lasts longer than 150µs, then the buck enters hiccup mode.

System Control Signals

PWRON Functions

PWRON is an input pin to that generates a start-up or shutdown event. This pin can be configured to detect a level or a falling edge via the MTP.

If the PWRON_MODE bit is set to 1, then the PWRON_DEBOUNCE_TIMER bit can set the PWRON pin's debounce timer to filter mechanical switch short-press noise.

If the PWRON_MODE bit is set to 0, then PWRON operates as an enable (EN) pin. Pull PWRON high to turn the PMIC on; pull PWRON low to turn it off.

PWRON_MODE = 1 (Edge Trigger)

Start-Up

The start-up sequence begins once V_{AVIN} exceeds its UVLO threshold and PWRON is pulled low for longer than PWRON_DEBOUNCE_TIMER while the PMIC is off. Once the start-up sequence is complete, then the PWRON detection function can be enabled.

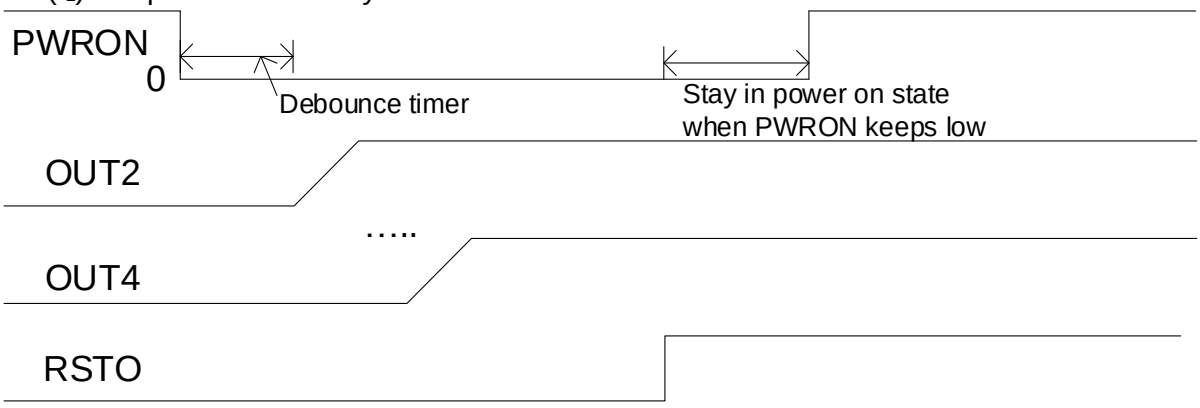

Figure 8: PWRON_MODE = 1 (Press PWRON to Start Up)

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Shutdown

The shutdown sequence begins once PWRON is pulled low for longer than PWRON_DEBOUNCE_TIMER while the PMIC is on. The MP5424 turns off all of the bucks, LDOs, and load switch. The shutdown sequence can be configured via the MTP e-fuse.

If the PWRON pin remains low after the shutdown sequence is complete, then the MP5424 remains in the shutdown state. If the PWRON pin is pulled high after the shutdown sequence is complete, then the MP5424 continues the shutdown sequence.

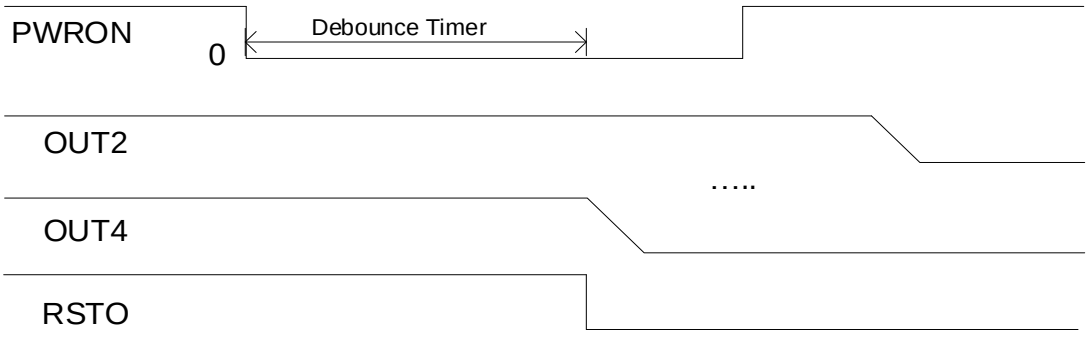

Figure 9: PWRON_MODE = 1 (Press PWRON to Shutdown)

PWRON_MODE = 0 (Level Trigger)

The PMIC enters the start-up sequence once V_{AVIN} exceeds its UVLO threshold and PWRON is pulled high.

If PWRON is pulled low while the MP5424 is on, then the device executes the shutdown sequence. If PWRON is pulled high while the MP5424 is off, then the MP5424 executes a start-up sequence. During a start-up or shutdown sequence, the PWRON pin function is blanked until the sequence is complete. For example, if PWRON is high during a shutdown sequence and then the PMIC finishes the shutdown sequence, the PMIC executes the start-up sequence (see Figure 10).

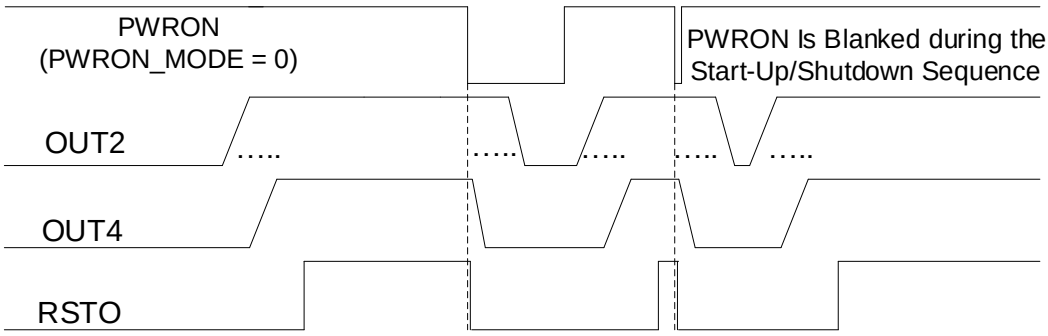

Figure 10: PWRON Enable and Disable Function

EN1 Functions

EN1 is a multi-function pin. The LSWO pin and LDO 2 can be selected as EN1's input according to the EN1_SELECT bit of CLT3 register. EN_EN1_Pin bit can enable/ disable EN1 functions. EN1_INV defines EN1 as active high or active low.

The EN1 pin can be used to control the power rails' start-up and shutdown sequences. This is useful for non-I²C interface applications.

Figure 11 on page 23 shows the EN1 function. If EN1_INV is high and EN1 controls buck 2 and buck 3, then buck 2 and buck 3 turn off sequentially when EN1 is pulled low. If EN1 is pulled high, buck 2 and buck 3 turn on sequentially. PWRON has a higher priority than EN1, so if PWRON is pulled low, then all of the power rails enter the shutdown sequence. The buck, LDO, and load switch enable/disable functions are controlled via the PWRON and EN1 pins.

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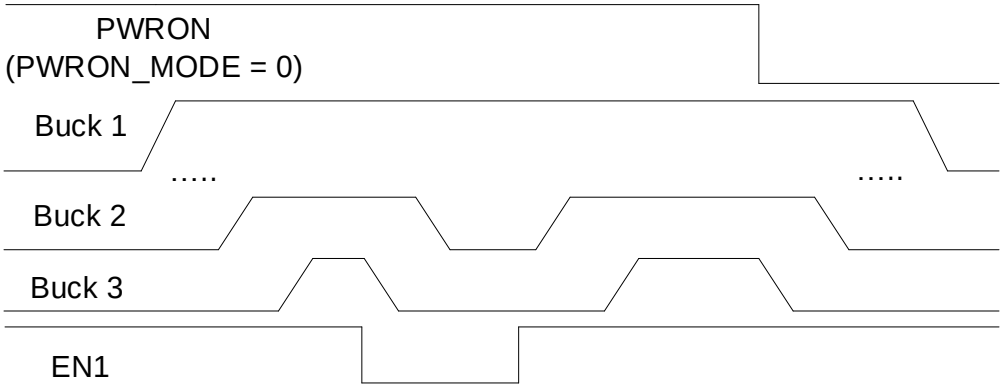

Figure 11: EN1 Function

Thermal Warning and Shutdown

Thermal warning and thermal shutdown prevent the part from operating at exceedingly high temperatures. If the silicon die temperature exceeds 120°C, then the MP5424 sets the OTWARNING bit to 1.

If the die temperature exceeds 153°C, then the MP5424 sets the OTEMPP bit to 1 and the system enters the shutdown sequence. Once the temperature drops to 130°C, the system enters the start-up sequence.

I²C Timing

The PMIC's I²C interface is powered by an internal, fixed, 2V power supply. If V_{INx} exceeds its UVLO threshold during a start-up through VIN, then the 2V LDO power supply is ready. The I²C function is disabled during the start-up sequence. Once the start-up sequence is complete for all enabled power rails, the I²C function is available (see Figure 12).

If the I²C is not used, SCL and SDA should be pulled high via a resistor.

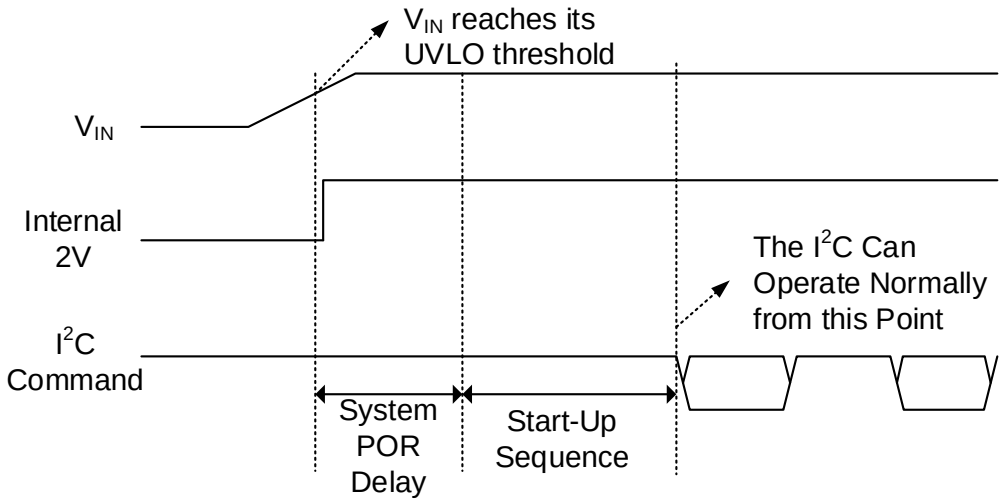

Figure 12: I²C Timing Diagram

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I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional serial interface consisting of a data line (SDA) and a clock line (SCL). These lines are pulled up externally to a bus voltage (V_{BUS}) when idle. A master device is connected to the line. The master generates the SCL signal and device address, and arranges the communication sequence.

The MP5424 interface is an I²C slave that can support fast mode (400kHz) and high-speed mode (3.4Mhz). The I²C interface adds flexibility to the power supply solution. Among other parameters, V_{OUT} and the transition slew rate can be controlled via the I²C interface. If the master sends the address as an 8-bit value, then the 7-bit address should be followed by a 0 to indicate a read (R) operation or 1 to indicate a write (W) operation.

Start and Stop Conditions

The start (S) and stop (P) conditions are signaled by the master device, and signify the beginning and the end of an I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 13).

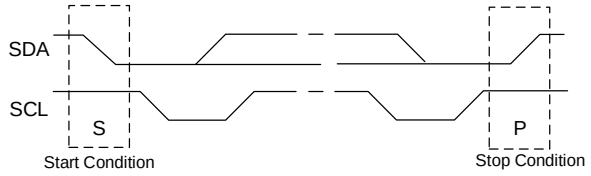

Figure 13: Start (S) and Stop (P) Conditions

The master then generates the SCL clocks, and transmits the device address and the read/write direction bit (R/W) on the SDA line.

Transfer Data

Data is transferred in 8-bit bytes via the SDA line. Each byte of data should be followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MP5424 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP5424 acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP5424. The MP5424 performs an update on the falling edge of the LSB byte. Figure 14, Figure 15, and Figure 16 show examples of I²C write and read sequences.

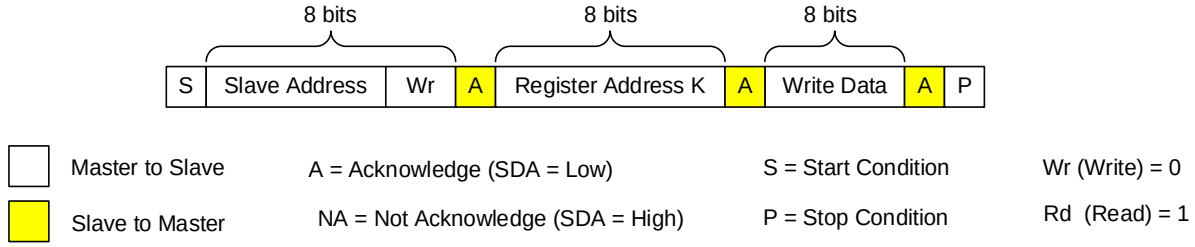

Figure 14: Write Single Register

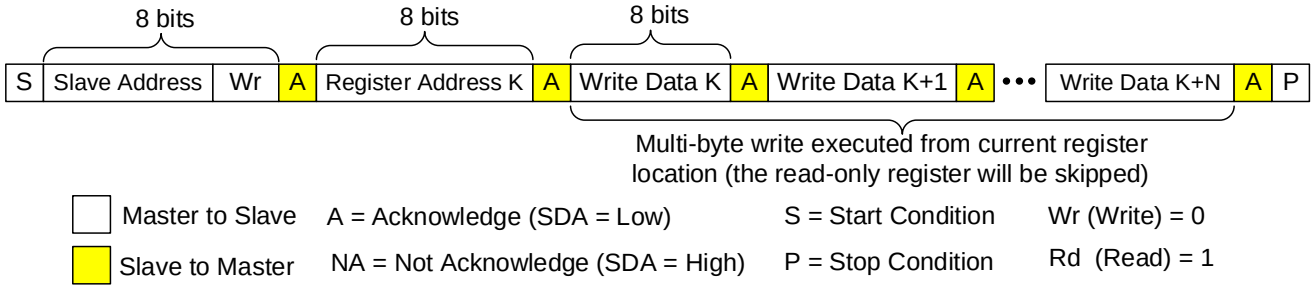

Figure 15: Write Multi-Register

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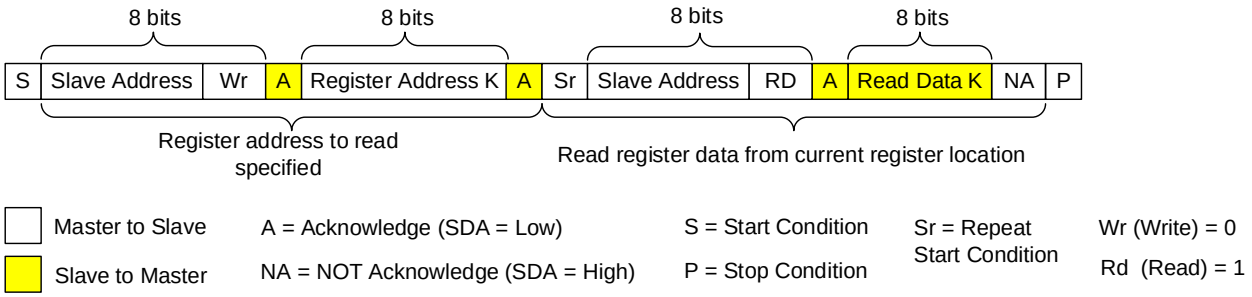

Figure 16: Read Single Register

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REGISTER DESCRIPTION

MTP E-Fuse Configuration Table

Offset	Name	D7	D6	D5	D4	D3	D2	D1	D0
00	CTL0	DVS SLEW RATE		FREQUENCY		N/A	PWRON_DEBOUNCE_TIMER		N/A
01	CTL1	RSTO_MODE		RSTO_DELAY		RSTO_PFI_THLD		N/A	
02	CTL2	N/A				TIME_SLOT		PWR_ON_TIME_SLOT_MODE	PWR_OFF_TIME_SLOT_MODE
03	Buck 1	BUCK1_VREF: 0.4V to 3.5875V/12.5mV step or 0.4V to 2.2V/7.4mV step							
04		N/A	OVPEN1	DISCHGEN1	MODE BUCK1	N/A			
05		ILIM1		PHASE_DELAY1		SOFTSTART1		N/A	
06		POWER_OFF_SLOT_NO_B1				POWER_ON_SLOT_NO_B1			
07	Buck 2	BUCK2_VREF: 0.4V to 3.5875V/12.5mV step or 0.4V to 2.2V/7.4mV step							
08		N/A	OVPEN2	DISCHGEN2	MODE BUCK2	N/A			
09		ILIM2		PHASE_DELAY2		SOFTSTART2		N/A	
0A		POWER_OFF_SLOT_NO_B2				POWER_ON_SLOT_NO_B2			
0B	Buck 3	BUCK3_VREF: 0.65V to 3.5875V/12.5mV step or 0.4V to 2.2V/7.4mV step							
0C		N/A	OVPEN3	DISCHGEN3	MODE BUCK3	N/A			
0D		ILIM3		PHASE_DELAY3		SOFTSTART3		N/A	
0E		POWER_OFF_SLOT_NO_B3				POWER_ON_SLOT_NO_B3			
0F	Buck 4	BUCK4_VREF: 0.4V to 3.5875V/12.5mV step							
10		N/A	OVPEN4	DISCHGEN4	MODE BUCK4	N/A			
11		ILIM4		PHASE_DELAY4		SOFTSTART4		N/A	
12		POWER_OFF_SLOT_NO_B4				POWER_ON_SLOT_NO_B4			
13	CTL3	N/A		EN1_SELECT	EN_OFF_DELAY	EN_OFF_MODE	BUCK3_VID	BUCK2_VID	BUCK1_VID
14	LDO 2	LDO2_VREF: 0.65V to 3.5875V/12.5mV step							
15		N/A	N/A	DISCHGEN_LDO2	I2C_SLAVE_ADDRESS				
16		POWER_OFF_SLOT_NO_LDO2				POWER_ON_SLOT_NO_LDO2			
17	LOAD_SW	N/A							
18		N/A	N/A	DISCHGEN_LDSW	N/A	N/A			
19		POWER_OFF_SLOT_NO_LDSW				POWER_ON_SLOT_NO_LDSW			
1A	LDO 4	LDO4_VREF: 0.65V to 3.5875V/12.5mV step							
1B		N/A	ILIM_LDO4	DISCHGEN_LDO4	N/A	N/A			
1C		POWER_OFF_SLOT_NO_LDO4				POWER_ON_SLOT_NO_LDO4			
1D	LDO 5	LDO5_VREF: 0.65V to 3.5875V/12.5mV step							
1E		N/A	ILIM_LDO5	DISCHGEN_LDO5	N/A	N/A			
1F		POWER_OFF_SLOT_NO_LDO5				POWER_ON_SLOT_NO_LDO5			
20	Mode	PARALLEL_1	PARALLEL_2	PWRON_MODE	EN_EN1_PIN	N/A	N/A		
21	EN1	EN1_INV	EN1_POWER_RAILS_CONTROL						
22	EN	EN_BUCK1	EN_BUCK2	EN_BUCK3	EN_BUCK4	EN_LDO2	EN_LDSW	EN_LDO4	EN_LDO5
23	ID1	MTP configure code ("0x00" for standard MP5424-0000, "0x01" for MP5424-0001)							
24	ID2	MTP revision number (MTP revision number is stored here in case the user has to update the MTP)							
25	CRC	Checksum of MTP registers 0x00 to 0x24. While writing the I²C register data to the MTP, the PMIC initiates a checksum of all the related I²C registers and writes the result in this byte. During start-up, the PMIC calculates and compares the MTP data with the 0x25 register's content. If they match, the MTP data is loaded to the I²C register; otherwise, the I²C register ignores the MTP data and uses the default setting.							

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MTP E-Fuse Description

Name	Bits	Default	Description
DVS SLEW RATE	D[7:6]	10	Voltage scaling slew rate for the buck 1, buck 2, buck 3, and buck 4 converters. The soft-start slew rate is set by the SOFTSTART bits. 00: Reserved 01: Reserved 10: 8mV/µs 11: 4mV/µs
FREQUENCY	D[5:4]	00	Switching frequency (f_{SW}) setting bit. 00: 1.1MHz 01: 1.65MHz 10: 2.2MHz 11: 2.75MHz
PWRON_DEBOUNCE_TIMER	D[2:1]	01	Sets the PWRON pin's debounce timer. It is valid only if PWRON_MODE is set to 1. See the PWRON_MODE = 1 (Edge Trigger) section on page 21 for more information. The debounce time is not related to default f_{SW}. 00: 0.5ms 01: 10ms 10: 40ms 11: 160ms
RSTO_MODE	D[7:6]	00	Sets the RSTO behavior. 00: Does not monitor any power rails. If the PMIC enters the shutdown sequence or V_{IN1} drops below its under-voltage lockout (UVLO) threshold, then RSTO goes low. RSTO goes high once the RSTO delay (t_{RSTO}) is complete 01: Monitors buck 4's power good (PG). If buck 4's PG (PG4) is good after t_{RSTO}, RSTO goes high . If buck 4 is turned off by the I²C, then PG4 is high. If PG4 goes low, then there is no t_{RSTO} 10: Monitors V_{IN1} (see the RSTO_PFI_THLD register). RSTO goes high if V_{IN1} > V_{IN1} UVLO threshold. RSTO goes low if V_{IN1} < V_{IN1} UVLO threshold. RSTO goes high after t_{RSTO}. RSTO goes low with no delay. If V_{IN1} > V_{IN1} UVLO threshold and PWRON is active, then RSTO monitors V_{IN1} while the PMIC is on 11: Monitors all enabled buck and LDO power rails. If the enabled bucks' PG and LDOs' PG are good, then RSTO goes high after t_{RSTO}. If any PG goes low, RSTO goes low without a delay.
RSTO_DELAY	D[5:4]	01	Sets t_{RSTO} before RSTO goes high. t_{RSTO} is not related to the default f_{SW}. 00: 100ms 01: 50ms 10: 10ms 11: 1ms
RSTO_PFI_THLD	D[3:2]	10	Sets the V_{IN1} UVLO rising threshold when RSTO_MODE is set to 10. 00: 2.7V 01: 2.9V 10: 4V 11: 4.4V
TIME_SLOT	D[3:2]	00	Sets the start-up/shutdown sequence time slot intervals. The start-up/shutdown sequences share the same time slot value. The time slot value is not related to the default f_{SW}. 00: 0.5ms 01: 2ms 10: 8ms 11: 16ms

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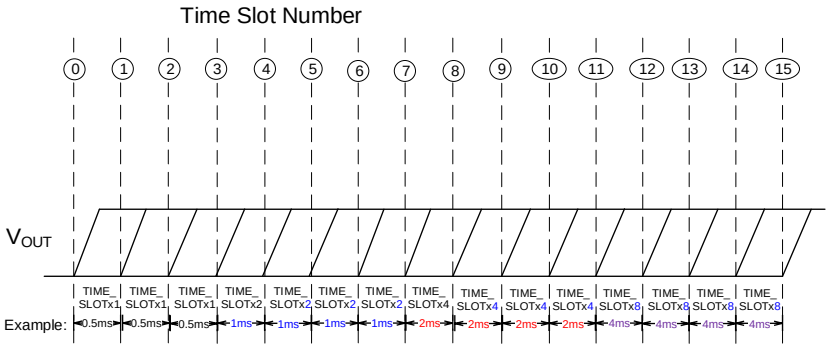
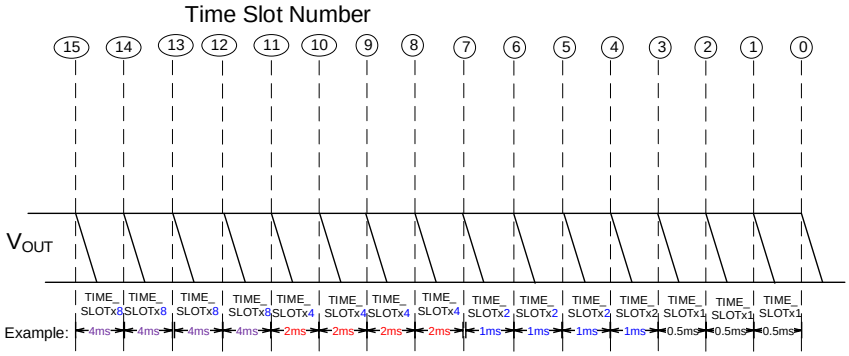
Name	Bits	Default	Description
PWR_ON_ TIME_SLOT_ MODE	D[1]	0	Selects the start-up sequence time slot mode. 0: The time slot is a fixed number set by TIME_SLOT 1: The time slot increases linearly, as shown below: • Time slot 0 to slot 3 has a TIME_SLOT x 1 interval • Time slot 3 to slot 7 has a TIME_SLOT x 2 interval • Time slot 7 to slot 11 has a TIME_SLOT x 4 interval • Time slot 11 to slot 15 has a TIME_SLOT x 8 interval  In a standard application, the start-up sequence ends at the maximum time slot of enabled channels. For example, if time slot 7 is the maximum slot number of the enabled channels (i.e. slot numbers above 7 are not used) during the start-up sequence, then the counter only works until time slot 7. The start-up sequence is complete, and the higher time slots are not executed.
PWR_OFF_ TIME_SLOT_ MODE	D[0]	0	Selects the shutdown sequence time slot mode. 0: The time slot is a fixed number set by TIME_SLOT 1: The time slot increases linearly, as shown below: • Time slot 0 to slot 3 has a TIME_SLOT x 1 interval • Time slot 3 to slot 7 has a TIME_SLOT x 2 interval • Time slot 7 to slot 11 has a TIME_SLOT x 4 interval • Time slot 11 to slot 15 has a TIME_SLOT x 8 interval  If the EN_OFF_DELAY is disabled, then the shutdown sequence begins at the maximum time slot of the enabled channels. For example, if time slot 7 is the maximum slot number of the enabled channels (i.e. slot numbers above 7 are not used) during the shutdown sequence, then the counter only works from time slot 7 to time slot 0. The shutdown sequence is complete, and the higher time slots are not executed. If the EN_OFF_DELAY is enabled, then the shutdown sequence starts from the 60th time interval, and the power rail turns off once the time interval decreases to the power rail's time slot. The shutdown delay of each power rail is determined by the TIME_SLOT, PWR_OFF_TIME_SLOT_MODE and the time slot number.

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Name	Bits	Default	Description
BUCK1_VREF, BUCK2_VREF, BUCK3_VREF, BUCK4_VREF, LDO2_VREF, LDO4_VREF, LDO5_VREF	D[7:0]	00110100, 00110011, 00110100, 01001100, 01110000, 11101000, 11101000	Sets the internal reference voltage (V_{REF}). Buck outputs are between 400mV and 3587.5mV with 12.5mV per step. LDO outputs are from 650mV to 3587.5mV with 12.5mV per step. See Table 1 on page 32 for more details. 0000 0000: 400mV 0000 0001: 412.5mV ... 1111 1111: 3587.5mV If the Buck1_VID, Buck2_VID, and Buck3_VID bits are set to 1, then the buck 1, buck 2, and buck 3 V_{OUT} range is between 400mV and 2.2V with a 7.4mV per step.
OVPEN1, OVPEN2, OVPEN3, OVPEN4	D[6]	1	Enable bit for buck 1, buck 2, buck 3, and buck 4 output over-voltage protection (OVP). 0: OVP disabled 1: OVP enabled
DISCHGEN1, DISCHGEN2, DISCHGEN3, DISCHGEN4	D[5]	1	Enable bit for buck 1, buck 2, buck 3, and buck 4 output discharge function. 0: Discharge function disabled 1: Discharge function enabled
MODEBUCK1, MODEBUCK2, MODEBUCK3, MODEBUCK4	D[4]	1	Selects auto-PFM/PWM mode or forced pulse-width modulation (FPWM) mode. 0: Auto-PFM/PWM mode 1: Forced PWM mode (FPWM)
ILIM1, ILIM3	D[7:6]	10	Configures the high-side MOSFET (HS-FET) peak current limit (I_{LIMIT_PEAK}) for buck 1 and buck 3. 00: 4.6A typical HS-FET I_{LIMIT_PEAK} 01: 6.6A typical HS-FET I_{LIMIT_PEAK} 10: 7.6A typical HS-FET I_{LIMIT_PEAK} 11: 9.3A typical HS-FET I_{LIMIT_PEAK}
ILIM2, ILIM4	D[7:6]	01	Configures the HS-FET I_{LIMIT_PEAK} for buck 2 and buck 4. 00: 2.7A typical HS-FET I_{LIMIT_PEAK} 01: 3.9A typical HS-FET I_{LIMIT_PEAK} 10: 5.1A typical HS-FET I_{LIMIT_PEAK} 11: 6.1A typical HS-FET I_{LIMIT_PEAK}
PHASE_ DELAY1, PHASE_ DELAY2, PHASE_ DELAY3, PHASE_ DELAY4	D[5:4]	00, 01, 01, 00	Sets the phase delay for buck 1, buck 2, buck 3, and buck 4. 00: 0° delay 01: 90° delay 10: 180° delay 11: 270° delay
SOFTSTART1, SOFTSTART2, SOFTSTART3, SOFTSTART4	D[3:2]	01	Soft-start time (t_{SS}) setting bit for buck 1, buck 2, buck 3, and buck 4. t_{SS} is between 10% and 90% of the target V_{OUT}. 00 :150µs 01: 300µs 10: 610µs 11: 920µs

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Name	Bits	Default	Description
POWER_OFF_SLOT_NO_B1, POWER_OFF_SLOT_NO_B2, POWER_OFF_SLOT_NO_B3, POWER_OFF_SLOT_NO_B4, POWER_OFF_SLOT_NO_LDO2, POWER_OFF_SLOT_NO_LDSW, POWER_OFF_SLOT_NO_LDO4, POWER_OFF_SLOT_NO_LDO5	D[7:4]	0011, 0010, 0011, 0001, 0000, 0100 1010 1011	This bit sets each power rail's time slot number during the shutdown sequence. See the TIME_SLOT register on page 28 and the PWR_OFF_TIME_SLOT_MODE register on page 29 for more details. The delay times between neighboring slots are not related to default f_{SW}. 0000: Time slot 0 0001: Time slot 1 0010: Time slot 2 0011: Time slot 3 0100: Time slot 4 0101: Time slot 5 0110: Time slot 6 0111: Time slot 7 1000: Time slot 8 1001: Time slot 9 1010: Time slot 10 1011: Time slot 11 1100: Time slot 12 1101: Time slot 13 1110: Time slot 14 1111: Time slot 15
POWER_ON_SLOT_NO_B1, POWER_ON_SLOT_NO_B2, POWER_ON_SLOT_NO_B3, POWER_ON_SLOT_NO_B4, POWER_ON_SLOT_NO_LDO2, POWER_ON_SLOT_NO_LDSW, POWER_ON_SLOT_NO_LDO4, POWER_ON_SLOT_NO_LDO5	D[3:0]	0011, 0010, 0011, 0001, 0000, 0100101 0 1011	This bit sets each power rail's time slot number during the start-up sequence (see the TIME_SLOT register on page 28 and the PWR_ON_TIME_SLOT_MODE register on page 29 for more details). The delay times between neighboring slots are not related to the default f_{SW}. 0000: Time slot 0 0001: Time slot 1 0010: Time slot 2 0011: Time slot 3 0100: Time slot 4 0101: Time slot 5 0110: Time slot 6 0111: Time slot 7 1000: Time slot 8 1001: Time slot 9 1010: Time slot 10 1011: Time slot 11 1100: Time slot 12 1101: Time slot 13 1110: Time slot 14 1111: Time slot 15
DISCHGEN_LDO2, DISCHGEN_LDO4, DISCHGEN_LDO5	D[5]	1	Enable bit for the LDO2, LDO4 and LDO5 output discharge function. 0: Discharge function disabled 1: Discharge function enabled
BUCK1_VID, BUCK2_VID, BUCK3_VID	D[2:0]	000	Sets the buck 1, buck 2, and buck 3 V_{OUT} range and resolution. 0: V_{OUT} is 400mV to 3.5875V with 12.5mV per step 1: V_{OUT} range is 400mV to 2.2V with 7.4mV per step
EN1_SELECT	D[5]	0	Selects LSWO or LDO 2 as the EN1 pin. If the EN1 function is enabled, then the corresponding load switch or LDO 2 channel and its discharge function should be turned off. 0: Selects LSWO as EN1 pin 1: Selects LDO2 as EN1 pin

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Name	Bits	Default	Description
EN_OFF_ DELAY	D[4]	0	Enables the shutdown delay. This bit is only active if EN_OFF_MODE = 0. 0: Shutdown delay disabled. The shutdown sequence begins at the largest time slot of the enabled channel 1: Enable shutdown delay. The shutdown sequence begins at the 60th time interval, the power rail turns off once the time interval decreases to the power rail's time interval. The time interval of each power rail is determined by TIME_SLOT, PWR_OFF_TIME_SLOT_MODE, and the time slot number
EN_OFF_ MODE	D[3]	0	Sets the shutdown sequence behavior controlled by the PWRON pin. There is always a shutdown sequence while controlled by EN1. 0: Shutdown sequence 1: No shutdown sequence. All power rails turn off at the same time
DISCHGEN_ LDSW	D[5]	1	Enable bit for the load switch output discharge function. 0: Discharge function disabled 1: Discharge function enabled
I2C_SLAVE_ ADDRESS	D[4:0]	01001	Sets the A5 to A1 bit of the slave I²C address. See the I²C Bus Slave Address section on page 34 for more details.
ILIM_LDO4, ILIM_LDO5	D[6]	0	Selects the LDO 4 and LDO 5 current limit (I_{LIMIT}). 0: Lower I_{LIMIT} supports 300mA I_{OUT} 1: Higher I_{LIMIT} supports 550mA I_{OUT}
PARALLEL_1	D[7]	0	Sets whether buck 1 and buck 3 operate in parallel. Use FB1 as the feedback pin. After the buck converters enter parallel mode, buck 3's I²C/MTP register is invalid. Parallel mode takes effect during a start-up through VIN. After start-up, the PMIC does not respond to changes on this bit. I_{LIMIT} is doubled based on buck 1's register setting. 0: Buck 1 and buck 3 do not operate in parallel 1: Buck 1 and buck 3 operate in parallel
PARALLEL_2	D[6]	0	Sets whether buck 2 and buck 4 operate in parallel mode. Use FB2 as the feedback pin. After the buck converters enter parallel mode, buck 4's I²C/MTP register is invalid. Parallel mode takes effect during a start-up through VIN. After start-up, the PMIC does not respond to changes on this bit. I_{LIMIT} is doubled based on buck 2's register setting. 0: Buck 2 and buck 4 do not operate in parallel 1: Buck 2 and buck 4 operate in parallel
PWRON_ MODE	D[5]	0	This bit defines the PWRON pin's behavior (level trigger or falling-edge trigger). 0: Level trigger. This functions as an EN pin. If the PWRON pin's V_{IN} exceeds the rising threshold, then the PMIC begins the start-up sequence 1: Falling-edge trigger. If the PWRON pin detects a high to low transition and the PMIC is off, then the PMIC begins the start-up sequence after a delay. If the PMIC is on, then the PMIC begins the shutdown sequence after a delay. The delay time is set by PWRON_DEBOUNCE_TIMER
EN_EN1_PIN	D[4]	0	Enable bit of EN1 function. EN1_POWER_RAILS_CONTROL defines which power rails are controlled by the EN1 pin. EN1_INV defines EN1 active low or active high. EN_SELECT defines LSWO or LDO 2 as EN1. 0: EN1 function disabled 1: EN1 function enabled
EN1_INV	D[7]	1	Sets EN1 to active low or active high. 0: A low-level input to EN1 turns on the corresponding power rails 1: A high-level input to EN1 turns on the corresponding power rails

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<table>
<tr><th>Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>EN1_POWER_RAILS_CONTROL</td><td>D[6:0]</td><td>0000111</td><td>This bit sets which power rails are controlled by EN1. Each bit controls 1 power rail from D[6] to D[0].
<table><tr><th>D[6]</th><th>D[5]</th><th>D[4]</th><th>D[3]</th><th>D[2]</th><th>D[1]</th><th>D[0]</th></tr><tr><td>Buck 1</td><td>Buck 2</td><td>Buck 3</td><td>Buck 4</td><td>LDSW</td><td>LDO 4</td><td>LDO 5</td></tr></table>0: EN1 does not control the power rail’s start-up/shutdown sequence
1: EN1 controls this power rail’s start-up/shutdown sequence
If the EN1 function is enabled, the corresponding load switch or LDO 2 channel and its discharge function should be turned off. Note that EN1 cannot control LDO 2. LDO 2 can only be controlled by PWRON</td></tr>
<tr><td>EN_BUCK1, EN_BUCK2, EN_BUCK3, EN_BUCK4, EN_LDO2, EN_LDSW, EN_LDO4, EN_LDO5</td><td>D[7:0]</td><td>0xFF</td><td>Enable control bit for each power rail.
0: Disabled
1: Enabled</td></tr>
</table>

Table 1: Output Reference Voltage Chart (BUCK1_VID = 0, Buck2_VID = 0, Buck3_VID = 0)

D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)
00000000	400	01010110	1475	10101100	2550
00000001	412.5	01010111	1487.5	10101101	2562.5
00000010	425	01011000	1500	10101110	2575
00000011	437.5	01011001	1512.5	10101111	2587.5
00000100	450	01011010	1525	10110000	2600
00000101	462.5	01011011	1537.5	10110001	2612.5
00000110	475	01011100	1550	10110010	2625
00000111	487.5	01011101	1562.5	10110011	2637.5
00001000	500	01011110	1575	10110100	2650
00001001	512.5	01011111	1587.5	10110101	2662.5
00001010	525	01100000	1600	10110110	2675
00001011	537.5	01100001	1612.5	10110111	2687.5
00001100	550	01100010	1625	10111000	2700
00001101	562.5	01100011	1637.5	10111001	2712.5
00001110	575	01100100	1650	10111010	2725
00001111	587.5	01100101	1662.5	10111011	2737.5
00010000	600	01100110	1675	10111100	2750
00010001	612.5	01100111	1687.5	10111101	2762.5
00010010	625	01101000	1700	10111110	2775
00010011	637.5	01101001	1712.5	10111111	2787.5
00010100	650	01101010	1725	11000000	2800
00010101	662.5	01101011	1737.5	11000001	2812.5
00010110	675	01101100	1750	11000010	2825
00010111	687.5	01101101	1762.5	11000011	2837.5

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D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)
00011000	700	01101110	1775	11000100	2850
00011001	712.5	01101111	1787.5	11000101	2862.5
00011010	725	01110000	1800	11000110	2875
00011011	737.5	01110001	1812.5	11000111	2887.5
00011100	750	01110010	1825	11001000	2900
00011101	762.5	01110011	1837.5	11001001	2912.5
00011110	775	01110100	1850	11001010	2925
00011111	787.5	01110101	1862.5	11001011	2937.5
00100000	800	01110110	1875	11001100	2950
00100001	812.5	01110111	1887.5	11001101	2962.5
00100010	825	01111000	1900	11001110	2975
00100011	837.5	01111001	1912.5	11001111	2987.5
00100100	850	01111010	1925	11010000	3000
00100101	862.5	01111011	1937.5	11010001	3012.5
00100110	875	01111100	1950	11010010	3025
00100111	887.5	01111101	1962.5	11010011	3037.5
00101000	900	01111110	1975	11010100	3050
00101001	912.5	01111111	1987.5	11010101	3062.5
00101010	925	10000000	2000	11010110	3075
00101011	937.5	10000001	2012.5	11010111	3087.5
00101100	950	10000010	2025	11011000	3100
00101101	962.5	10000011	2037.5	11011001	3112.5
00101110	975	10000100	2050	11011010	3125
00101111	987.5	10000101	2062.5	11011011	3137.5
00110000	1000	10000110	2075	11011100	3150
00110001	1012.5	10000111	2087.5	11011101	3162.5
00110010	1025	10001000	2100	11011110	3175
00110011	1037.5	10001001	2112.5	11011111	3187.5
00110100	1050	10001010	2125	11100000	3200
00110101	1062.5	10001011	2137.5	11100001	3212.5
00110110	1075	10001100	2150	11100010	3225
00110111	1087.5	10001101	2162.5	11100011	3237.5
00111000	1100	10001110	2175	11100100	3250
00111001	1112.5	10001111	2187.5	11100101	3262.5
00111010	1125	10010000	2200	11100110	3275
00111011	1137.5	10010001	2212.5	11100111	3287.5
00111100	1150	10010010	2225	11101000	3300
00111101	1162.5	10010011	2237.5	11101001	3312.5
00111110	1175	10010100	2250	11101010	3325

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D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)
00111111	1187.5	10010101	2262.5	11101011	3337.5
01000000	1200	10010110	2275	11101100	3350
01000001	1212.5	10010111	2287.5	11101101	3362.5
01000010	1225	10011000	2300	11101110	3375
01000011	1237.5	10011001	2312.5	11101111	3387.5
01000100	1250	10011010	2325	11110000	3400
01000101	1262.5	10011011	2337.5	11110001	3412.5
01000110	1275	10011100	2350	11110010	3425
01000111	1287.5	10011101	2362.5	11110011	3437.5
01001000	1300	10011110	2375	11110100	3450
01001001	1312.5	10011111	2387.5	11110101	3462.5
01001010	1325	10100000	2400	11110110	3475
01001011	1337.5	10100001	2412.5	11110111	3487.5
01001100	1350	10100010	2425	11111000	3500
01001101	1362.5	10100011	2437.5	11111001	3512.5
01001110	1375	10100100	2450	11111010	3525
01001111	1387.5	10100101	2462.5	11111011	3537.5
01010000	1400	10100110	2475	11111100	3550
01010001	1412.5	10100111	2487.5	11111101	3562.5
01010010	1425	10101000	2500	11111110	3575
01010011	1437.5	10101001	2512.5	11111111	3587.5
01010100	1450	10101010	2525		
01010101	1462.5	10101011	2537.5		

I²C Bus Slave Address

The slave address is a 7-bit address followed by an 8th read or write (R/W) data direction bit. The A5, A4, A3, A2, and A1 bits can be configured via the MTP e-fuse.

	A7	A6	A5	A4	A3	A2	A1
Setting Value	1	1	0 (15)	1 (15)	0 (15)	0 (15)	1 (15)

Notes:

15) This bit is configurable via the MTP e-fuse.
16) The slave address is 0x69 (A[7:1] = 1101 001) by default.

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I²C REGISTER MAP

Add (hex)	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	CTL0	R/W	DVS SLEW RATE		FREQUENCY		Reserved (18)	PWRON_DEBOUNCE_TIMER		Reserved
01	CTL1	R/W	RSTO_MODE		RSTO_DELAY		RSTO_PFI_THLD		Reserved	
02	CTL2	R/W	Reserved		Reserved		TIME_SLOT		PWR_ON_TIME_SLOT_MODE	PWR_OFF_TIME_SLOT_MODE
03	Buck 1	R/W	BUCK1_VREF: 0.4V to 3.5875V/12.5mV step or 0.4V to 2.2V/7.4mV step							
04		R/W	Reserved	OVPEN1	DISCHGEN1	MODEBUCK1	Reserved			
05		R/W	ILIM1		PHASE_DELAY1		SOFTSTART1		Reserved	
06		R/W	POWER_OFF_SLOT_NO_B1				POWER_ON_SLOT_NO_B1			
07	Buck 2	R/W	BUCK2_VREF: 0.4V to 3.5875V/12.5mV step or 0.4V to 2.2V/7.4mV step							
08		R/W	Reserved	OVPEN2	DISCHGEN2	MODEBUCK2	RESERVED			
09		R/W	ILIM2		PHASE_DELAY2		SOFTSTART2		Reserved	
0A		R/W	POWER_OFF_SLOT_NO_B2				POWER_ON_SLOT_NO_B2			
0B	Buck 3	R/W	BUCK3_VREF: 0.4V to 3.5875V/12.5mV step or 0.4V to 2.2V/7.4mV step							
0C		R/W	Reserved	OVPEN3	DISCHGEN3	MODEBUCK3	Reserved			
0D		R/W	ILIM3		PHASE_DELAY3		SOFTSTART3		Reserved	
0E		R/W	POWER_OFF_SLOT_NO_B3				POWER_ON_SLOT_NO_B3			
0F	Buck 4	R/W	BUCK4_VREF: 0.4V to 3.5875V/12.5mV step							
10		R/W	RESERVED	OVPEN4	DISCHGEN4	MODEBUCK4	Reserved			
11		R/W	ILIM4		PHASE_DELAY4		SOFTSTART4		RESERVED	
12		R/W	POWER_OFF_SLOT_NO_B4				POWER_ON_SLOT_NO_B4			
13	CTL3	R/W	RESERVED		EN1_SELECT	EN_OFF_DELAY	EN_OFF_MODE	BUCK3_VID	BUCK2_VID	BUCK1_VID
14	LDO 2	R/W	LDO2_VREF: 0.65V to 3.5875V/12.5mV step							
15		R/W	Reserved	Reserved	DISCHGEN_LDO2	I2C_SLAVE_ADDRESS				
16		R/W	POWER_OFF_SLOT_NO_LDO2				POWER_ON_SLOT_NO_LDO2			
17	LOAD_SW	R/W	Reserved							
18		R/W	Reserved	Reserved	DISCHGEN_LDSW	Reserved	Reserved			
19		R/W	POWER_OFF_SLOT_NO_LDSW				POWER_ON_SLOT_NO_LDSW			
1A	LDO 4	R/W	LDO4_VREF: 0.65V to 3.5875V/12.5mV step							
1B		R/W	Reserved	ILIM_LDO4	DISCHGEN_LDO4	Reserved	Reserved			
1C		R/W	POWER_OFF_SLOT_NO_LDO4				POWER_ON_SLOT_NO_LDO4			
1D	LDO 5	R/W	LDO5_VREF: 0.65V to 3.5875V/12.5mV step							
1E		R/W	Reserved	ILIM_LDO5	DISCHGEN_LDO5	Reserved	RESERVED			
1F		R/W	POWER_OFF_SLOT_NO_LDO5				POWER_ON_SLOT_NO_LDO5			
20	Parallel Mode	R/W	PARALLEL_1 (17)	PARALLEL_2 (17)	PWRON_MODE (17)	EN_EN1_PIN (17)	RESERVED			
21	Standby 1	R/W	EN1_INV (17)	EN1_POWER_RAILS_CONTROL(17)						
22	EN	R/W	EN_BUCK1	EN_BUCK2	EN_BUCK3	EN_BUCK4	EN_LDO2	EN_LDSW	EN_LDO4	EN_LDO5
23	MTP_CTL	R/W	MTP configure code ("0x00" for standard MP5424-0000, "0x01" for MP5424-0001)							
24		R/W	MTP revision number (MTP revision number is stored here, in case the user must update the MTP)							
25		R/W	ENTER_MTP_MODE	PROGRAM_MTP (18)	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
26		W	MTP Program Password							
27	Status 1	R	PGLDO4	Reserved "1"	PGLDO2	Reserved "1"	PGBUCK4	PG BUCK3	PGBUCK2	PGBUCK1
28	Status 2	R	OTWARNING	OTEMPP	Reserved	CHECKSUM FLAG	Reserved	Reserved	Reserved	Reserved
29	ID2	R	VENDOR ID				Reserved	PGLDO5	CURRENT MTP PAGE INDEX	

Notes:

17) The I²C bits do not control the real circuitry. Only the MTP bits control those functions. The MTP value only reloads the circuitry when the PWRON pin turns off, the MTP is configured, or AVIN > UVLO threshold.

18) Reserved bits must be written to 0.

Register Description

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Most of the register bits share the same description as the MTP e-fuse configuration table on page 26. Table 2 shows the descriptions of the I²C register bits that are different from the MTP register bits.

The I²C register's default values are determined by the MTP table.

The I²C register can be reset to the hard-coded default values under two conditions:

1. There is a CRC error while loading the MTP.
2. The MTP page is set to 0.

Thermal shutdown does not reset the I²C register.

Table 2: I²C Register Descriptions

Name	Bits	Default	Description
ENTER_MTP_MODE	D[7]	0	Set ENTER_MTP_MODE to 1 to enter pre-MTP configure mode. After MTP configuration is complete, ENTER_MTP_MODE resets automatically to 0.
PROGRAM_MTP	D[6]	0	If PROGRAM_MTP is set 1, then the PMIC executes an MTP configure action . After MTP configuration is complete, PROGRAM_MTP resets automatically to 0.
PGx	D[X]	0	PG indicator for the buck converters and LDOs. If V_{OUT} exceeds 90% of the V_{REF}, then PGx = 1. If V_{OUT} drops below 80% of V_{REF}, then PGx = 0. During I²C-controlled dynamic voltage scaling, the PG deglitch timer blanks the possible PG glitch. These PG bits change dynamically to indicate the power good of each buck's and each LDO's status.
OTWARNING	D[7]	0	Die temperature early warning bit. If OTWARNING is high, this indicates that the die temperature has exceeded 120°C. OTWARNING latches once it is triggered. Write 1 to OTWARNING to clear it.
OTEMPP	D[6]	0	Over-temperature (OT) indicator. If OTEMPP is high, this indicates that thermal shutdown has been triggered. OTEMPP latches once it is triggered. Write 1 to OTEMPP to clear it.
VENDOR ID	D[7:4]	1000	Vendor identification.
CHECKSUM FLAG	D[4]	0	1: The current MTP page has a CRC or checksum error 0: The current MTP data passes the CRC test
CURRENT MTP PAGE INDEX	D[1:0]	00	CURRENT MTP PAGE INDEX stores the current MTP page index information. The IC cannot access the MTP while D[1:0] = 10b. The MP5424 MTP can only be configured two times. 00: Default page; two other pages can be used 01: First page 10: Second page 11: Reserved

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APPLICATION INFORMATION

Selecting the Inductor

MPL Optimized Performance with MPS Inductor MPL-AL6050 Series

For most applications, use a 0.47µH to 2.2µH inductor with a DC current rating at least 25% greater than the maximum load current (I_{LOAD_MAX}). For improved efficiency, use an inductor with a DC resistance below 15mΩ. For most designs, the inductance (L_1) can be calculated with Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of I_{LOAD_MAX}. The maximum inductor peak current ($I_{L(MAX)}$) can be estimated with Equation (2):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Choose an inductor with a higher inductance to improve efficiency under light-load conditions (<100mA).

MPS inductors are optimized and tested for use with our complete line of integrated circuits. Table 3 lists MPS's power inductor recommendations for use with the MP5424. Select a part number based on your design requirements.

Table 3: Power Inductor Selection

Part Number	Inductance	Manufacturer
Select family series (MPL-AL)	1µH to 1.5µH	MPS
MPL-AL6050-1R0	1µH	MPS
MPL-AL6050-1R5	1.5µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Step-Down Converter Input Capacitor (C1)

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply the AC current to the converter while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C1 (I_{C1}) can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, which can be estimated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose C1 to have an RMS current rating greater than half of I_{LOAD_MAX}.

C1 can be electrolytic, tantalum, or ceramic. If using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (0.1µF) placed as close to the IC as possible. If using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Step-Down Converter Output Capacitor (C2)

The output capacitor (C2) for the step-down converter maintains the DC V_{OUT}. C2 can be ceramic, tantalum, or electrolytic. For the best results, use low-ESR capacitors to keep the output voltage ripple (ΔV_{OUT}) low. For most applications, two 22µF ceramic capacitors are sufficient .

ΔV_{OUT} can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (6)$$

Where R_{ESR} is the equivalent series resistance (ESR) value of C2.

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For ceramic capacitors, the capacitance dominates the impedance at f_{SW}, and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}.

For simplification, ΔV_{OUT} be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

The characteristics of C2 also affect the system stability.

Table 4 lists the recommended components for MP5424.

Table 4: Recommended External Components for DC/DC Converters and LDOs

Component	Value	Notes
VIN1 input capacitor (C_{IN})	22μF	0805 size/10V ceramic capacitor
VIN2 C_{IN}	22μF	0805 size/10V ceramic capacitor
VIN3 C_{IN}	22μF	0805 size/10V ceramic capacitor
VIN4 C_{IN}	22μF	0805 size/10V ceramic capacitor
VIN5 C_{IN}	10μF	0805 size/10V ceramic capacitor
AVIN C_{IN}	0.1μF	0603 size/10V ceramic capacitor
Buck 1 output capacitor (C_{OUT})	22μF x 2	0805 size/10V ceramic capacitor
Buck 1 inductor	1μH	I_{SAT} > current limit
Buck 2 C_{OUT}	22μF x 2	0805 size/10V ceramic capacitor
Buck 2 inductor	1.5μH	I_{SAT} > current limit
Buck 3 C_{OUT}	22μF x 2	0805 size/10V ceramic capacitor
Buck 3 inductor	1μH	I_{SAT} > current limit
Buck 4 C_{OUT}	22μF x 2	0805 size/10V ceramic capacitor
Buck 4 inductor	1.5μH	I_{SAT} > current limit
LSWI C_{IN}	10μF	0603 size/6.3V ceramic capacitor
LDO 2 C_{OUT}	2.2μF	0603 size/6.3V ceramic capacitor
LSWO C_{OUT}	10μF	0603 size/6.3V ceramic capacitor
LDO 4 C_{OUT}	2.2μF	0603 size/6.3V ceramic capacitor
LDO 5 C_{OUT}	2.2μF	0603 size/6.3V ceramic capacitor
RSTO pull-up resistor	100kΩ	0603 or 0402 size film resistor
AVIN series resistor to VIN1 RSTO pull-up resistor	4.7Ω	0603 or 0402 size film resistor

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PCB Layout Guidelines [19]

Efficient PCB layout is critical for stable operation. It is recommended to use a 4-layer board for improved performance. For the best results, refer to Figure 17 and follow the guidelines below:

1. Connect the input ground to the GNDx pin using short and wide traces.
2. Connect the input capacitor to the VINx pin using short and wide traces.
3. Ensure FB1, FB2, FB3, and FB4 are Kelvin-connected to the buck 1, buck 2, buck 3, and buck 4 output capacitors. Do not connect FB directly to the inductor's output node.
4. Route SW away from sensitive analog areas, such as FB1, FB2, FB3, and FB4.

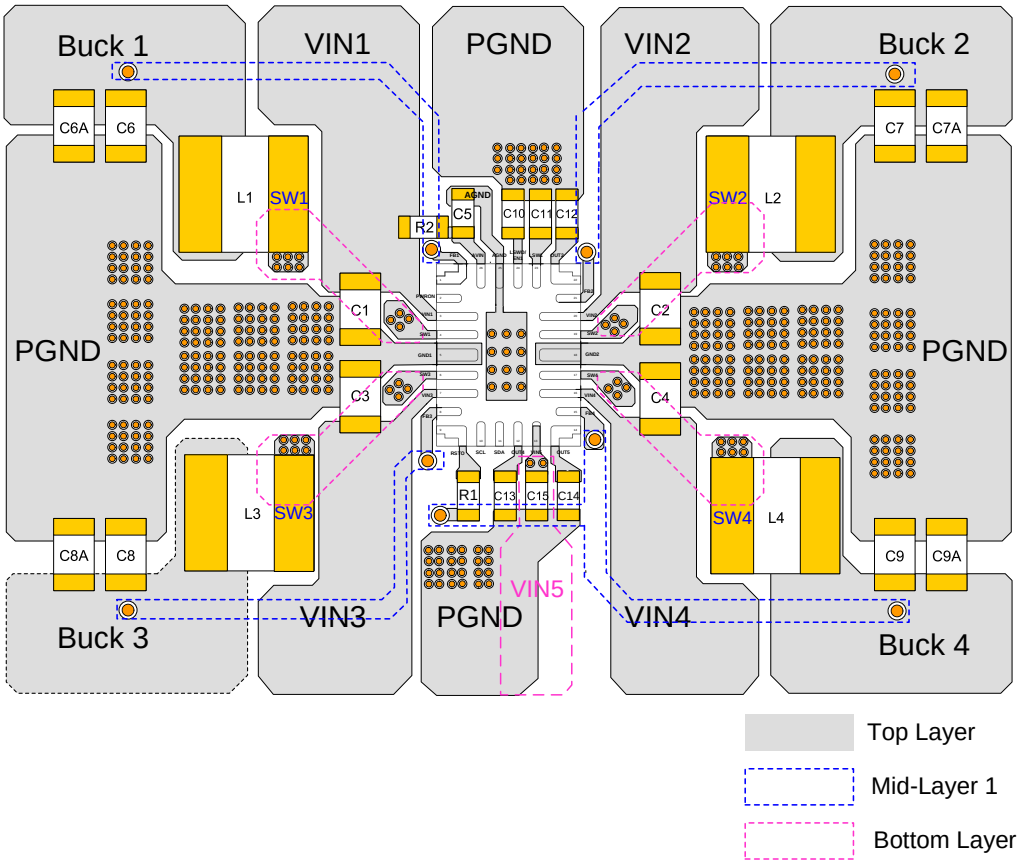

Figure 17: Recommended PCB Layout [20]

Notes:

19) The recommended PCB layout is based on Figure 18 on page 40.
20) It is recommended to separate buck 1's PGND and buck 3's PGND from buck 2's PGND and buck 4's PGND on the top layer.

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TYPICAL APPLICATION CIRCUITS

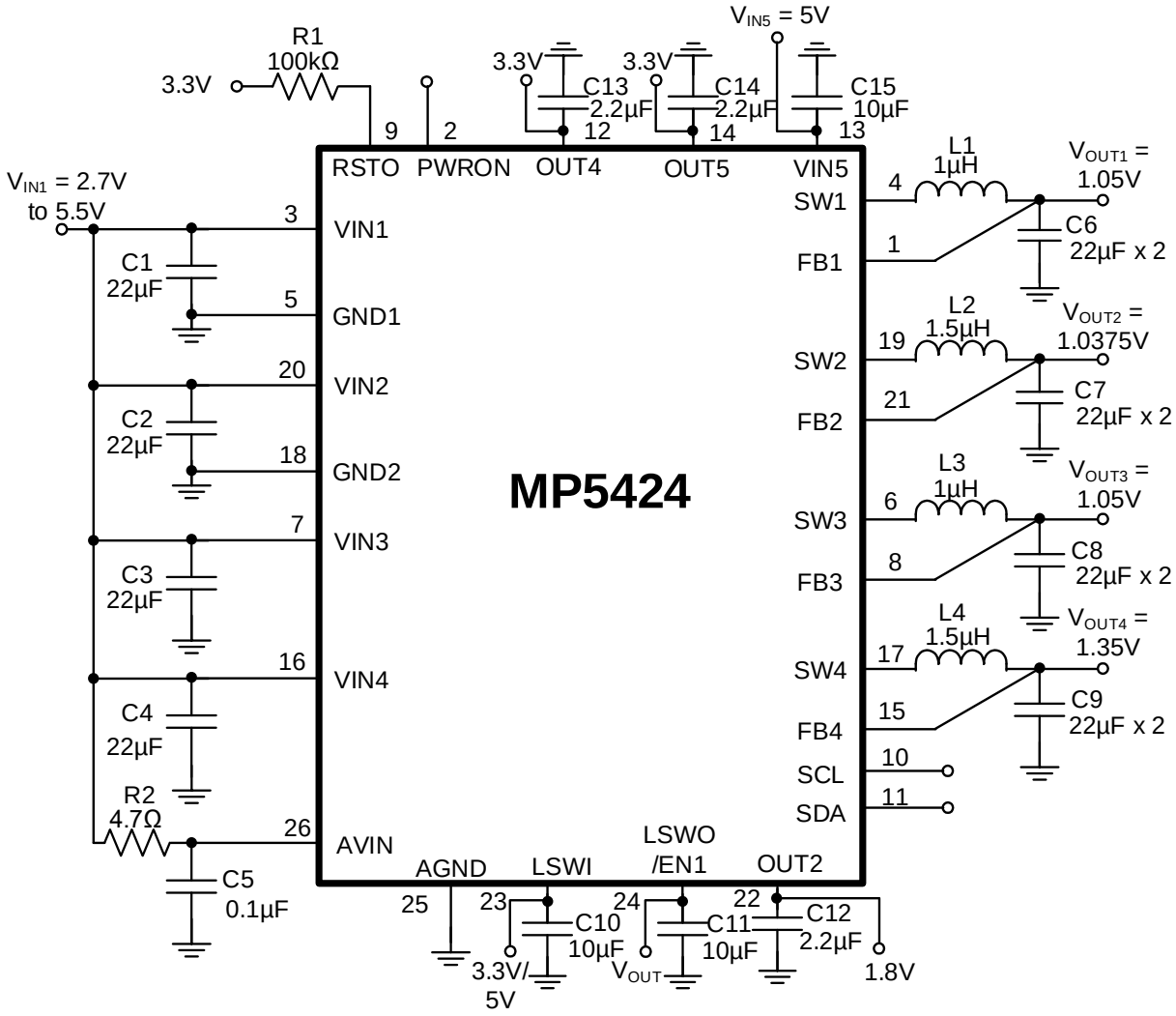

Figure 18: Typical Application Circuit (21) (22)

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TYPICAL APPLICATION CIRCUITS *(continued)*

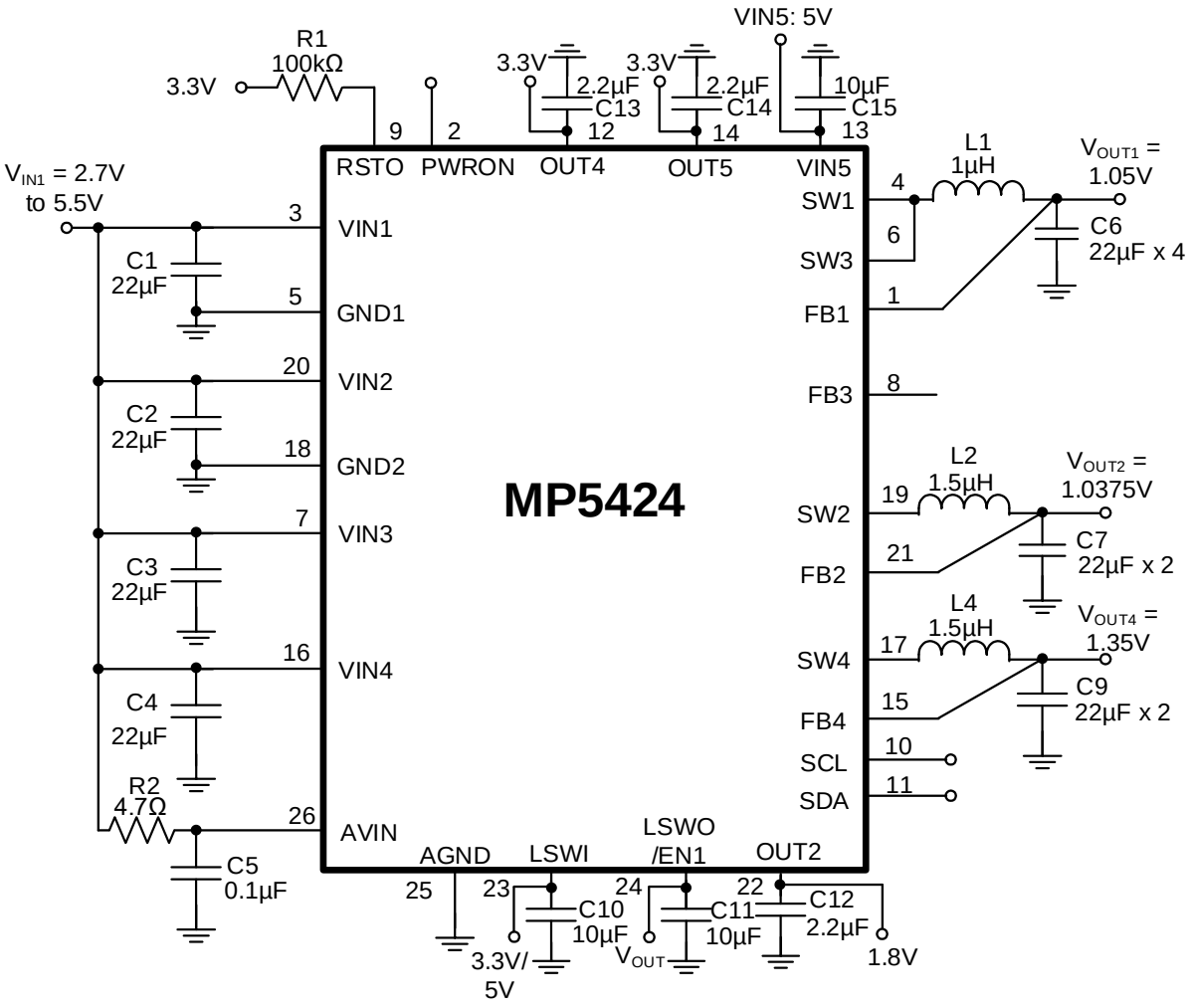

Figure 19: Typical Application Circuit (with Buck 1 and Buck 3 in Parallel) (21) (22)

Notes:

21) VIN5's minimum V_{IN} is equal to the maximum nominal V_{OUT} of LDO 4 and LDO 5. Connect the VIN5 and VIN1 pins if LDO 4 and LDO 5 are not used.

22) If operating at a 2.2MHz f_{SW} and with a small duty cycle, ensure that the buck's on time is >100ns for increased system stability.

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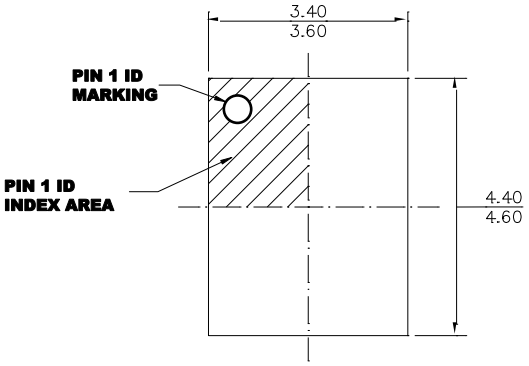
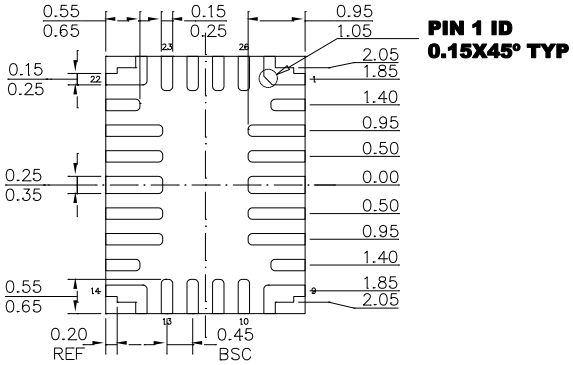
PACKAGE INFORMATION

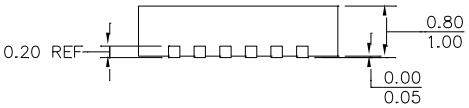
QFN-26 (3.5mmx4.5mm)



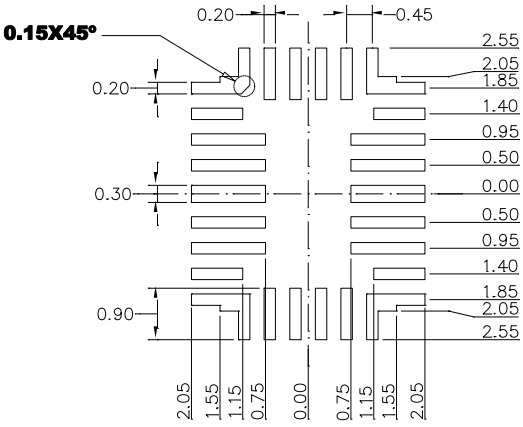
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1,9,14,22 HAVE THE SAME LENGTH AND WIDTH.
2)ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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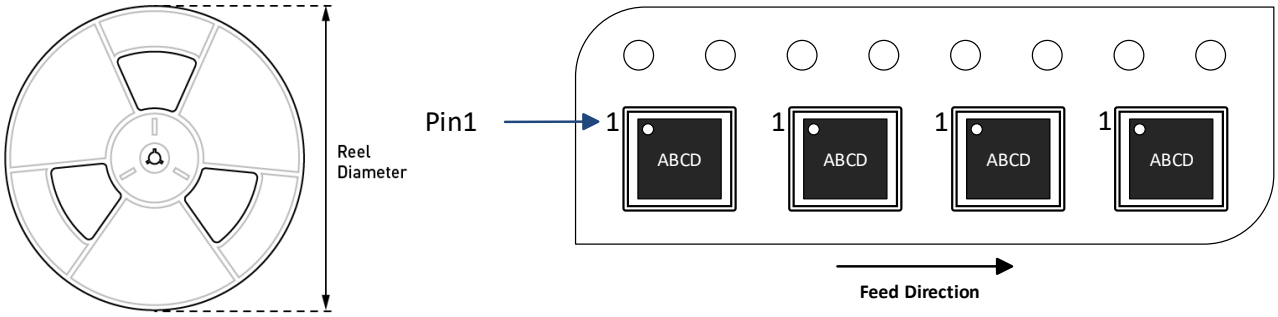
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5424GRM-0000-Z	QFN-26 (3.5mmx4.5mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/06/2021	Initial Release	-

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