

## Features

- ESD Protection for 1 Line with Bi-directional
- Provide ESD protection for the protected line to  
**IEC 61000-4-2 (ESD)  $\pm 15\text{kV}$  (air / contact)**  
**IEC 61000-4-4 (EFT) 40A (5/50ns)**  
**Cable Discharged Event (CDE)**
- Suitable for, **33V and below**, operating voltage applications
- **0402 small DFN package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

## Applications

- Cellular Handsets and Accessories
- Small Panel Modules
- Control Signal Line Protection
- Power Line Protection
- Portable Devices
- Touch Panels
- Notebooks and Handhelds
- Peripherals

## Description

AZ4233-01F is a design which includes one bi-directional ESD rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic system. The AZ4233-01F has been specifically designed to protect sensitive components which are connected to data and transmission lines from

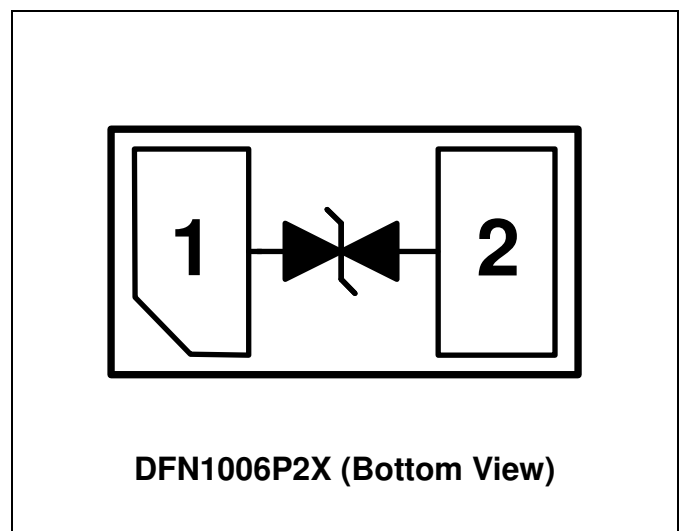
over-voltage damage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Cable Discharge Event (CDE).

AZ4233-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ4233-01F is bi-directional and may be used on lines where the signal swings above and below ground.

AZ4233-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram / Pin Configuration





## SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Operating Supply Voltage (pin-1 to pin-2)	$V_{DC}$	34	V
Pin-1 to pin-2 ESD per IEC 61000-4-2 (Air)	$V_{ESD-1}$	$\pm 15$	kV
Pin-1 to pin-2 ESD per IEC 61000-4-2 (Contact)	$V_{ESD-2}$	$\pm 15$	
Lead Soldering Temperature	$T_{SOL}$	260 (10 sec.)	$^{\circ}C$
Operating Temperature	$T_{OP}$	-55 to +85	$^{\circ}C$
Storage Temperature	$T_{STO}$	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	$V_{RWM}$	$T=25^{\circ}C$ .	-33		33	V
Reverse Leakage Current	$I_{Leak}$	$V_{RWM} = \pm 33V, T=25^{\circ}C$ .			1	$\mu A$
Reverse Breakdown Voltage	$V_{BV}$	$I_{BV} = 1mA, T=25^{\circ}C$ .	35		42	V
ESD Clamping Voltage (Note 1)	$V_{clamp}$	IEC 61000-4-2 +8kV ( $I_{TLP} = 16A$ ), Contact mode, $T=25^{\circ}C$ .		70		V
Channel Input Capacitance	$C_{IN}$	$V_R = 0V, f = 1MHz, T=25^{\circ}C$ .		13	20	pF

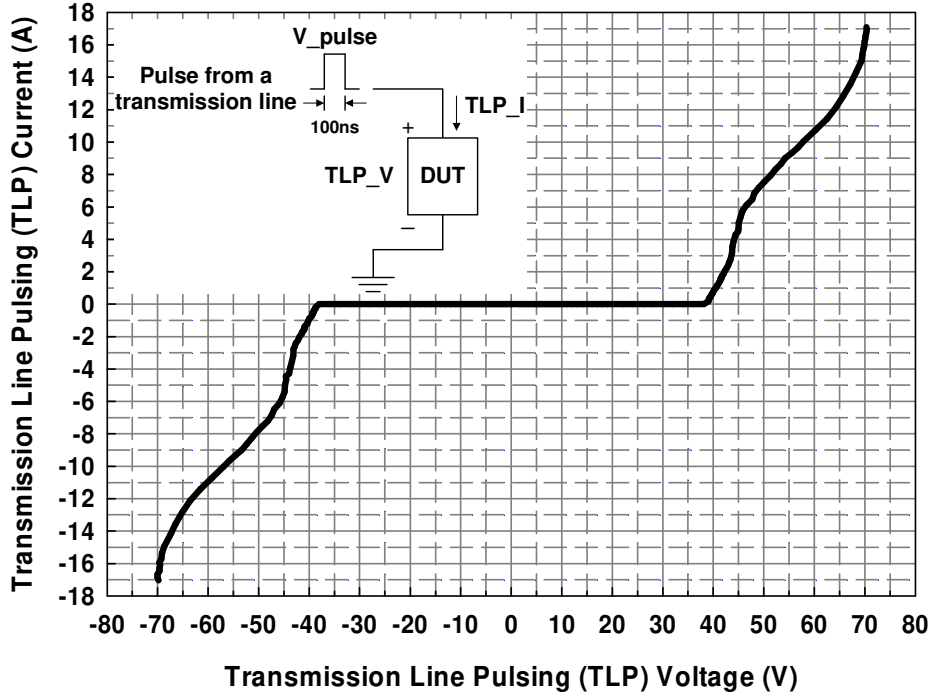
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions:  $Z_0 = 50\Omega, t_p = 100ns, t_r = 1ns$ .

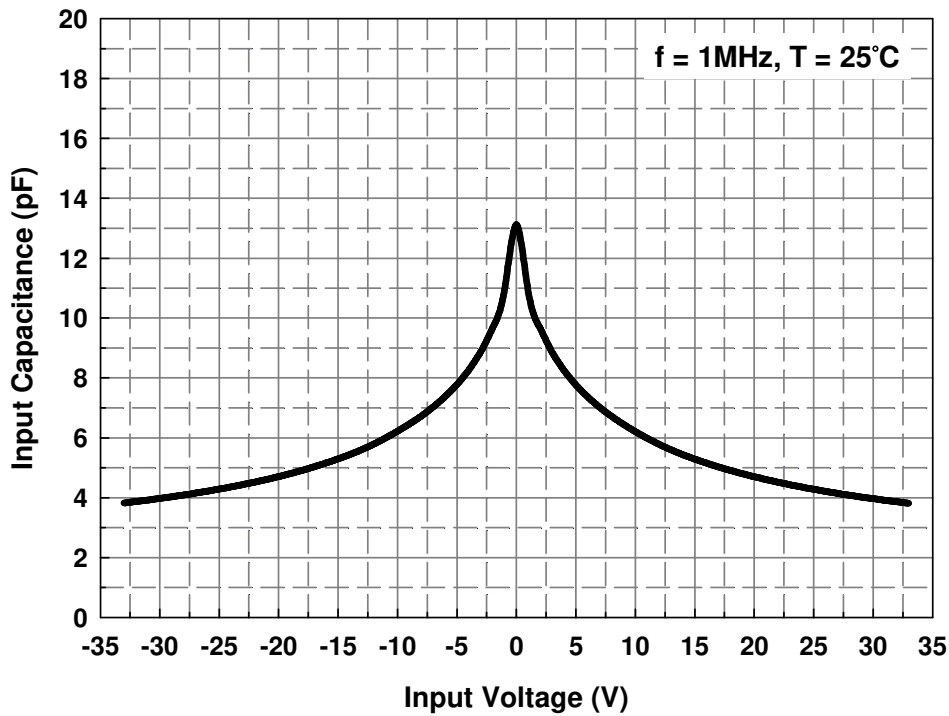


## Typical Characteristics

### Transmission Line Pulsing (TLP) Measurement



### Typical Variation of $C_{IN}$ vs. $V_{IN}$





## Applications Information

The AZ4233-01F is designed to protect one line against system ESD/EFT/CDE pulse by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ4233-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ4233-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4233-01F.
- Place the AZ4233-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

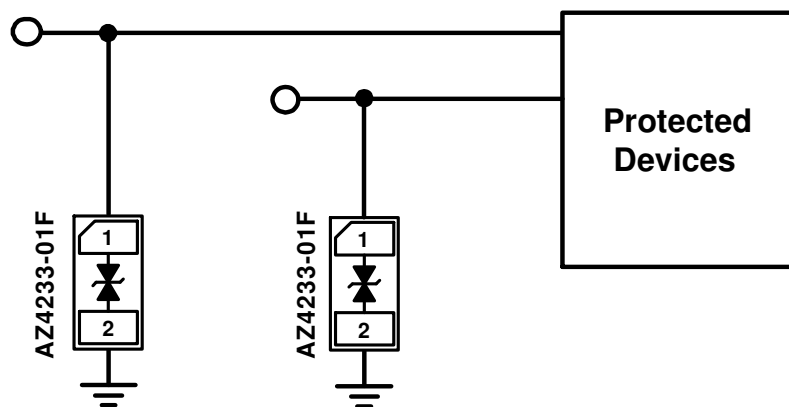
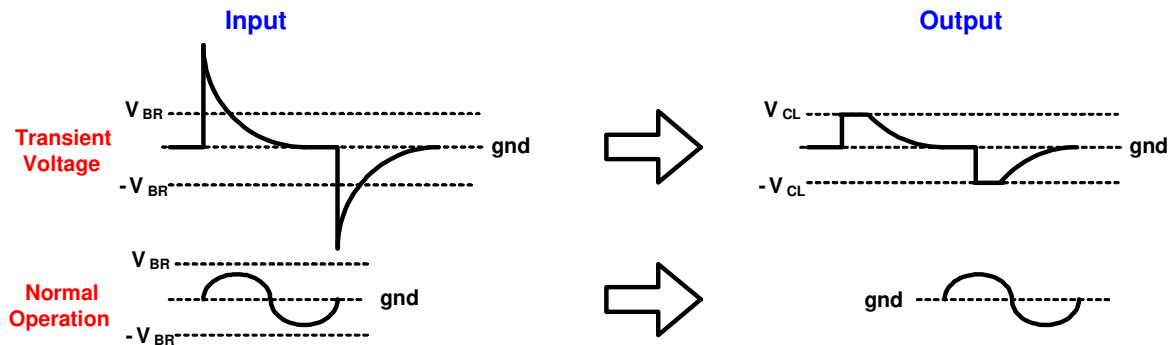


Fig. 1



Fig. 2 shows another simplified example of using AZ4233-01F to protect the control line, low speed data line, and power line from ESD transient stress.

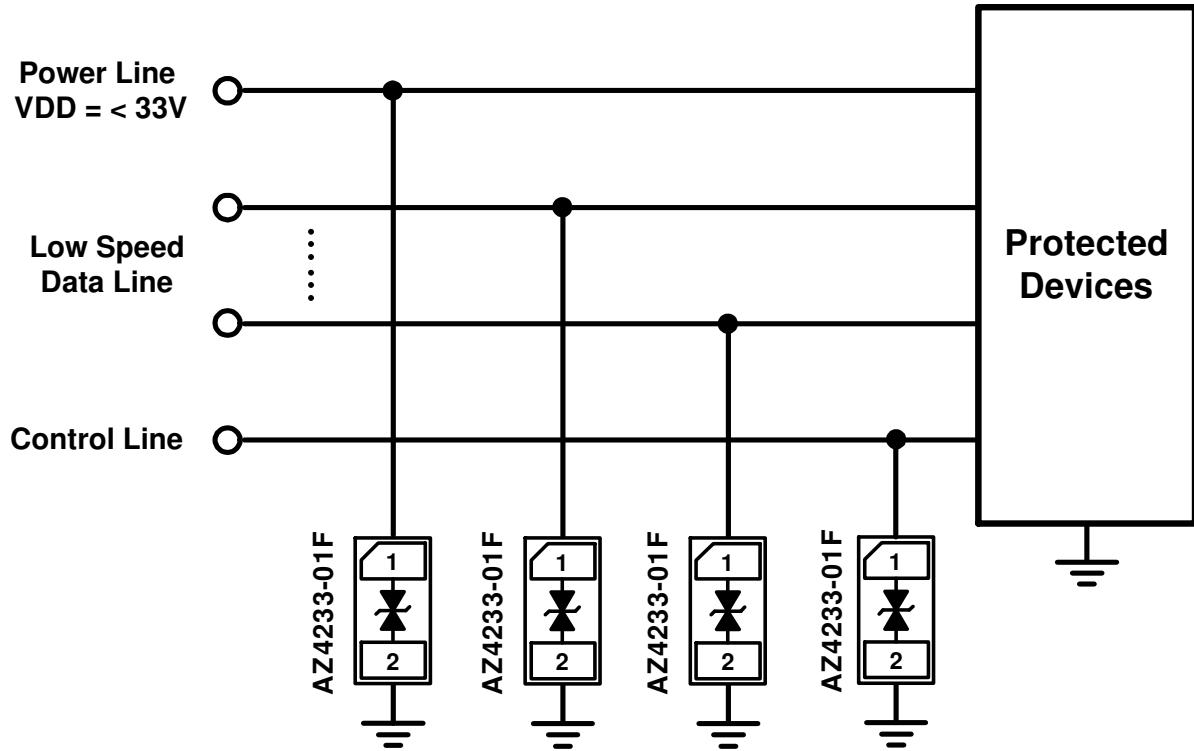
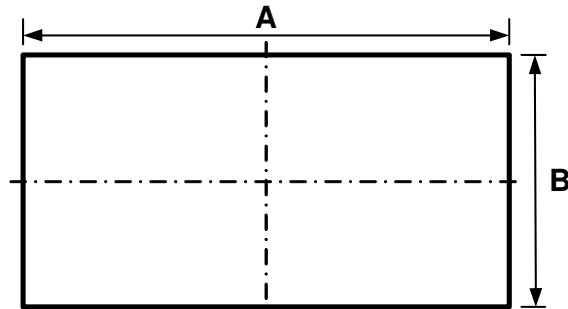


Fig. 2 ESD protection scheme by using AZ4233-01F.



## Mechanical Details

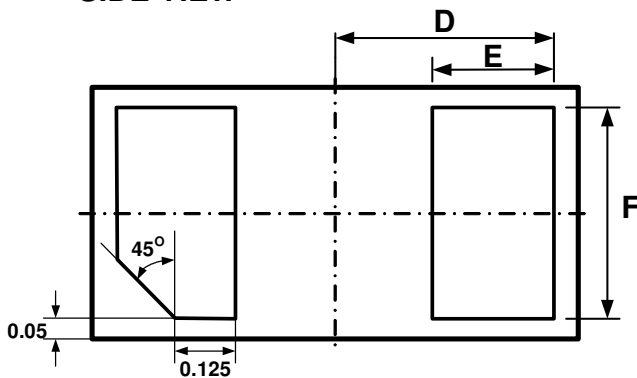
### DFN1006P2X PACKAGE DIAGRAMS



TOP VIEW



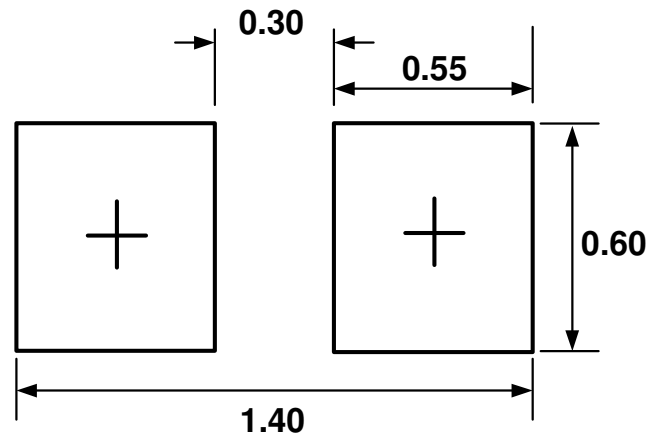
SIDE VIEW



BOTTOM VIEW

Symbol	Millimeters		Inches	
	min	max	min	max
A	0.95	1.05	0.037	0.041
B	0.55	0.65	0.022	0.026
C	0.40	0.55	0.016	0.022
D	0.45		0.018	
E	0.20	0.30	0.008	0.012
F	0.45	0.55	0.018	0.022

## LAND LAYOUT

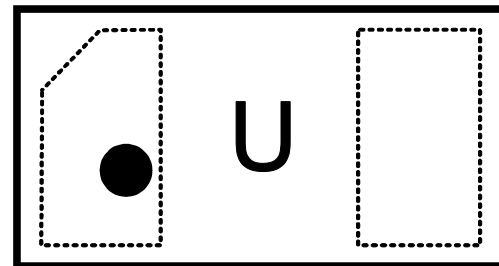


(Unit: mm)

### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## MARKING CODE



Top View

U = Device Code

Part Number	Marking Code
AZ4233-01F.R7GR (Green Part)	U

Note. Green means Pb-free, RoHS, and Halogen free compliant.



## Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ4233-01FR7GR	Green	T/R	7 inch	12,000/reel	4 reels = 48,000/box	6 boxes = 288,000/carton

## Revision History

Revision	Modification Description
Revision 2014/01/20	Preliminary Release.
Revision 2015/07/24	1. Update <b>ABSOLUTE MAXIMUM RATINGS</b> of ESD. 2. Add the Typical Characterization. 3. Add the Ordering information.
Revision 2017/05/16	Formal Release.
Revision 2019/05/31	Update the ordering information.