

MAC4DSM, MAC4DSN



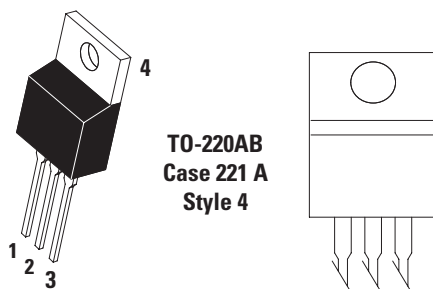
Description

The MAC4DSM and MAC4DSN are designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

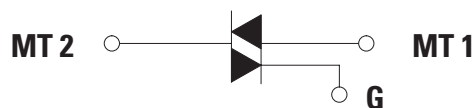
Features

- Small Size Surface Mount DPAK Package
- Passivated Die for Reliability and Uniformity
- Blocking Voltage to 800 V
- On-State Current Rating of 4.0 A RMS at 108°C
- Low IGT – 10 mA Maximum in 3 Quadrants
- High Immunity to dv/dt – 50 V/μs at 125°C
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V Machine Model, C > 400 V
- Pb-Free Packages are Available

Pin Out



Functional Diagram



Maximum Ratings ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (Gate Open, Sine Wave 50 to 60 Hz, $T_J = -40^\circ$ to 110°C)	V_{DRM} V_{RRM}	600 800	V
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, $T_C = 108^\circ\text{C}$)	$I_T (\text{RMS})$	4.0	A
Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, $T_C = 108^\circ\text{C}$)	I_{TSM}	40	A
Circuit Fusing Consideration ($t = 8.3$ msec)	I^2t	6.6	A ² sec
Peak Gate Current (Pulse Width ≤ 20 μsec , $T_C = 108^\circ\text{C}$)	I_{GM}	4.0	A
Peak Gate Power (Pulse Width ≤ 10 μsec , $T_C = 108^\circ\text{C}$)	P_{GM}	2.0	W
Peak Gate Voltage (Pulse Width ≤ 20 μsec , $T_C = 108^\circ\text{C}$)	V_{GM}	5.0	V
Average Gate Power ($t = 8.3$ msec, $T_C = 108^\circ\text{C}$)	$P_{\text{G(AV)}}$	1.0	W
Operating Junction Temperature Range	T_J	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

Thermal Characteristics

Rating	Symbol	Value	Unit
Thermal Resistance Junction-to-Case (AC) Junction-to-Ambient Junction-to-Ambient (Note 2)	$R_{\theta\text{JC}}$ $R_{\theta\text{JA}}$ $R_{\theta\text{JA}}$	3.5 88 80	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds (Note 3)	T_L	260	$^\circ\text{C}$

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

3. 1/8" from case for 10 seconds.

Electrical Characteristics - OFF ($T_J = 25^\circ\text{C}$ unless otherwise noted ; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Repetitive Blocking Current ($V_D = V_{\text{DRM}} = V_{\text{RRM}}$; Gate Open)	I_{DRM} I_{RRM}	-	-	0.01	mA
		-	-	2.0	

Electrical Characteristics - ON ($T_J = 25^\circ\text{C}$ unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak On-State Voltage (Note 4) ($I_{\text{TM}} = \pm 6.0$ A)	V_{TM}	-	1.3	1.6	V
Gate Trigger Current (Continuous dc) ($V_D = 12$ V, $R_L = 100$ Ω)	I_{GT}	2.9	4.0	10	mA
		2.9	5.0	10	
		2.9	7.0	10	
Holding Current ($V_D = 12$ V, Gate Open, Initiating Current = ± 200 mA)	I_{H}	2.0	5.5	1.5	mA
Latching Current	I_{L}	-	6.0	30	mA
		-	10	30	
		-	6.0	30	
Gate Trigger Voltage (Continuous dc) ($V_D = 12$ V, $R_L = 100$ Ω)	V_{GT}	0.5	0.7	1.3	V
		0.5	0.65	1.3	
		0.5	0.7	1.3	
Gate Non-Trigger Voltage ($T_J = 125^\circ\text{C}$) ($V_D = 12$ V, $R_L = 100$ Ω)	V_{GD}	0.2	0.4	-	V
		0.2	0.4	-	
		0.2	0.4	-	

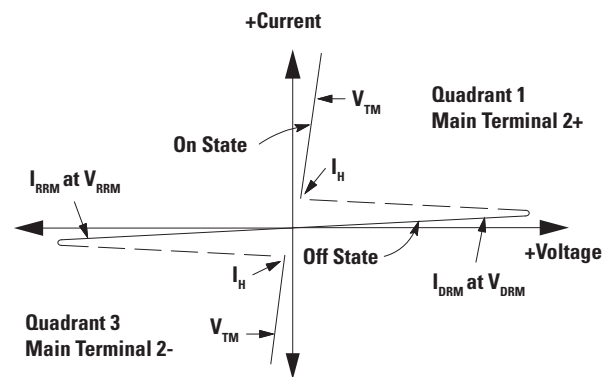
4. Indicates Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle $\leq 2\%$.

Dynamic Characteristics

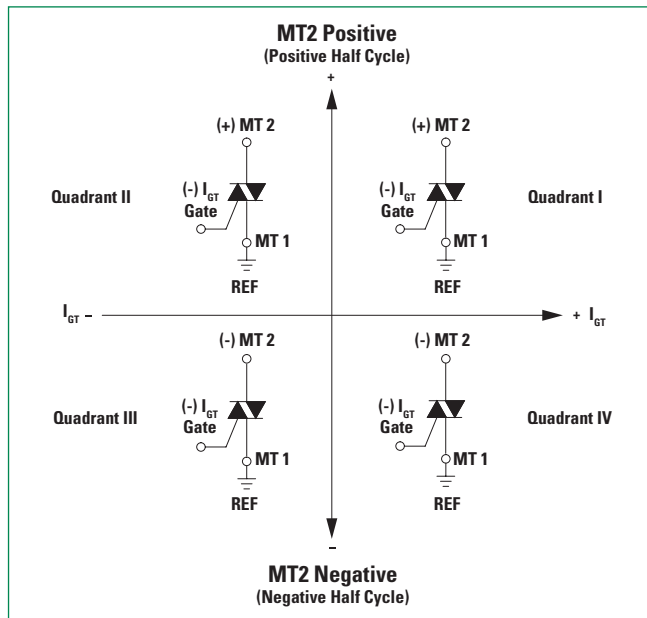
Characteristic	Symbol	Min	Typ	Max	Unit
Rate of Change of Commutating Current ($V_D = 400\text{ V}$, $I_{TM} = 3.5\text{ A}$, Commutating $dv/dt = 10\text{ V}/\mu\text{sec}$, Gate Open, $T_J = 125^\circ\text{C}$, $f = 500\text{ Hz}$, $CL = 5.0\text{ }\mu\text{F}$, $LL = 20\text{ mH}$, No Snubber) See Figure 16	$(di/dt)_c$	2.0	4.0	–	A/ms
Critical Rate of Rise of Off-State Voltage ($V_D = 0.67 \times V_{DRM}$, Exponential Waveform, Gate Open, $T_J = 125^\circ\text{C}$)	dV/dt	50	175	–	V/ μs

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All Polarities are referenced to MT1.
With in-phase signals (using standard AC lines) quadrants I and III are used

Figure 1. Typical RMS Current Derating

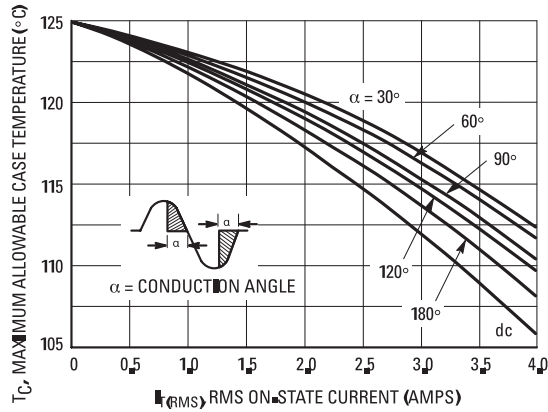


Figure 2. On-State Power Dissipation

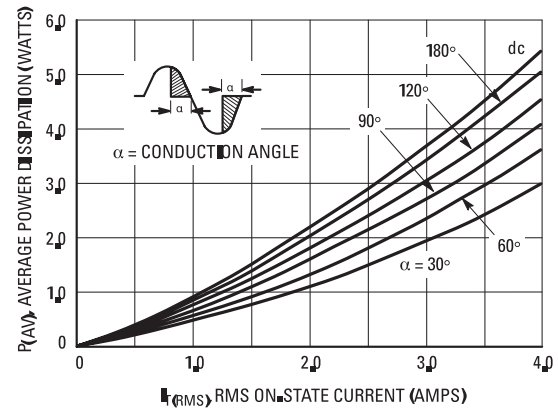


Figure 3. On-State Characteristics

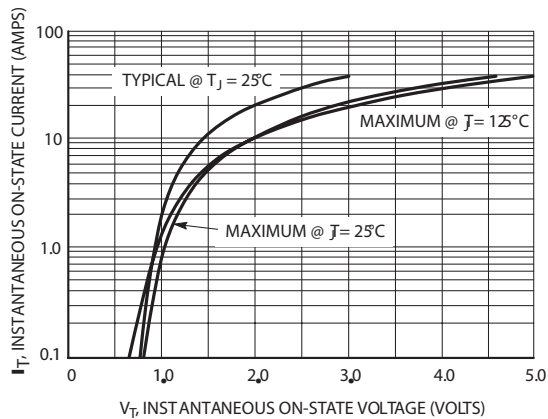


Figure 4. Transient Thermal Response

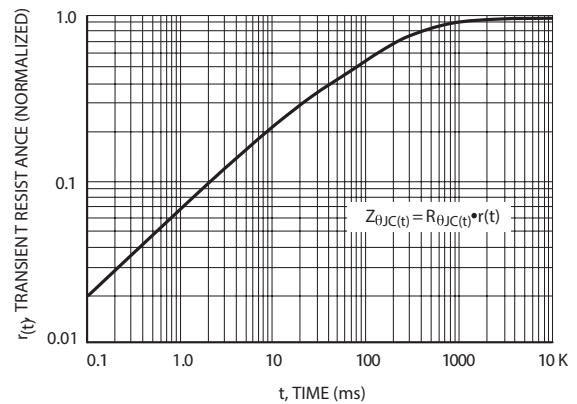


Figure 5. Typical Gate Trigger Current vs. Junction Temperature

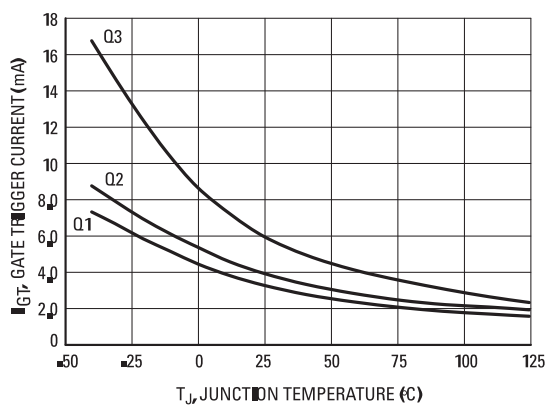


Figure 6. Typical Gate Trigger Voltage vs. Junction Temperature

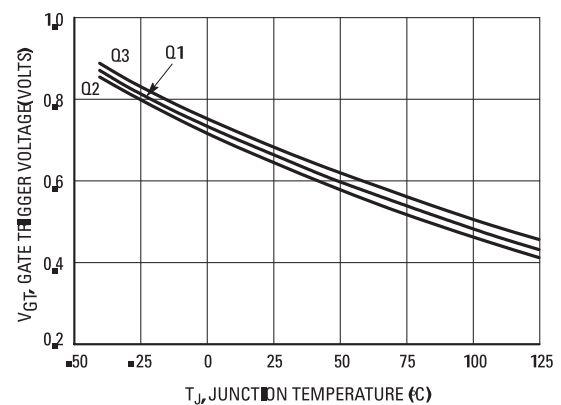


Figure 7. Typical Holding Current vs. Junction Temperature

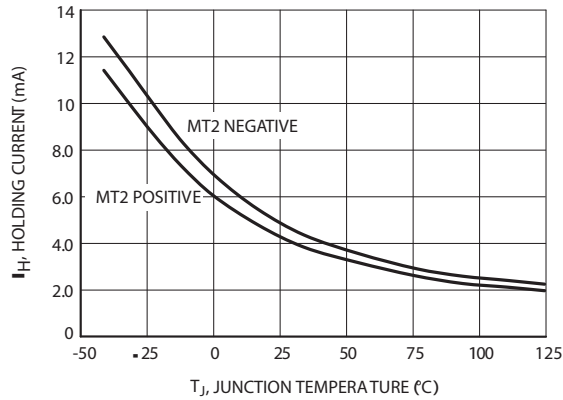


Figure 8. Typical Latching Current vs. Junction Temperature

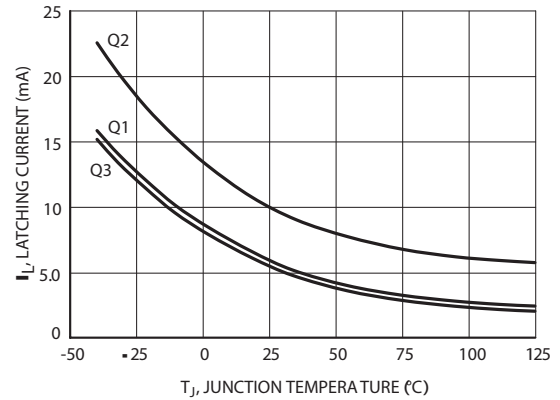


Figure 9. Exponential Static dv/dt vs. Gate-MT1 Resistance, MT2(+)

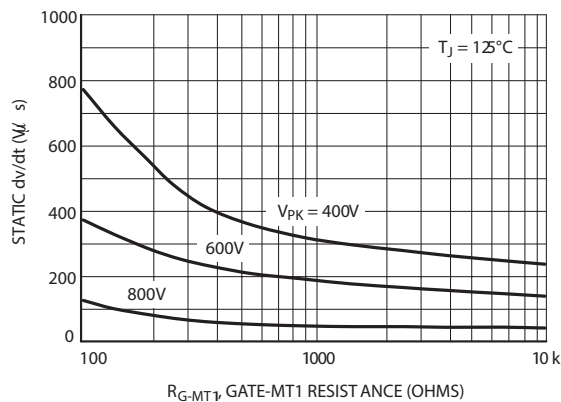


Figure 10. Exponential Static dv/dt vs. Gate-MT1 Resistance, MT2(-)

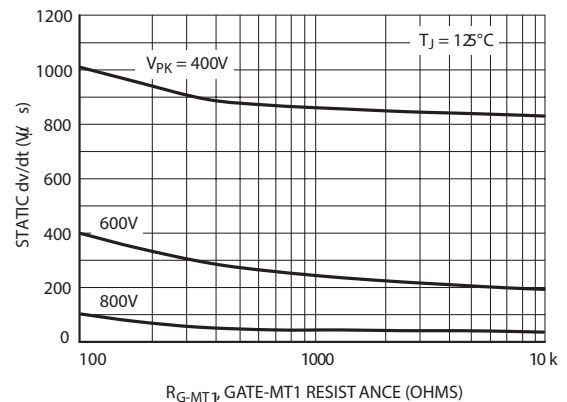


Figure 9. Exponential Static dv/dt vs. Gate-MT1 Resistance, MT2(+)

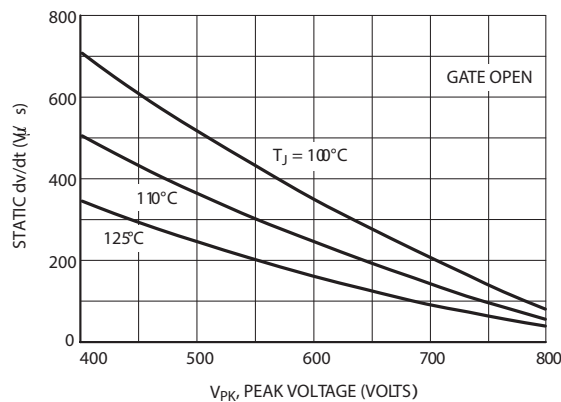


Figure 10. Exponential Static dv/dt vs. Gate-MT1 Resistance, MT2(-)

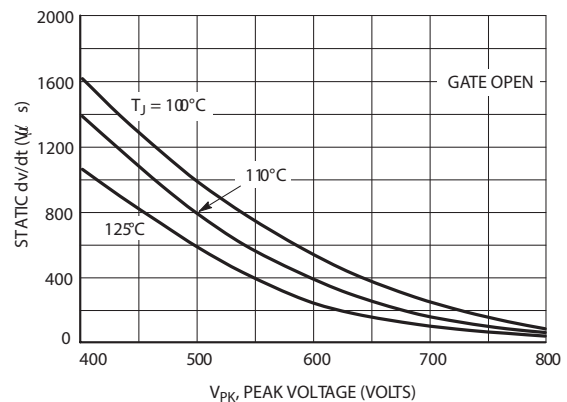


Figure 13. Typical Holding Current vs. Junction Temperature

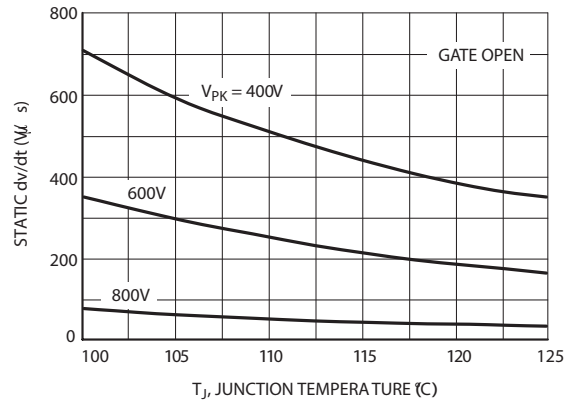


Figure 14. Typical Latching Current vs. Junction Temperature

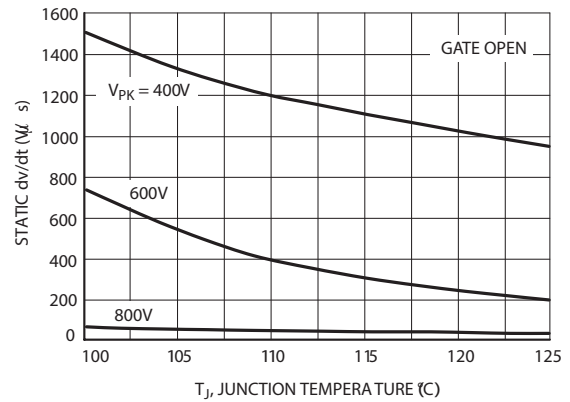


Figure 15. Typical Holding Current vs. Junction Temperature

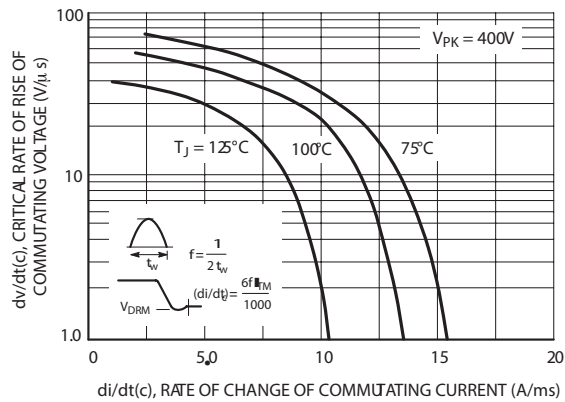
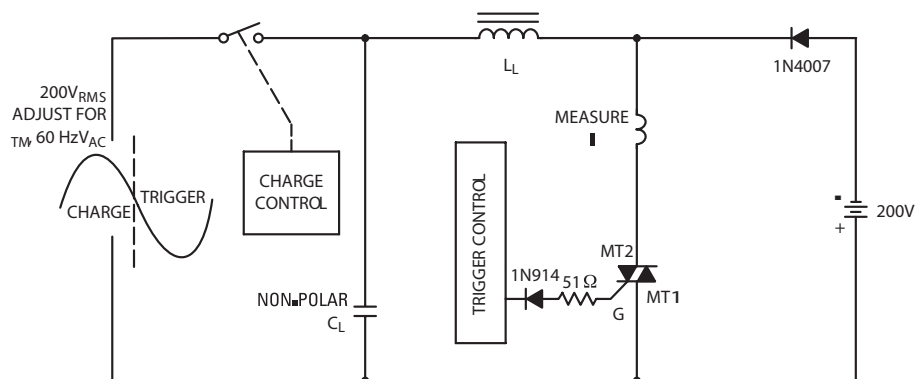
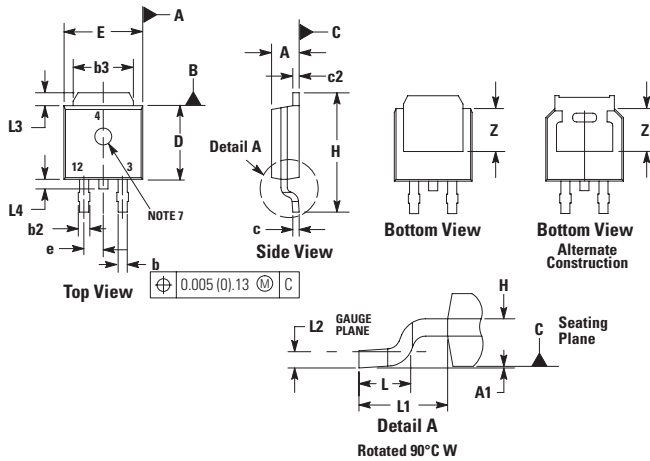


Figure 16. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current (di/dt)

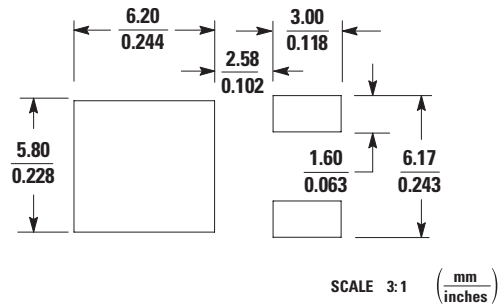


Note: Component values are for verification of rated (di/dt). See AN1048 for additional information.

Dimensions



Soldering Footprint

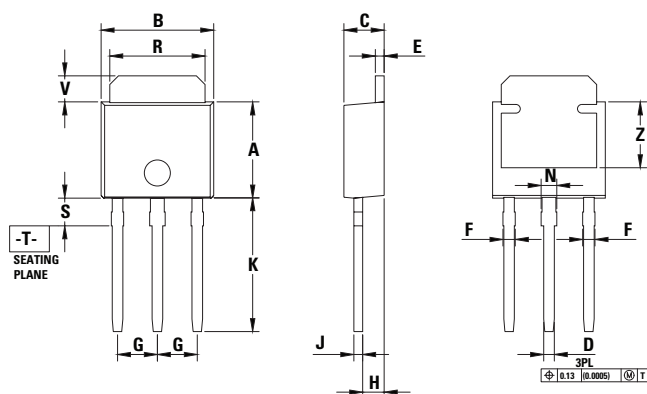


Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.087	0.094	2.20	2.40
A1	0.000	0.005	0.00	0.12
b	0.022	0.030	0.55	0.75
b2	0.026	0.033	0.65	0.85
b3	0.209	0.217	5.30	5.50
c	0.019	0.023	0.49	0.59
c2	0.019	0.023	0.49	0.59
D	0.213	0.224	5.40	5.70
E	0.252	0.260	6.40	6.60
e	0.091		2.30	
H	0.374	0.406	9.50	10.30
L	0.058	0.070	1.47	1.78
L1	0.114		2.90	
L2	0.019	0.023	0.49	0.59
L3	0.053	0.065	1.35	1.65
L4	0.028	0.039	0.70	1.00
Z	0.154	-	3.90	-

1. Dimensioning and tolerancing per ansi y14.5m, 1982.
2. Controlling Dimension: inch. Style 6: Pin 1. Mt1
2. Mt2
3. Gate
4. Mt2

Dimensions

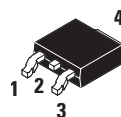
DPAK-3
Case 369D
T0251-3L POD



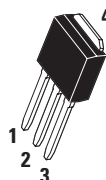
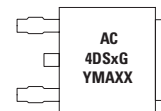
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.213	0.224	5.40	5.70
B	0.252	0.260	6.40	6.60
C	0.087	0.094	2.20	2.40
D	0.024	0.030	0.60	0.75
E	0.022	0.026	0.55	0.65
F	0.022	0.03	0.58	0.78
G	0.091		2.30	
H	0.046	0.050	1.18	1.28
J	0.019	0.023	0.49	0.59
K	0.291	0.315	7.40	8.00
N	0.03	0.038	0.78	0.98
R	0.209	0.217	5.30	5.50
S	0.063		1.60	
V	0.053	0.065	1.35	1.65
Z	0.150		3.80	

1. Dimensioning and Tolerancing Per ANSI Y14.5M, 1982.
2. Controlling Dimension: Inch.
- STYLE 6: Pin 1. MT1
2. MT2
3. Gate
4. MT2

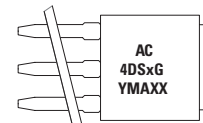
Part Marking System



DPAK-3
Case 369C
Style 6



DPAK-3
Case 369D
Style 6



AC4DCx = Device Code
x = M, or N
Y = Year
M = Month
A = Assembly Site
XX = Lot Serial Code
G = Pb-Free Package

Pin Assignment	
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

Ordering Information

Device	Package Type	Package	Shipping
MAC4DSM-001	DPAK-3	369D	4000 Unit/Box
MAC4DSM-001G	DPAK-3 (Pb-Free)	369D	4000 Unit/Box
MAC4DSMT4	DPAK-3	369C	2500 / Tape & Reel
MAC4DSMT4G	DPAK-3 (Pb-Free)	369C	2500 / Tape & Reel
MAC4DSN-001	DPAK-3	369D	4000 Unit/Box
MAC4DSN-001G	DPAK-3 (Pb-Free)	369D	4000 Unit/Box
MAC4DSNT4	DPAK-3	369C	2500 / Tape & Reel