

High Efficiency Thyristor

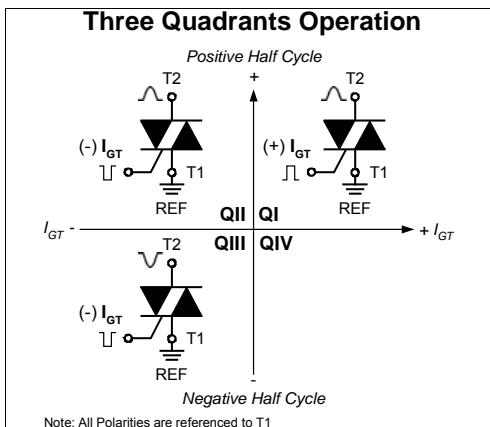
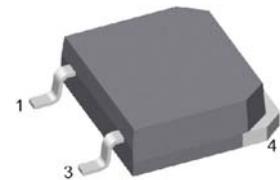
V_{RRM} = 1200 V
 I_{TAV} = 30 A
 V_T = 1,25 V

Three Quadrants operation: QI - QIII
1~ Triac

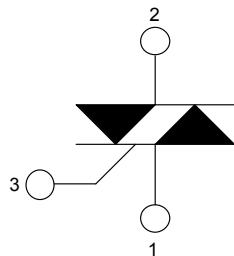
Part number

CLA60MT1200NTZ

Marking on Product: *CLA60MT1200NTZ*



Backside: anode/cathode



Features / Advantages:

- Triac for line frequency
- Three Quadrants Operation - QI - QIII
- Planar passivated chip
- Long-term stability of blocking currents and voltages

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-268AA (D3Pak-HV)

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0
- High creepage distance between terminals

Disclaimer Notice

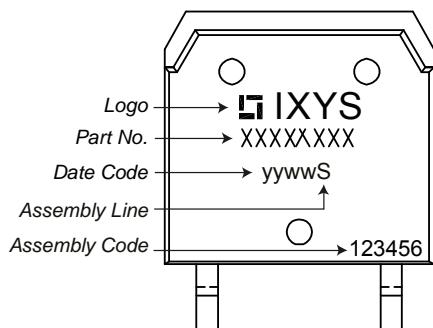
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Rectifier

Symbol	Definition	Conditions	Ratings			
			min.	typ.	max.	
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^\circ C$			1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^\circ C$			1200	V
I_{RD}	reverse current, drain current	$V_{RD} = 1200 \text{ V}$ $V_{RD} = 1200 \text{ V}$	$T_{VJ} = 25^\circ C$ $T_{VJ} = 125^\circ C$		10 2	μA mA
V_T	forward voltage drop	$I_T = 30 \text{ A}$ $I_T = 60 \text{ A}$ $I_T = 30 \text{ A}$ $I_T = 60 \text{ A}$	$T_{VJ} = 25^\circ C$ $T_{VJ} = 125^\circ C$		1,28 1,56 1,25 1,61	V V V V
I_{TAV}	average forward current	$T_C = 120^\circ C$	$T_{VJ} = 150^\circ C$		30	A
I_{RMS}	RMS forward current per phase	180° sine			66	A
V_{TO}	threshold voltage	r_T slope resistance } for power loss calculation only	$T_{VJ} = 150^\circ C$		0,86	V
	slope resistance				12,5	$m\Omega$
R_{thJC}	thermal resistance junction to case				0,55	K/W
R_{thCH}	thermal resistance case to heatsink			0,15		K/W
P_{tot}	total power dissipation		$T_C = 25^\circ C$		230	W
I_{TSM}	max. forward surge current	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{sine}$ $t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{sine}$ $t = 10 \text{ ms}; (50 \text{ Hz}), \text{sine}$ $t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{sine}$	$T_{VJ} = 45^\circ C$ $V_R = 0 \text{ V}$ $T_{VJ} = 150^\circ C$ $V_R = 0 \text{ V}$		380 410 325 350	A A
I^2t	value for fusing	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{sine}$ $t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{sine}$ $t = 10 \text{ ms}; (50 \text{ Hz}), \text{sine}$ $t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{sine}$	$T_{VJ} = 45^\circ C$ $V_R = 0 \text{ V}$ $T_{VJ} = 150^\circ C$ $V_R = 0 \text{ V}$		720 700 530 510	A^2s A^2s A^2s A^2s
C_J	junction capacitance	$V_R = 400 \text{ V}$ $f = 1 \text{ MHz}$	$T_{VJ} = 25^\circ C$	25		pF
P_{GM}	max. gate power dissipation	$t_p = 30 \mu s$ $t_p = 300 \mu s$	$T_C = 150^\circ C$		10 5 0,5	W W W
P_{GAV}	average gate power dissipation					
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^\circ C; f = 50 \text{ Hz}$ repetitive, $I_T = 90 \text{ A}$ $t_p = 200 \mu s; di_G/dt = 0,3 \text{ A}/\mu s;$ $I_G = 0,3 \text{ A}; V_D = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 30 \text{ A}$			150	$A/\mu s$
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V_D = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty$; method 1 (linear voltage rise)	$T_{VJ} = 150^\circ C$		500	$V/\mu s$
V_{GT}	gate trigger voltage	$V_D = 6 \text{ V}$	$T_{VJ} = 25^\circ C$ $T_{VJ} = -40^\circ C$		1,7 1,9	V V
I_{GT}	gate trigger current	$V_D = 6 \text{ V}$	$T_{VJ} = 25^\circ C$ $T_{VJ} = -40^\circ C$		± 60 ± 80	mA mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^\circ C$		0,2	V
I_{GD}	gate non-trigger current				± 1	mA
I_L	latching current	$t_p = 10 \mu s$ $I_G = 0,3 \text{ A}; di_G/dt = 0,3 \text{ A}/\mu s$	$T_{VJ} = 25^\circ C$		90	mA
I_H	holding current	$V_D = 6 \text{ V}$ $R_{GK} = \infty$	$T_{VJ} = 25^\circ C$		60	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$ $I_G = 0,3 \text{ A}; di_G/dt = 0,3 \text{ A}/\mu s$	$T_{VJ} = 25^\circ C$		2	μs
t_q	turn-off time	$V_R = 100 \text{ V}; I_T = 30 \text{ A}; V_D = \frac{2}{3} V_{DRM}$ $T_{VJ} = 125^\circ C$ $di/dt = 10 \text{ A}/\mu s$ $dv/dt = 20 \text{ V}/\mu s$ $t_p = 200 \mu s$		150		μs

Package TO-268AA (D3Pak-HV)

Symbol	Definition	Conditions	Ratings			
			min.	typ.	max.	
I_{RMS}	RMS current	per terminal			70	A
T_{VJ}	virtual junction temperature		-40		150	°C
T_{op}	operation temperature		-40		125	°C
T_{stg}	storage temperature		-40		150	°C
Weight				4		g
F_c	mounting force with clip		20		120	N
$d_{Spp/App}$	creepage distance on surface striking distance through air	terminal to terminal	9,4			mm
$d_{Spb/Apb}$		terminal to backside	5,6			mm

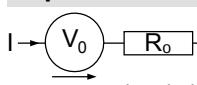
Product Marking

Part description

C = Thyristor (SCR)
 L = High Efficiency Thyristor
 A = (up to 1200V)
 60 = Current Rating [A]
 MT = 1~ Triac
 1200 = Reverse Voltage [V]
 N = Three Quadrants operation: QI - QIII
 TZ = TO-268AA (D3Pak) (2HV)

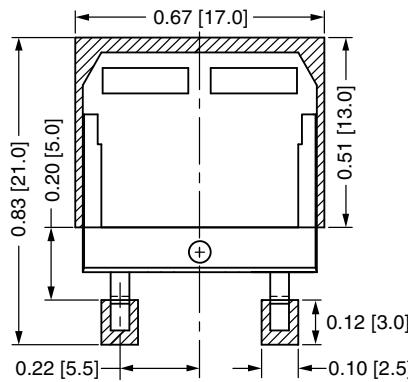
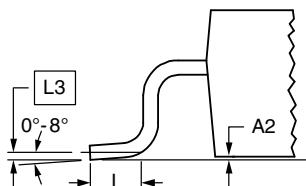
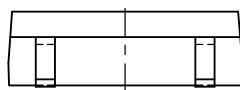
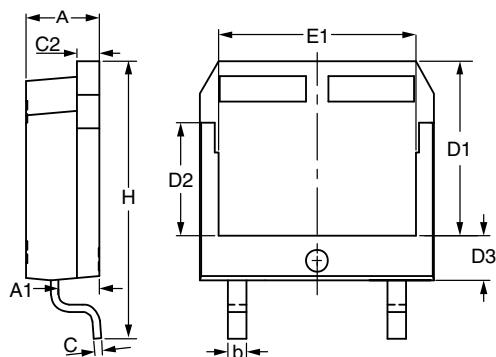
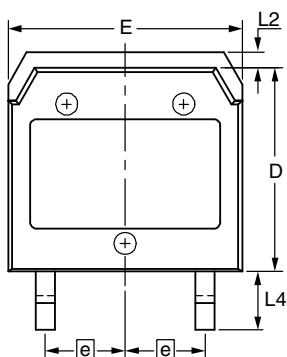
Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA60MT1200NTZ-TUB	CLA60MT1200NTZ	Tube	30	512767
Alternative	CLA60MT1200NTZ-TRL	CLA60MT1200NTZ	Tape & Reel	400	525122

Similar Part	Package	Voltage class
CLA60MT1200NHB	TO-247AD (3)	1200
CLA60MT1200NHR	ISO247 (3)	1200

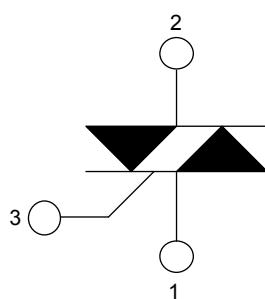
Equivalent Circuits for Simulation
** on die level*
 $T_{VJ} = 150^\circ\text{C}$

	Thyristor	
V_0	threshold voltage	0,86
$R_{0\max}$	slope resistance *	10

V
 $\text{m}\Omega$

Outlines TO-268AA (D3Pak-HV)


Dim.	Millimeter		Inches	
	min	max	min	max
A	4.90	5.10	0.193	0.201
A1	2.70	2.90	0.106	0.114
A2	0.02	0.25	0.001	0.010
b	1.15	1.45	0.045	0.057
C	0.40	0.65	0.016	0.026
C2	1.45	1.60	0.057	0.063
D	13.80	14.00	0.543	0.551
D1	11.80	12.10	0.465	0.476
D2	7.50	7.80	0.295	0.307
D3	2.90	3.20	0.114	0.126
E	15.85	16.05	0.624	0.632
E1	13.30	13.60	0.524	0.535
e	5.450	BSC	0.215	BSC
H	18.70	19.10	0.736	0.752
L	1.70	2.00	0.067	0.079
L2	1.00	1.15	0.039	0.045
L3	0.250	BSC	0.010	BSC
L4	3.80	4.10	0.150	0.161

RECOMMENDED MINIMUM FOOT PRINT


Thyristor

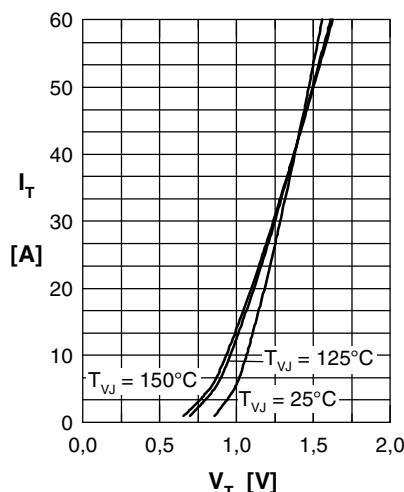


Fig. 1 Forward characteristics

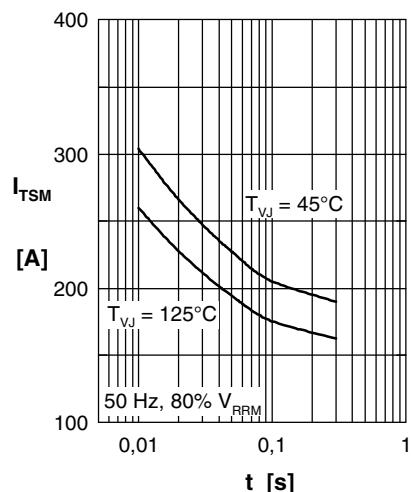


Fig. 2 Surge overload current
 I_{TSM} : crest value, t : duration

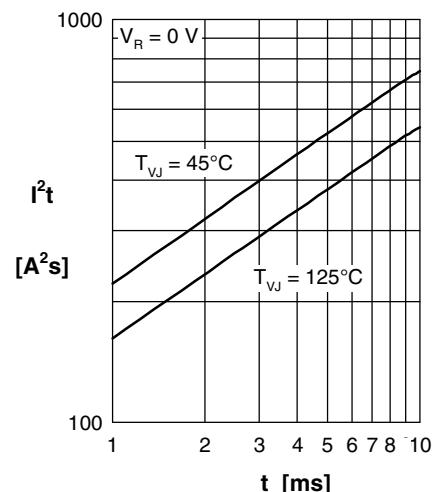


Fig. 3 I^2t versus time (1-10 s)

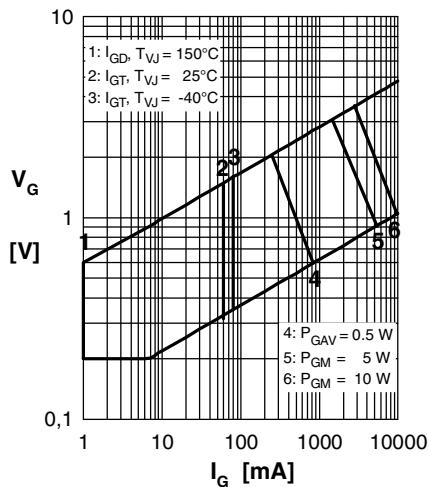


Fig. 4 Gate voltage & gate current

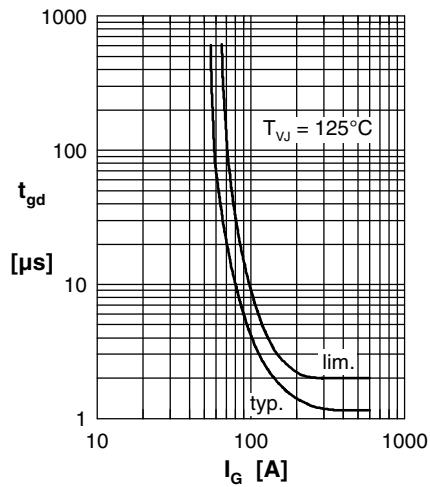


Fig. 5 Gate controlled delay time t_{gd}

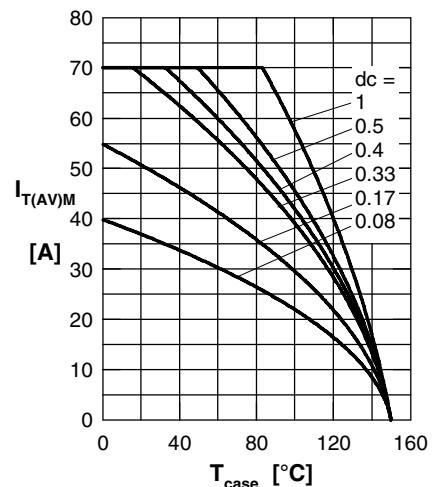


Fig. 6 Max. forward current at case temperature

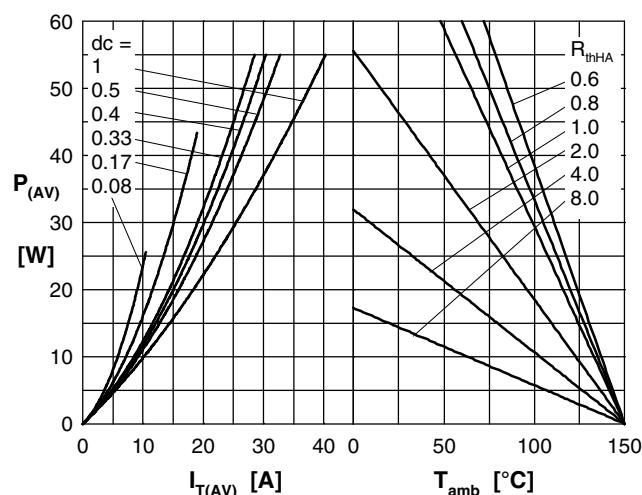


Fig. 7a Power dissipation versus direct output current
Fig. 7b and ambient temperature

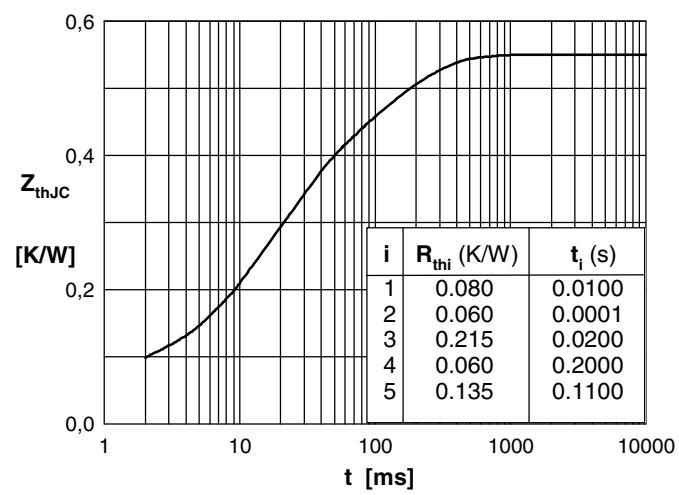


Fig. 7 Transient thermal impedance junction to case