2-Bit Dual-Supply **Non-Inverting Level Translator**

NLSV2T244

The NLSV2T244 is a 2-bit configurable dual-supply voltage level translator. The input A_n and output B_n ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal low-voltage translation from the input A_n to the output B_n port.

Features

- Wide V_{CCA} and V_{CCB} Operating Range: 0.9 V to 4.5 V
- High-Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 4.5 V
- Non-preferential V_{CCA} and V_{CCB} Sequencing
- Outputs at 3-State until Active V_{CC} is Reached
- Power-Off Protection
- Outputs Switch to 3-State with V_{CCB} at GND
- Small Packaging: UDFN8, SO-8, Micro8
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable*
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

 Typical Applications

 Typical Applications

• Mobile Phones, PDAs, Other Portable Devices

Important Information

• ESD Protection for All Pins:

HBM (Human Body Model) > 5000

MARKING DIAGRAMS



UDFN8 MU SUFFIX CASE 517AJ



= Specific Device Code = Date Code = Pb-Free Package



SO-8 **D SUFFIX CASE 751**



Assembly Location Wafer Lot = Year = Work Week Pb-Free Package



Micro8 DM SUFFIX CASE 846A



Assembly Location = Year = Work Week Pb-Free Package

ORDERING INFORMATION

; AEC-Q100 C Free and are RoHS	Y = Year W = Work Week Pb-Free Package						
2F JTRO FOR	ORDERING INFORMATION						
COLLIE.	Device	Package	Shipping [†]				
MATATI	NLSV2T244MUTAG	UDFN8 (Pb-Free)	3000 / Tape & Reel				
	NLSV2T244DR2G	SO-8 (Pb-Free)	2500 / Tape & Reel				
	NLSV2T244DMR2G	Micro8 (Pb-Free)	4000 / Tape & Reel				
	NLVSV2T244DMR2G*	Micro8 (Pb-Free)	4000 / Tape & Reel				

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

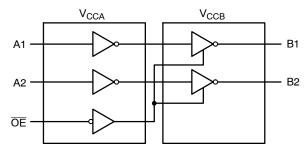
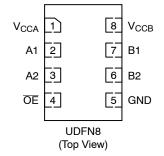
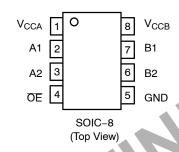
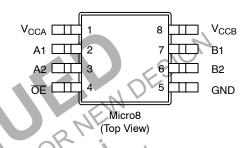


Figure 1. Logic Diagram

PIN ASSIGNMENTS







PIN ASSIGNMENT

PIN	FUNCTION
V _{CCA}	Input Port DC Power Supply
V _{CCB}	Output Port DC Power Supply
GND	Ground
A _n	Input Port
B _n	Output Port
ŌĒ	Output Enable
THIS DE	VICEPLEASEN

TRUTH TABLE

O Ch	puts	Outputs
Œ	A _n	B _n
10, WP	L	L
RLI	Н	Н
О, н	Х	3-State

MAXIMUM RATINGS

Symbol	Rating		Value	Condition	Unit
V _{CCA} , V _{CCB}	DC Supply Voltage		-0.5 to +5.5		V
VI	DC Input Voltage	A _n	-0.5 to +5.5		V
V _C	Control Input	ΟE	-0.5 to +5.5		V
Vo	DC Output Voltage (Power Down)	B _n	-0.5 to +5.5	V _{CCA} = V _{CCB} = 0	V
	(Active Mode)	B _n	-0.5 to +5.5		V
	(Tri-State Mode)	B _n	-0.5 to +5.5		V
I _{IK}	DC Input Diode Current		-20	V _I < GND	mA
lok	DC Output Diode Current		-50	V _O < GND	mA
Io	DC Output Source/Sink Current		±50		mA
I _{CCA} , I _{CCB}	DC Supply Current Per Supply Pin		±100		mA
I _{GND}	DC Ground Current per Ground Pin		±100	(2)	mA
T _{STG}	Storage Temperature		-65 to +150	CIQ!	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Paramet	ter	Min	Max	Unit
V_{CCA}, V_{CCB}	Positive DC Supply Voltage		0.9	4.5	V
VI	Bus Input Voltage	SEI	GND	4.5	V
V_{C}	Control Input	OE (GND	4.5	V
V _{IO}	Bus Output Voltage	(Power Down Mode) B _n	GND	4.5	V
		(Active Mode) B _n	GND	V _{CCB}	V
		(Tri-State Mode) B _n	GND	4.5	V
T _A	Operating Temperature Range	MICH	-40	+85	°C
Δt / ΔV	Input Transition Rise or Rate V_I , from 30% to 70% of V_{CC} ; $V_{CC} = 3$.3 ∨ ±0.3 V	0	10	nS

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

					-40°C to	+85°C	
Symbol	Parameter	Test Conditions	V _{CCA} (V)	V _{CCB} (V)	Min	Max	Unit
V _{IH}	Input HIGH Voltage		3.6 – 4.5	0.9 – 4.5	2.2	-	V
	(An, \overline{OE})		2.7 – 3.6		2.0	-	
			2.3 – 2.7		1.6	-	
			1.4 – 2.3		0.65 * V _{CCA}	-	
			0.9 – 1.4		0.9 * V _{CCA}	-	
V _{IL}	Input LOW Voltage		3.6 – 4.5	0.9 – 4.5	_	0.8	V
	(An, \overline{OE})		2.7 – 3.6		-	0.8	
			2.3 – 2.7		-	0.7	
			1.4 – 2.3		-	0.35 * V _{CCA}	
			0.9 – 1.4		-	0.1 * V _{CCA}	
V _{OH}	Output HIGH Voltage	I _{OH} = -100 μA; V _I = V _{IH}	0.9 – 4.5	0.9 – 4.5	V _{CCB} - 0.2	Ms	V
		$I_{OH} = -0.5 \text{ mA}; V_I = V_{IH}$	0.9	0.9	0.75 * V _{CCB}	CIO)	
		I _{OH} = -2 mA; V _I = V _{IH}	1.4	1.4	1.05	-	
		$I_{OH} = -6 \text{ mA}; V_I = V_{IH}$	1.65	1.65	1\25	-	
			2.3	2.3	2.0	_	
		I _{OH} = -12 mA; V _I = V _{IH}	2.3	2.3	1.8	_	
		OH I III	2.7	2.7	2.2	<u> </u>	
		$I_{OH} = -18 \text{ mA}; V_{I} = V_{IH}$	2.3	2,3 5	1.7	_	
		OH TOWNS TO VIA	3.0	3.0	2.4	_	
		$I_{OH} = -24 \text{ mA}; V_{I} = V_{IH}$	3.0	3.0	2.2		
V _{OL}	Output LOW Voltage	$I_{OL} = 100 \mu\text{A}; V_{I} = V_{IL}$	0.9 – 4.5	0.9 – 4.5	_	0.2	V
*OL	output 2011 Voltage	$I_{OL} = 0.5 \text{ mA; } V_{I} = V_{IL}$	1,12	1.1	_	0.3	
		$I_{OL} = 0.5 \text{ mA}; V_I = V_{IL}$	1.4	1.4		0.35	
			1.65	1.65	_	0.33	
		$I_{OL} = 0 \text{ IIA}, V_1 = V_{IL}$ $I_{OL} = 12 \text{ mA}; V_1 = V_{IL}$	2.3	2.3	_	0.3	
	151	10F = 15114, AL AL			_		
	CE CP	I _{OL} = 18 mA; V _I = V _{IL}	2.7	2.7	-	0.4	
	OF ICE IS NO EDEVICE PLEA	10L = 18 MA, VI = VIL	2.3	2.3	-	0.6	
	DE DE	04 24 74 74	3.0	3.0	_	0.4	
	CV CV	I _{OL} = 24 mA; V _I = V _{IL}	3.0	3.0	-	0.55	
lı .	Input Leakage Current	V _I = V _{CCA} or GND	0.9 – 4.5	0.9 – 4.5	-1.0	1.0	μΑ
l _{OFF}	Power-Off Leakage Current	OE = 0 V	0 0.9 – 4.5	0.9 – 4.5 0	–1.0 –1.0	1.0 1.0	μΑ
I _{CCA}	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$, $V_{CCA} = V_{CCB}$	0.9 – 4.5	0.9 – 4.5	-	1.0	μΑ
I _{CCB}	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$, $V_{CCA} = V_{CCB}$	0.9 – 4.5	0.9 – 4.5	-	1.0	μΑ
CA + ICCB	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$, $V_{CCA} = V_{CCB}$	0.9 – 4.5	0.9 – 4.5	-	2.0	μΑ
ΔI_{CCA}	Increase in I _{CC} per Input Voltage, Other Inputs at V _{CCA} or GND	$V_I = V_{CCA} - 0.6 V;$ $V_I = V_{CCA}$ or GND	4.5 3.6	4.5 3.6	-	10 5.0	μΑ
ΔI_{CCB}	Increase in I_{CC} per Input Voltage, Other Inputs at V_{CCA} or GND	$V_I = V_{CCA} - 0.6 V;$ $V_I = V_{CCA}$ or GND	4.5 3.6	4.5 3.6	-	10 5.0	μА
I _{OZ}	I/O Tri-State Output Leakage Current	$T_A = 25^{\circ}C, \overline{OE} = 0 V$	0.9 – 4.5	0.9 – 4.5	-1.0	1.0	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TOTAL STATIC POWER CONSUMPTION (I_{CCA} + I_{CCB})

					-40°C to	o +85°C					
	V _{CCB} (V)										
	4.	4.5 3.3 2.8 1.8 0.9									
V _{CCA} (V)	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
4.5		2		2		2		2		< 1.5	μΑ
3.3		2		2		2		2		< 1.5	μΑ
2.8		< 2		< 1		< 1		< 0.5		< 0.5	μΑ
1.8		< 1		< 1		< 0.5		< 0.5		< 0.5	μΑ
0.9		< 0.5		< 0.5		< 0.5		< 0.5		< 0.5	μΑ

NOTE: Connect ground before applying supply voltage V_{CCA} or V_{CCB}. This device is designed with the feature that the power–up sequence of V_{CCA} and V_{CCB} will not damage the IC.

AC ELECTRICAL CHARACTERISTICS

			-40°C to +85°C										
		,		V _{CCB} (V)									
			4.	.5	3.	3	2.	.8	1.	8	(F)	2	
Symbol	Parameter	V _{CCA} (V)	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t _{PLH} ,	Propagation	4.5		1.6		1.8		2.0	1	2.1		2.3	nS
t _{PHL} (Note 1)	Delay,	3.3		1.7		1.9		2.1	R	2.3		2.6	
(11010-1)	A _n to B _n	2.8		1.9		2.1		2.3	,	2.5	N	2.8	
		1.8		2.1		2.4		2.5	250	2.7		3.0	
		1.2		2.4		2.7	10.	2.8	N	3.0		3.3	
t _{PZH} ,	Output Enable,	4.5		2.6		3.8	0	4.0	DL.	4.1		4.3	nS
t _{PZL} (Note 1)	,	3.3		3.7	ON	3.9	7	4.1		4.3		4.6	
(11010-1)	OE to B _n	2.5		3.9	7	4.1	R	4.3		4.5		4.8	
		1.8	/	4.1	7	4.4		4.5		4.7		5.0	
		1.2	0,	4.4), '(4.7		4.8		5.0		5.3	
t _{PHZ} ,	Output	4.5	S	2.6	. V.	3.8		4.0		4.1		4.3	nS
t _{PLZ} (Note 1)	Disable,	3.3	· P	3.7	,	3.9		4.1		4.3		4.6	
(11010-1)	OE to B _n	2.5		3.9		4.1		4.3		4.5		4.8	
	OF"	1.8	60	4.1		4.4		4.5		4.7		5.0	
	115	1.2		4.4		4.7		4.8		5.0		5.3	
t _{OSHL} ,	Output to	4.5		0.15		0.15		0.15		0.15		0.15	nS
t _{OSLH} (Note 1)	Output Skew,	3.3		0.15		0.15		0.15		0.15		0.15	
(14010-1)	Time	2.5		0.15		0.15		0.15		0.15		0.15	
		1.8		0.15		0.15		0.15		0.15		0.15	
		1.2		0.15		0.15		0.15		0.15		0.15	

^{1.} Propagation delays defined per Figure 2.

CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 2)	Unit
C _{IN}	Control Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CCA/B}$	3.5	pF
C _{I/O}	I/O Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CCA/B}$	5.0	pF
C _{PD}	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CCA}, f = 10 \text{ MHz}$	20	pF

Typical values are at T_A = +25°C.
 C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: I_{CC(operating)} ≅ C_{PD} x V_{CC} x f_{IN} x N_{SW} where I_{CC} = I_{CCA} + I_{CCB} and N_{SW} = total number of outputs switching.

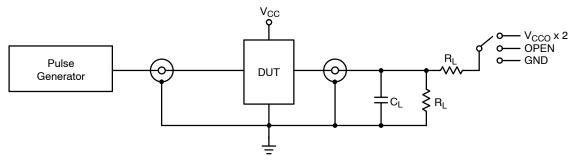


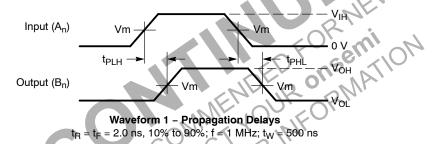
Figure 2. AC (Propagation Delay) Test Circuit

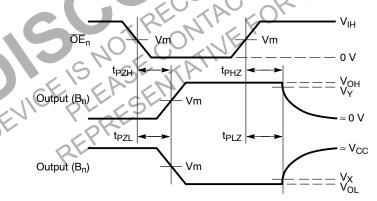
Test	Switch
t _{PLH} , t _{PHL}	OPEN
t _{PLZ} , t _{PZL}	V _{CCO} x 2
t _{PHZ} , t _{PZH}	GND

C_L = 15 pF or equivalent (includes probe and jig capacitance)

 R_L = 2 $k\Omega$ or equivalent

 Z_{OUT} of pulse generator = 50 Ω





Waveform 2 – Output Enable and Disable Times $t_R = t_F = 2.0 \text{ ns}, 10\% \text{ to } 90\%; f = 1 \text{ MHz}; t_W = 500 \text{ ns}$

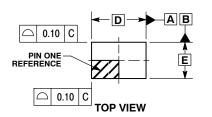
Figure 3. AC (Propagation Delay) Test Circuit Waveforms

	V _{CC}							
Symbol	3.0 V – 4.5 V	2.3 V – 2.7 V	1.65 V – 1.95 V	1.4 V – 1.6 V	0.9 V – 1.3 V			
V _{mA}	V _{CCA} /2							
V _{mB}	V _{CCB} /2							
V _X	V _{OL} x 0.1							
V_{Y}	V _{OH} x 0.9							

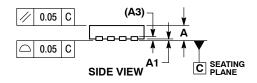
SCALE 4:1

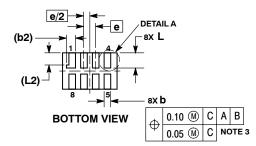


DATE 08 NOV 2006

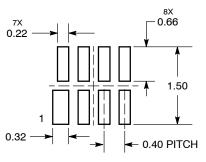








MOUNTING FOOTPRINT SOLDERMASK DEFINED



DIMENSIONS: MILLIMETERS

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSION & APPLIES TO PLATED
- DINICIPION D APPLIES TO PLATED
 TERMINAL AND IS MEASURED BETWEEN
 0.15 AND 0.30 mm FROM TERMINAL TIP.
 MOLD FLASH ALLOWED ON TERMINALS
 ALONG EDGE OF PACKAGE, FLASH MAY
 NOT EXCEED 0.03 ONTO BOTTOM
 SURFACE OF TERMINALS.
 DETAIL A SHOWS ODTIONAL
- DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

	MILLIMETERS						
DIM	MIN	MAX					
Α	0.45	0.55					
A1	0.00	0.05					
A3	0.127	REF					
b	0.15	0.25					
b2	0.30	REF					
D	1.80	BSC					
E	1.20	BSC					
е	0.40	BSC					
L	0.45	0.55					
L1	0.00	0.03					
L2	0.40	REF					

GENERIC MARKING DIAGRAM*



XX = Specific Device Code

= Date Code

= Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

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DESCRIPTION:	UDFN8 1.8X1.2, 0.4P		PAGE 1 OF 1

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SOIC-8 NB CASE 751-07 **ISSUE AK**

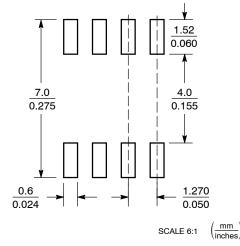
DATE 16 FEB 2011



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

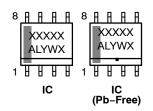
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.80	5.00	0.189	0.197
В	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC 0.10 0.25		0.050 BSC	
Н			0.10 0.25 0.004 0.01	0.010
7	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
М	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



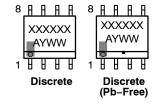
^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code = Assembly Location = Wafer Lot = Year = Work Week W

= Pb-Free Package



XXXXXX = Specific Device Code = Assembly Location Α

= Year ww = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB		PAGE 1 OF 2

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SOIC-8 NB CASE 751-07 ISSUE AK

DATE 16 FEB 2011

			DITTE TO LED 2
STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	8. DRAIN 1 STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC STYLE 21: PIN 1. CATHODE 1	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE STYLE 22: PIN 1. I/O LINE 1	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1 STYLE 23: PIN 1. LINE 1 IN	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN STYLE 24: PIN 1. BASE
2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

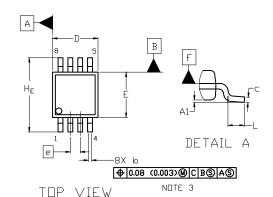
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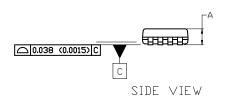
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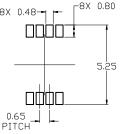






NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DDES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
- DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
- A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



RECOMMENDED MOUNTING FOOTPRINT

MID	MILLIMETERS		
ואונע	MIN.	N□M.	MAX.
Α	-	-	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
С	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
HE	4.75	5.05	
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code Α = Assembly Location

Υ = Year W = Work Week = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:	STYLE 2:	STYLE 3:
PIN 1. SOURCE	PIN 1. SOURCE 1	PIN 1. N-SOURCE
SOURCE	2. GATE 1	2. N-GATE
SOURCE	3. SOURCE 2	P-SOURCE
GATE	4. GATE 2	4. P-GATE
DRAIN	5. DRAIN 2	5. P-DRAIN
DRAIN	6. DRAIN 2	6. P-DRAIN
7. DRAIN	7. DRAIN 1	7. N-DRAIN
8. DRAIN	8. DRAIN 1	8. N-DRAIN

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DESCRIPTION:	DESCRIPTION: MICRO8		PAGE 1 OF 1

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