NVT4558

SIM card interface level translator with EMI filter and ESD protection

Rev. 1.1 — 6 September 2023 Product data sheet

1 General description

The NVT4558 device is built for interfacing a SIM card with a single low-voltage 1.08 V to 1.98 V host side interface. The NVT4558 contains three 1.62 V to 3.6 V level translators to convert the data, RSTn and CLKn signals between a SIM card and a host microcontroller.

The NVT4558 has been optimized for operation with mobile phone processors that support 1.2 V I/O and 1.8 V I/O.

The NVT4558 is compliant with all ISO-7816 SIM/Smart card interface requirements and is compliant with JEDEC JESD76-2 requirements for CMOS 1.2 V logic devices.

2 Features and benefits

- Supports clock speed up to 10 MHz clock
- Compliant with all ISO-7816 SIM/Smart card interface requirements
- Support SIM card supply voltages with range of 1.62 V to 3.6 V
- Host microcontroller operating voltage range: 1.08 V to 1.98 V
- Automatic level translation of I/O, RSTn and CLKn between SIM card and host side interface with capacitance isolation
- Incorporates shutdown feature for the SIM card signals according to ISO-7816-3
- Enable and disable through hardware enable pin or with automatic enable and disable feature
- Integrated pull-up and pull-down resistors
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Integrated 8 kV ESD protection according to IEC 61000-4-2, level 4 on V_{CCB} or any of the card side pins
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Available in 10-pin XQFN10 package with 0.4 mm pitch

3 Applications

- NVT4558 can be used with a range of SIM card attached devices including:
  - Mobile and personal phones
  - Wireless modems
  - SIM card terminals

4 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NVT4558HK	58	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm	SOT1160-1

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NVT4558HK	NVT4558HKX	XQFN10	Reel 7" Q1/T1 NDP	4000	T_{amb} = -40 °C to +85 °C

5 Functional diagram

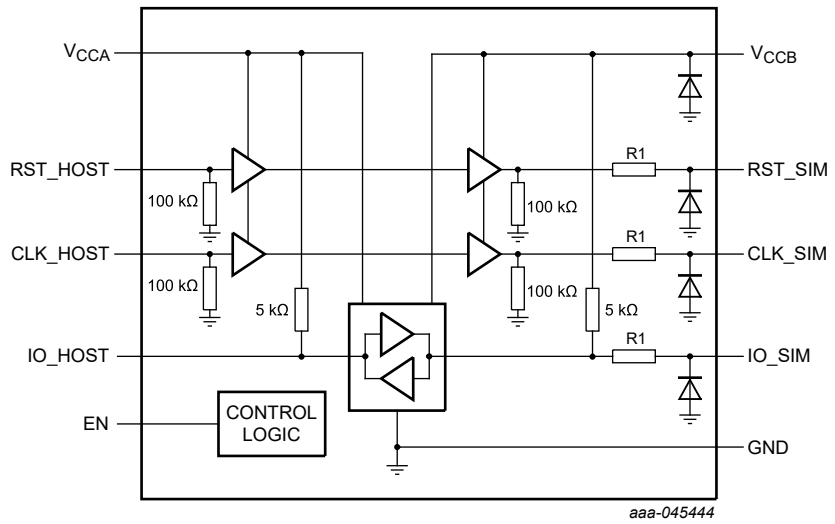


Figure 1. Functional diagram

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

6 Pinning information

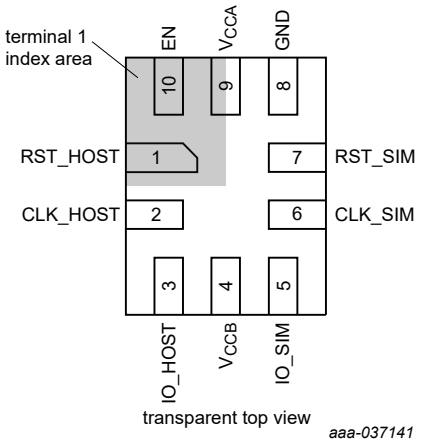


Figure 2. Pin configuration for XQFN10

6.1 Pin description

Table 3. Pin description

Symbol	Pinning for XQFN10	Type	Description
RST_HOST	1	I	Reset input from host controller.
V_{CCA}	9	supply	Supply voltage for the host controller side input/output pins (CLK_HOST, RST_HOST, IO_HOST). This pin should be bypassed with a 0.1 µF ceramic capacitor close to the pin.
RST_SIM	7	O	Reset output pin for the SIM card.
CLK_HOST	2	I	Clock input from host controller.
GND	8	ground	Ground for the SIM card and host controller. Proper grounding and bypassing are required to meet ESD specifications.
CLK_SIM	6	O	Clock output pin for the SIM card.
IO_HOST	3	I/O	Host controller bidirectional data input/output. The host output must be on an open-drain driver.
V_{CCB}	4	supply	SIM card supply voltage. When V_{CCB} is below the V_{CCB_DIS}, the device is disabled. This pin should be bypassed with a 0.1 µF ceramic capacitor close to the pin.
IO_SIM	5	I/O	SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver.
EN	10	I	Host controller driven enable pin. This pin should be HIGH (V_{CCA}) for normal operation, and LOW to help avoid race conditions specifically during the shutdown sequence.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

7 Functional description

Table 4. Function table

Supply voltage		Input	Input/output		Operational mode
V_{CCA}	V_{CCB}	EN [1] [2]	Host	SIM card	
1.08 V to 1.98 V	1.62 V to 3.6 V	H	HOST = SIM Card	SIM Card = HOST	Active
1.08 V to 1.98 V	1.62 V to 3.6 V	L	See Table 5, Condition B		Shutdown Mode
GND	1.62 V to 3.6 V	X	See Table 5, Condition B		Shutdown Mode
1.08 V to 1.98 V	GND	X	See Table 5, Condition A		Shutdown Mode
GND	GND	X	See Table 5, Condition A		Shutdown Mode

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.
[2] V_{IL} and V_{IH} are referenced to V_{CCA}. The EN can be controlled by an external device limit of V_{CCA} + 0.3 V.

Table 5. Pin condition

Pin condition	Condition A	Condition B
RST_HOST	100 kΩ pull LOW	100 kΩ pull LOW
CLK_HOST	100 kΩ pull LOW	100 kΩ pull LOW
IO_HOST	5 kΩ pull to V_{CCA}	5 kΩ pull to V_{CCA}
RST_SIM	100 kΩ pull LOW	750 Ω pull LOW
CLK_SIM	100 kΩ pull LOW	750 Ω pull LOW
IO_SIM	High Z	163 Ω pull LOW

Refer to Figure 1.

7.1 Shutdown sequence

The ISO 7816-3 specification specifies the shutdown sequence for the SIM card signals to ensure that the card is properly disabled for power savings. Also during hot swap, the orderly shutdown of these signals helps to avoid any improper write and corruption of data.

When the enable, EN, is asserted LOW, the shutdown sequence is initiated by powering down the RST_SIM channel. Once the RST_SIM channel is powered down, CLK_SIM and IO_SIM are powered down sequentially one-by-one. An internal pull-down resistor on the SIM pins is used to pull these channels LOW. The shutdown sequence is completed in a few microseconds. It is important that EN is pulled LOW before V_{CCA} and V_{CCB} supplies go LOW to ensure that the shutdown sequence is properly initiated.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

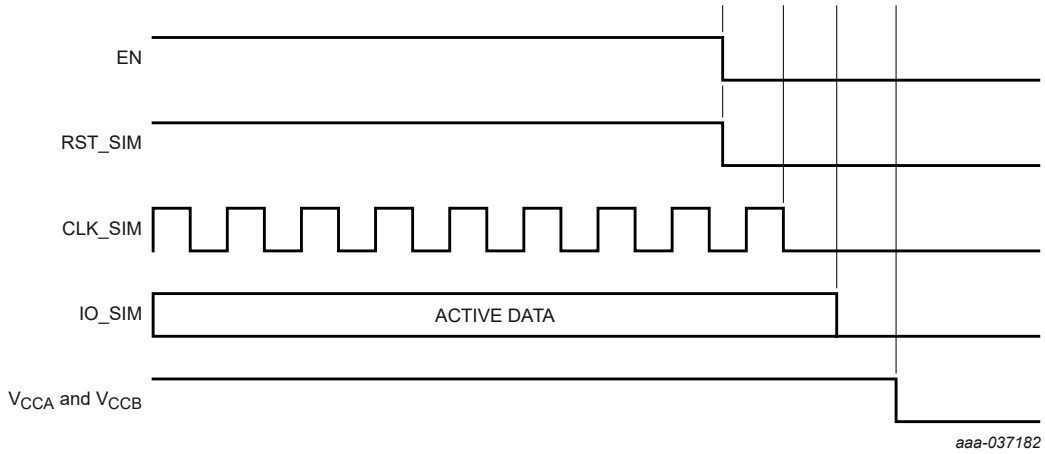
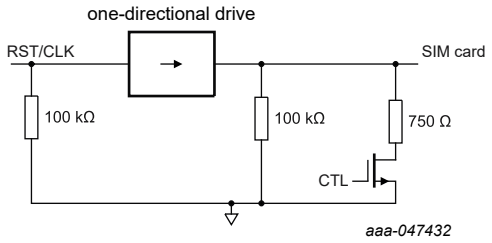


Figure 3. Shutdown sequence for RST_SIM, CLK_SIM, IO_SIM and V_{CCA}/V_{CCB} SIM card translator

7.2 Embedded Enable if Enable is tied to V_{CCA}

The device contains an auto-enable feature. If V_{CCB} rises above V_{CCB_EN}, the level translator logic is enabled automatically. As soon as V_{CCB} drops below the V_{CCB_DIS}, the SIM card side drivers and the level translator logic is disabled. Host side IO pin is configured as input with a 5 kΩ resistor pulled up to V_{CCA}.

When the V_{CCB} drops below V_{CCB_DIS} voltage but is still higher than a Vth MOS threshold (e.g., 0.8 V) the pulldown NMOS in the one-directional drive will be off and NMOS controlled by CTL will be on, and the 750 Ω resistor for CLK/RST and 163 Ω resistor for IO will keep the card side signals low. Additionally the CLK/RST pins on both the Host and Card side have a 100 kΩ pull down resistor. The 163 Ω resistor is used for discharge at power off and the 100 kΩ resister is used for keep RST_SIM/CLK_SIM low when V_{CCB} goes below Vth.



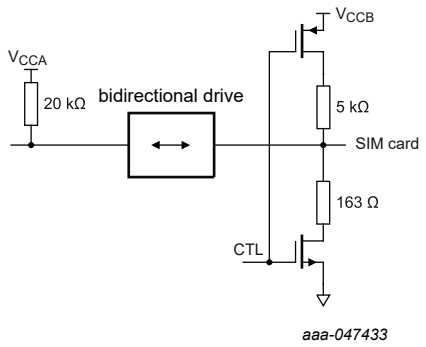
When V_{CCB_EN} = 0 then CTL = V_{CCB} and line is high-Z.

When V_{CCB_EN} = 1 then CTL = GND and line is active.

Figure 4. RST/CLK voltage level translation architecture

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.



When V_{CCB_EN} = 0 then CTL = V_{CCB} and line is high-Z.

When V_{CCB_EN} = 1 then CTL = GND and line is active.

Figure 5. IO voltage level translation architecture

7.3 EMI filter

All input/output driver stages are equipped with EMI filters to reduce interferences towards sensitive mobile communication.

7.4 ESD protection

The device has robust ESD protections on all SIM card pins as well as on the V_{CCB} pin. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

8 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	host supply voltage			GND - 0.5	2.4	V
V_{CCB}	SIM supply voltage			GND - 0.5	4.0	V
$V_{I(CLK\_HOST)}$	input voltage on pin CLK_HOST	input signal voltage, HOST side		GND - 0.5	V_{CCA} + 0.3	V
$V_{I(RST\_HOST)}$	input voltage on pin RST_HOST	input signal voltage, HOST side		GND - 0.5	V_{CCA} + 0.3	V
$V_{I(IO\_HOST)}$	input voltage on pin IO_HOST	input signal voltage, HOST side		GND - 0.5	V_{CCA} + 0.3	V
$V_{I(CLK\_SIM)}$	input voltage on pin CLK_SIM	input signal voltage, SIM side		GND - 0.5	V_{CCB} + 0.3	V
$V_{I(RST\_SIM)}$	input voltage on pin RST_SIM	input signal voltage, SIM side		GND - 0.5	V_{CCB} + 0.3	V
$V_{I(IO\_SIM)}$	input voltage on pin IO_SIM	input signal voltage, SIM side		GND - 0.5	V_{CCB} + 0.3	V
$V_{I(enable)}$	input voltage on enable	input signal voltage, enable		GND - 0.5	V_{CCA} + 0.3	V
T_{stg}	storage temperature			-55	+125	°C
T_{amb}	ambient temperature			-40	+85	°C

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 6. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4, all memory card-side pins, V_{CCB} and GND	[1]			
		contact discharge		-8	+8	kV
		air discharge	[2]	-15	+15	kV
		Human Body Model (HBM) JS-001-2017; all pins		-2000	+2000	V
		Charge Device Model (CDM) JS-002-2018; all pins		-500	+500	V
$I_{lu(IO)}$	input/output latch-up current	JESD 78: -0.5 x V_{CC} < V_I < 1.5 x V_{CC}; T_j = 85 °C		-100	+100	mA

[1] All system level tests are performed with the application-specific capacitors connected to the supply pins V_{SUPPLY}, V_{LDO} and V_{CCA}.

[2] The IEC 61000-4-2 standards are defined so that each level is considered equivalent - a Level 4 contact discharge of 8 kV is considered equivalent to a 15 kV air discharge. Air discharge is provided for information only and was not tested. Per IEC61000-4-2: Contact discharge is the preferred test method, air discharges shall be used where contact discharge cannot be applied. Please refer to AN10897: A guide to designing for ESD and EMC and AN11267: EMC and system level ESD design guidelines for LCD drivers for more information on ESD testing and ESD design techniques.

9 Characteristics

Table 7. Supplies

1.62 V ≤ V_{CCB} ≤ 3.6 V; 1.08 V ≤ V_{CCA} ≤ 1.98 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

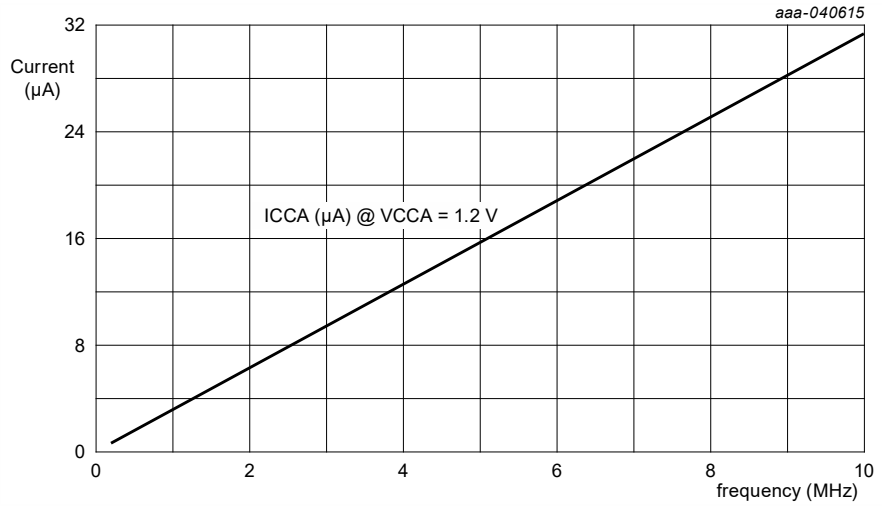
Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{CCA}	supply voltage			1.08	-	1.98	V
I_{CCA}	supply current	operating mode; f_{CLK_HOST} = 1 MHz, EN = V_{CCA}		-	5	10	µA
		Quiescent current; EN = V_{CCA}, IO_HOST = V_{CCA} and CLK_HOST = GND		-	0.01	1	µA
		shutdown mode; EN = GND		-	-	1	µA
V_{CCB}	SIM supply voltage			1.62	-	3.6	V
I_{CCB}	SIM supply current	operating mode; f_{CLK_HOST} = 1 MHz, EN = V_{CCA}, C_l = 50 pF V_{CCB} = 3.6 V		-	300	350	µA
		Quiescent current; EN = V_{CCA}, IO_HOST = V_{CCA} and CLK_HOST = GND		-	3.7	10	µA
		shutdown mode; EN = GND		-	-	3.7	µA
V_I	input voltage	host side	[2]	-0.3	-	V_{CCA} + 0.3	V
		sim card side		-0.3	-	V_{CCB} + 0.3	V
		enable pin		-0.3	-	V_{CCA} + 0.3	V

[1] Typical values measured at 25 °C.

[2] The voltage must not exceed 1.98 V steady state.

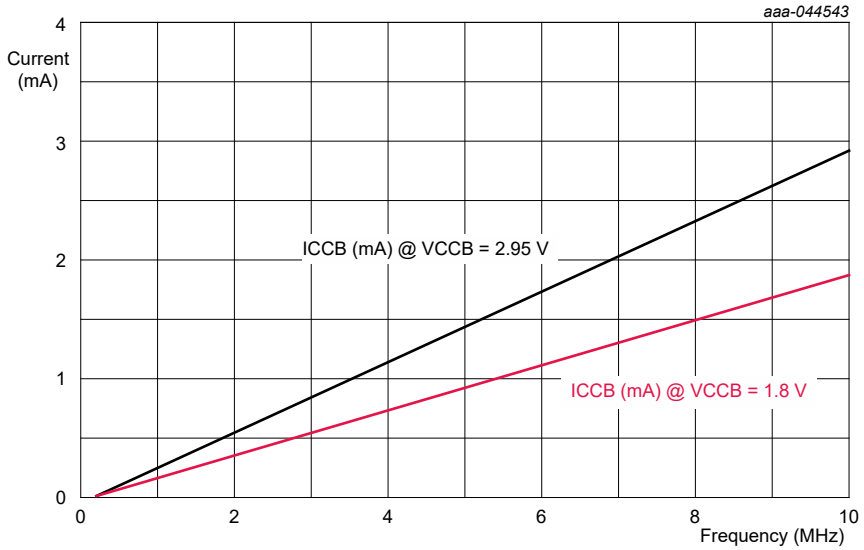
All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.



V_{CCA} = 1.2 V and V_{CCB} = 1.8 V or 2.95 V; C_I = 50 pF

Figure 6. Operating Mode Current over Frequency- Host side



V_{CCA} = 1.2 V and V_{CCB} = 1.8 V or 2.95 V; C_I = 50 pF

Figure 7. Operating Mode Current over Frequency - Card side

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 8. Static characteristics

1.62 V ≤ V_{CCB} ≤ 3.6 V; 1.08 V ≤ V_{CCA} ≤ 1.98 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
Automatic enable feature: V_{CCB}							
V_{CCB_EN}	device enable voltage level	V_{CCA} ≥ 1.0 V, V_{CCB} rising edge		1.62	-	-	V
V_{CCB_DIS}	device disable voltage level	V_{CCA} ≥ 1.0 V, V_{CCB} falling edge		-	-	0.8	V
Hardware enable pin							
V_{IH}	HIGH-level input voltage	EN pin		0.7 × V_{CCA}	-	-	V
V_{IL}	LOW-level input voltage	EN pin		-	-	0.3 × V_{CCA}	V
Level shifter							
V_{IH}	HIGH-level input voltage	IO_HOST, RST_HOST, CLK_HOST					
		1.08 V ≤ V_{CCA} < 1.98 V	[2]	0.65 × V_{CCA}	-	-	V
		IO_SIM	[2]	0.7 × V_{CCB}	-	-	V
V_{IL}	LOW-level input voltage	IO_HOST, RST_HOST, CLK_HOST	[2]	-	-	0.35 × V_{CCA}	V
		IO_SIM	[2]	-	-	0.3 × V_{CCB}	V
R_{PU}	pull-up resistance	IO_SIM connected to V_{CCB}	[3]	3.5	5	7.5	kΩ
		IO_HOST connected to V_{CCA}	[3]	3.5	5	7.5	kΩ
V_{OH}	HIGH-level output voltage	RST_SIM, CLK_SIM; I_{OH} = -1 mA	[2]	0.8 × V_{CCB}	-	V_{CCB}	V
		IO_SIM; I_{OH} = -10 µA	[2]	0.8 × V_{CCB}	-	V_{CCB}	V
		IO_HOST; I_{OH} = -8 µA	[2]	0.8 × V_{CCA}	-	V_{CCA}	V
V_{OL}	LOW-level output voltage	RST_SIM, CLK_SIM; I_{OL} = 1 mA	[2]	0	-	0.125 × V_{CCB}	mV
		IO_SIM; I_{OL} = 1 mA	[2]	0	-	0.125 × V_{CCB}	mV
		IO_HOST; I_{OL} = 1 mA	[2]	0	-	0.25 × V_{CCA}	mV
R_{pd}	pull-down resistance	CLK_HOST/SIM, RST_HOST/SIM		70	100	130	kΩ
EMI filter							
R_s	series resistance	IO_SIM; R1 tolerance ± 30 % [4]	[2]	-	30	-	Ω
		RST_SIM; R1 tolerance ± 30 % [4]		-	30	-	Ω
		CLK_SIM; R1 tolerance ± 30 % [4]	[2]	-	30	-	Ω
C_{io}	input/output capacitance	IO_SIM	[2]	-	8.5	-	pF
		RST_SIM		-	8.5	-	pF
		CLK_SIM	[2]	-	8.5	-	pF

[1] Typical values measured at 25 °C.
[2] V_{IL}, V_{IH} depend on the individual supply voltage per interface.
[3] See Figure 10 for details.
[4] Guaranteed by design

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

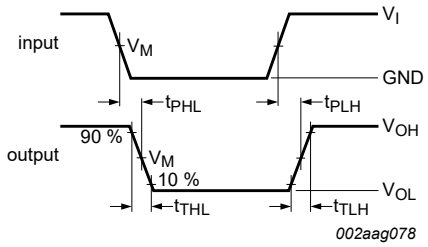
Table 9. Dynamic characteristics

1.62 V ≤ V_{CCB} ≤ 3.6 V; 1.08 V ≤ V_{CCA} ≤ 1.98 V; f_{clk} = f_{io} = 1 MHz; T_{amb} = -40 °C to +85 °C; unless otherwise specified. Refer to Figure 8.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CCA} = 1.8 V; V_{CCB} = 3.0 V; SIM card C_L ≤ 30 pF; host C_L ≤ 10 pF							
t_{PD}	propagation delay	I/O channel; SIM card side to host side		-	8	15	ns
		all channels; host side to SIM card side		-	8	15	ns
t_t	transition time			-	-	10	ns
$t_{sk(o)}$	output skew time	between channels; IO_SIM and CLK_SIM	[1]	-	2	-	ns
f_{clk}	clock frequency	CLK_SIM [2]		-	-	10	MHz
V_{CCA} = 1.2 V; V_{CCB} = 1.8 V; SIM card C_L ≤ 30 pF; host C_L ≤ 10 pF							
t_{PD}	propagation delay	I/O channel; SIM card side to host side		-	15	25	ns
		all channels; host side to SIM card side		-	15	25	ns
t_t	transition time			-	-	10	ns
$t_{sk(o)}$	output skew time	between channels; IO_SIM and CLK_SIM	[1]	-	2	-	ns
f_{clk}	clock frequency	CLK_SIM [2]		-	-	10	MHz

[1] Skew between any two outputs of the same package switching in the same direction with the same C_L.
[2] Guaranteed by design

9.1 Waveforms



Measurement points are given in Table 9.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
t_{PHL} and t_{PLH} are t_{PD} propagation delay; t_{THL} and t_{TLH} are the transition time.

Figure 8. Data input to data output propagation delay times

10 Application information

The application circuit for the NVT4558, which shows the typical interface with a SIM card, is shown in Figure 9.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

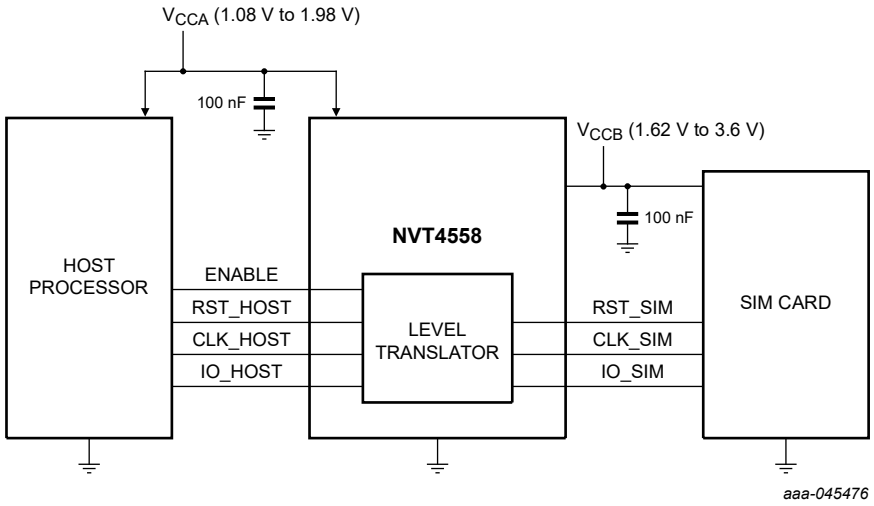


Figure 9. NVT4558 application circuit interfacing with typical SIM card

10.1 Input/output capacitor considerations

It is recommended that a low Equivalent Series Resistance (ESR) 100 nF capacitor is used respectively at V_{CCA} and V_{CCB} input terminals of the device. X5R and X7R type multi-layer ceramic capacitors (MLCC) are preferred because they have minimal variation in value and ESR over temperature. The maximum ESR should be < 500 mΩ (50 mΩ typical).

10.2 Layout consideration

The capacitors should be placed directly at the terminals and ground plane. It is recommended to design the PCB so that the V_{CCA} and V_{CCB} pins are bypassed with a capacitor with each ground returning to a common node at the GND pin of the device such that ground loops are minimized.

Additional information can be found in *AN13158 - NVT4858/NVT4557/NVT4558 voltage-level translator layout guideline* https://www.nxp.com/docs/en/application-note/AN13158.pdf.

10.3 Level translator stage

The architecture of the device I/O channel is shown in Figure 10. The device does not require an extra input signal to control the direction of data flow from host to SIM or from SIM to host. As a change of driving direction is just possible when both sides are in HIGH state, the control logic is recognizing the first falling edge granting it control about the other signal side. During a rising edge signal, the non-driving output is driven by a one-shot circuit to accelerate the rising edge. In case of a communication error or some other unforeseen incident that would drive both connected sides to be drivers at the same time, the internal logic automatically prevents stuck-at situation, so both I/Os will return to HIGH level once released from being driven LOW.

The channels RST and CLK only contain single direction drivers without the direction control mechanism of the I/O channel, as these are only driven from the host to the card side.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

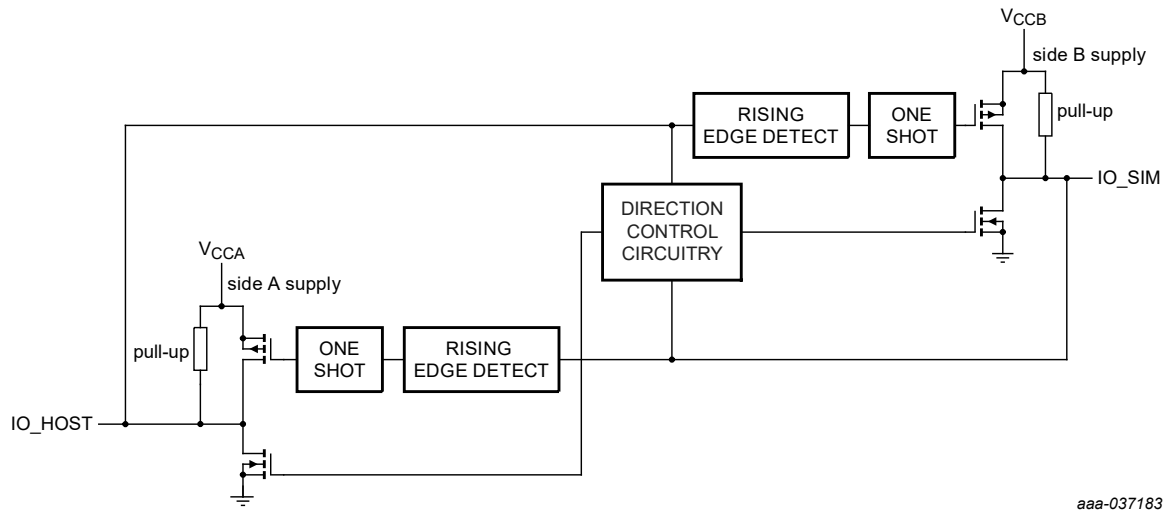


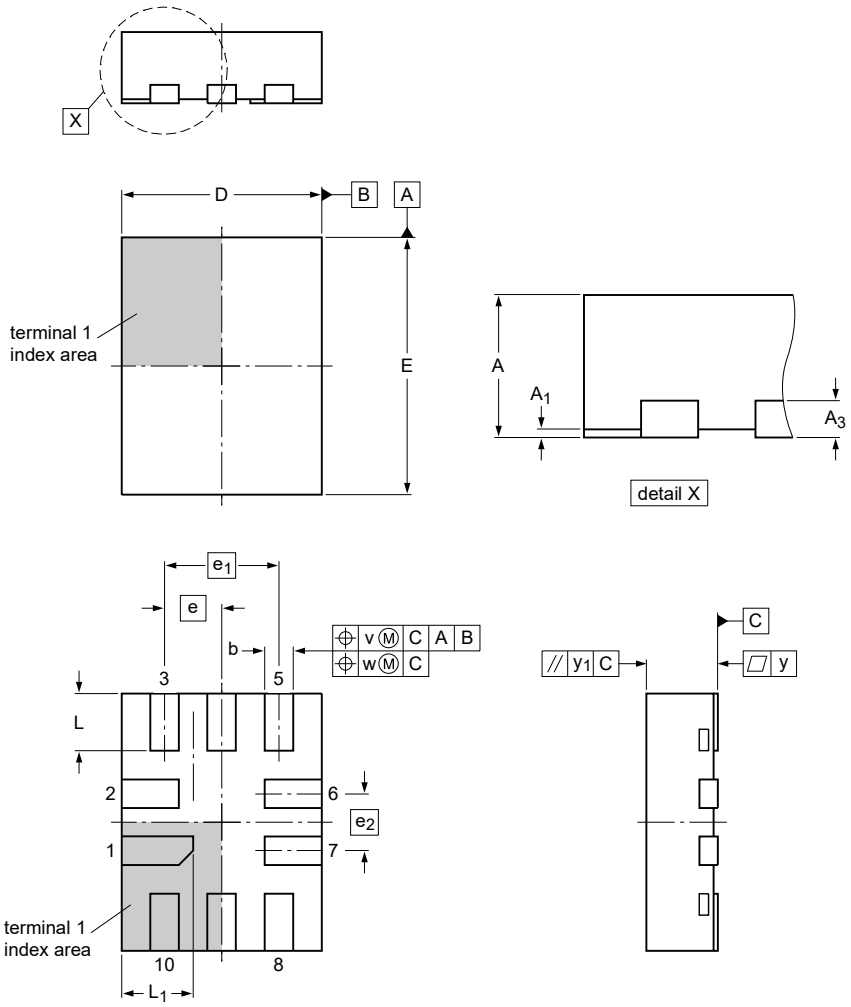
Figure 10. Automatic direction control level translator for HIGH-level direction change interfaces

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

11 Package outline

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm **SOT1160-1**



Dimensions

Unit[1]		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	max	0.50	0.05		0.25	1.5	1.9				0.45	0.55				
	nom	0.45		0.127	0.20	1.4	1.8	0.4	0.8	0.4	0.40	0.50	0.1	0.05	0.05	0.05
	min	0.40	0.00		0.15	1.3	1.7				0.35	0.45				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1160-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1160-1	- - -	- - -	- - -		~~09-12-29~~ 21-01-26

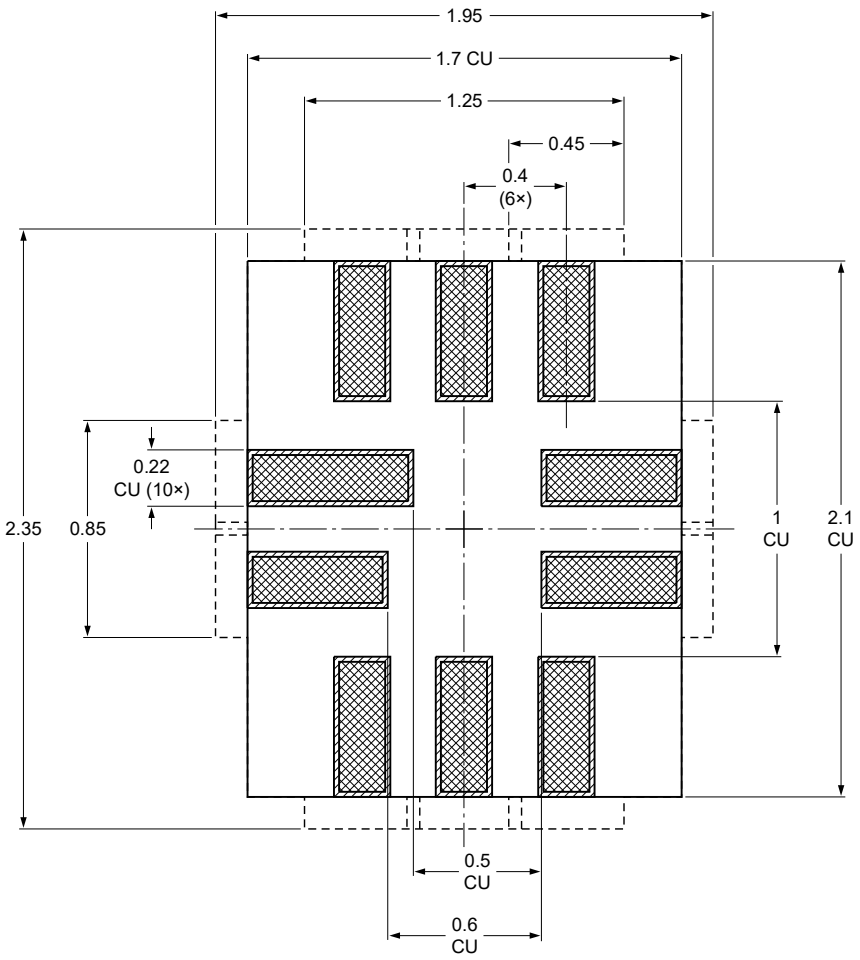
Figure 11. Package outline XQFN10 (SOT1160-1)

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

12 PCB layout

Footprint information for reflow soldering of XQFN10 package **SOT1160-1**



placement area

solder land

solder paste deposit, - 0.02 around copper, stencil thickness 0.1

occupied area

solder land plus solder paste

solder resist, 0.0625 around copper

clearance, 0.125 around occupied area

Dimensions in mm

sot1160-1_fr

Figure 12. SOT1160-1 (XQFN10) footprint information for reflow soldering

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

13 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a SnPb process, thus reducing the process window

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and Table 11

Table 10. SnPb eutectic process (from J-STD-020D)

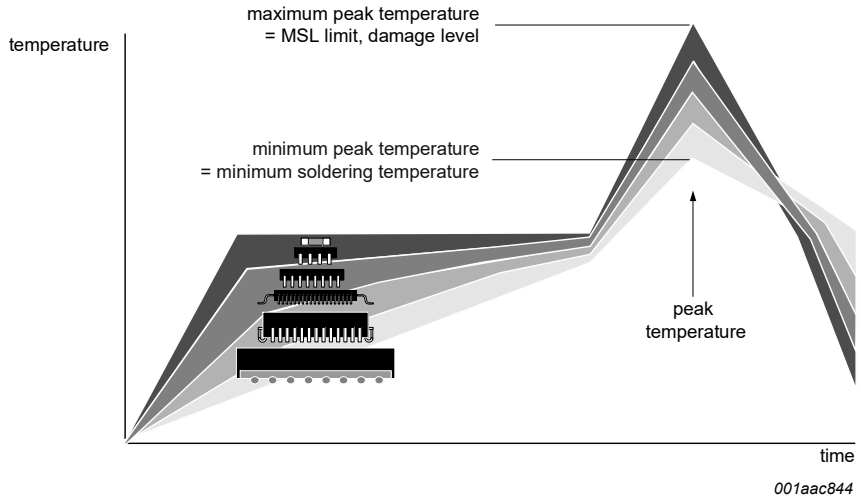
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Figure 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

14 Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DP	Dry Pack
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
HBM	Human Body Model
I/O	Input/Output
LDO	Low DropOut regulator
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal-Oxide Semiconductor
SIM	Subscriber Identification Module

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

15 Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NVT4558 v.1.1	20230906	Product data sheet	-	NVT4558 v.1.0
Modifications:	• Table 7: I_{CCB} shutdown mode max value changed from 1 to 3.7			
NVT4558 v.1.0	20221207	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Tables

Figures

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2023 NXP B.V. **All rights reserved.**

For more information, please visit: http://www.nxp.com

Date of release: 6 September 2023
Document identifier: NVT4558