Revision 1.0.0
ADV Issue Date: 03/06/2024

CUSTOMER ADVISORY

ADV2402

Stratix® 10 Device Datasheet Update

Description:

Intel® is notifying customers of important updates to the Intel® Stratix® 10 Device Datasheet. Below are the most recent updates to the Intel Stratix 10 device datasheet.

- Updated the following diagrams:
  - AS Configuration Serial Output Timing Diagram (Refer to Figure 28 of Page 112)
  - AS Configuration Serial Input Timing Diagram (Refer to Figure 29 of Page 112)
- Updated the Device Datasheet topic:
  - Updated datasheet status for all variant to Final in the Datasheet Status for Intel Stratix 10 Devices table. Removed the footnote on the specifications related to Intel Intellectual Property (IP) products, UPI IP, and DDR-T IP are preliminary. (Refer to Table 2 of Page 4)
  - Removed a note in the Device Datasheet topic. (Refer to Table 64 of Page 64)
- Added a footnote to Recommended Operating Conditions for Intel Stratix 10 Devices table. (Refer to Table 7 of Page 13)
- Removed mentions of GX/SX/MX/TX in Intel Stratix 10 H-Tile devices in table and topic titles. (See Table 10 & 11 of Page 15, Pages 58 and 60 content, Table 67 of Page 66.)
- Removed mentions of GX/SX in Intel Stratix 10 L-Tile devices in table and topic titles. (See Table 8 of Page 14, Table 9 of Page 15, Page49 content, Table 46 of Page 49, Page 52 content.)
- Removed mentions of TX/MX in Intel Stratix 10 E-Tile devices in table and topic titles. (See Table 12 of Page 16.)
- Updated footnote on the data rate for Transceiver Power Supply Operating Conditions for Intel Stratix 10 DX P-Tile Devices table. (Refer to Table 73 of Page 70)
- Added Differential POD12 Standards Specifications for Intel Stratix 10 Devices table. (Refer to Table 24 of Page 27)

- Updated the footnotes in the Differential I/O Standards Specifications for Intel Stratix 10 Devices table. (Refer to footnote 41 and 42 of Page 29)
- Removed the description for H-Tile Transmitter Specifications table.
- Removed the footnote for Intel UPI in the P-Tile PLLA Performance table. (Refer to table 13 of page 17 & table 74 of page 71)
- Added a new diagram RMII TX Timing Diagram in HPS Ethernet Media Access Controller (EMAC) Timing Characteristics topic. (Refer to Figure 14 of Page 90)
- Updated General Configuration Timing Diagram. (Refer to Figure 26 of Page 108)
- Updated table description for AS Timing Parameters for Intel Stratix 10 Devices table. (Refer to description of Table 103 of Page 110)
- Updated table description for Configuration Bit Stream Sizes for Intel Stratix 10 Devices table. (Refer to description of Table 105 of Page 115)
- Updated Programmable IOE Delay for Intel Stratix 10 Devices table. (Refer to Table 106 of Page 116)

The Intel Stratix 10 device datasheet can be found here:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-10/s10_datasheet.pdf

Recommended Action:

Customers are requested to review the change and determine the impact on their designs. Refer to the revision history of the datasheet for a complete list and history of updates.

For question or support, please contact your local Sales representative, or submit a question or request at the My Intel support page, log-in via:
https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Products Affected:

This notification is sent to customers of Intel Stratix 10 devices to ensure access to the latest version of the Intel Stratix 10 datasheet.

Please see the notes columns in the list of affected products (link below) to determine the specific part numbers where the updates apply.

The list of affected part numbers (OPNs) can be downloaded in Excel form:

https://cdrdv2.intel.com/v1/dl/getContent/817495

Change Implementation:

Table 1:

Milestones	Availability
Availability of Intel® Stratix® 10 Device Datasheet Update	Now

Contact:

For more information, please contact your local Sales representative, or submit a question or request at the My Intel support page, log-in via:
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Revision History:

Date	Rev	Description
03/6/2022	1.0.0	Initial Release