## AUTOMOTIVE, 105°C OPERATION, 10 V, SENSE-INPUT VOLTAGE DETECTOR

**Rev.1.3**$_{00}$

The S-19102/19108 Series is a high-accuracy voltage detector developed using CMOS technology. The detection voltage is fixed internally with an accuracy of ±3.5% (−$V_{DET(S)}$ ≥ 2.2 V). It operates with current consumption of 500 nA typ.
Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared, so the output is stable even if the SENSE pin falls to 0 V.
Two output forms Nch open-drain output and CMOS output are available.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
For more information regarding our FIT rate calculation, contact our sales representatives.

**Caution  This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

## ■ Features

- Detection voltage:            1.0 V to 5.0 V (0.1 V step)
- Detection voltage accuracy:   ±3.5% (2.2 V ≤ −$V_{DET(S)}$ ≤ 5.0 V, Ta = −40°C to +105°C)
                                ±(2.5% + 22 mV) (1.0 V ≤ −$V_{DET(S)}$ < 2.2 V, Ta = −40°C to +105°C)
- Current consumption:          500 nA typ.
- Operation voltage range:      0.95 V to 10.0 V
- Hysteresis width:             5% ± 2% (Ta = −40°C to +105°C)
- Output form:                  Nch open-drain output (Active "L")
                                CMOS output (Active "L")
- Operation temperature range:  Ta = −40°C to +105°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified[1]

   **[1].**   Contact our sales representatives for details.
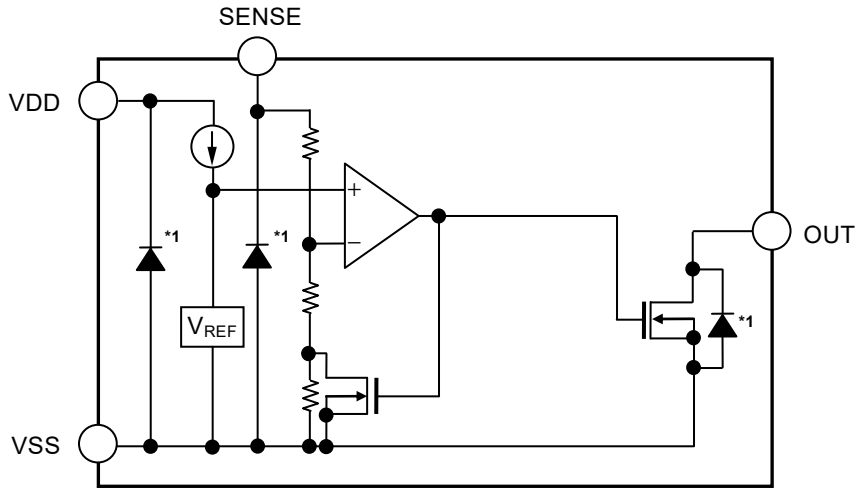
## ■ Applications

- For automotive use (accessory, car navigation system, car audio system, etc.)

## ■ Package

- SOT-23-5

# ■ Block Diagrams

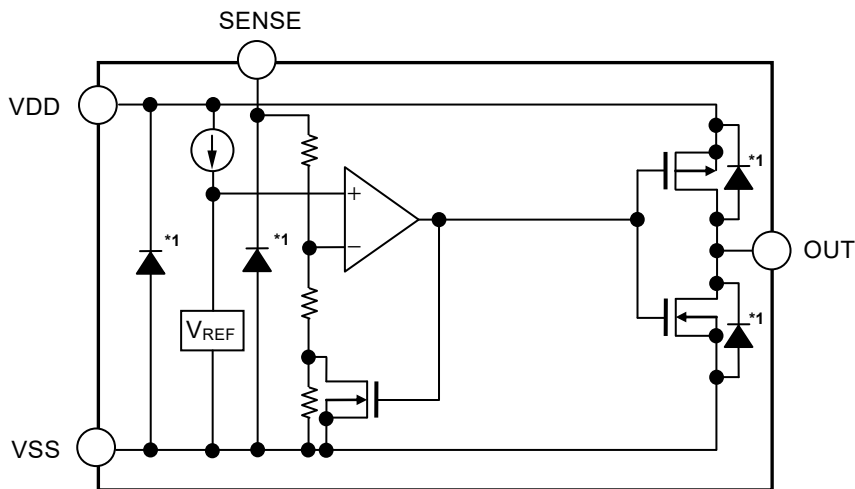### 1. S-19102/19108 Series N type (Nch open-drain output)

| Function | Status |
|---|---|
| Output logic | Active "L" |



**\*1.** Parasitic diode

**Figure 1**

### 2. S-19102/19108 Series C type (CMOS output)

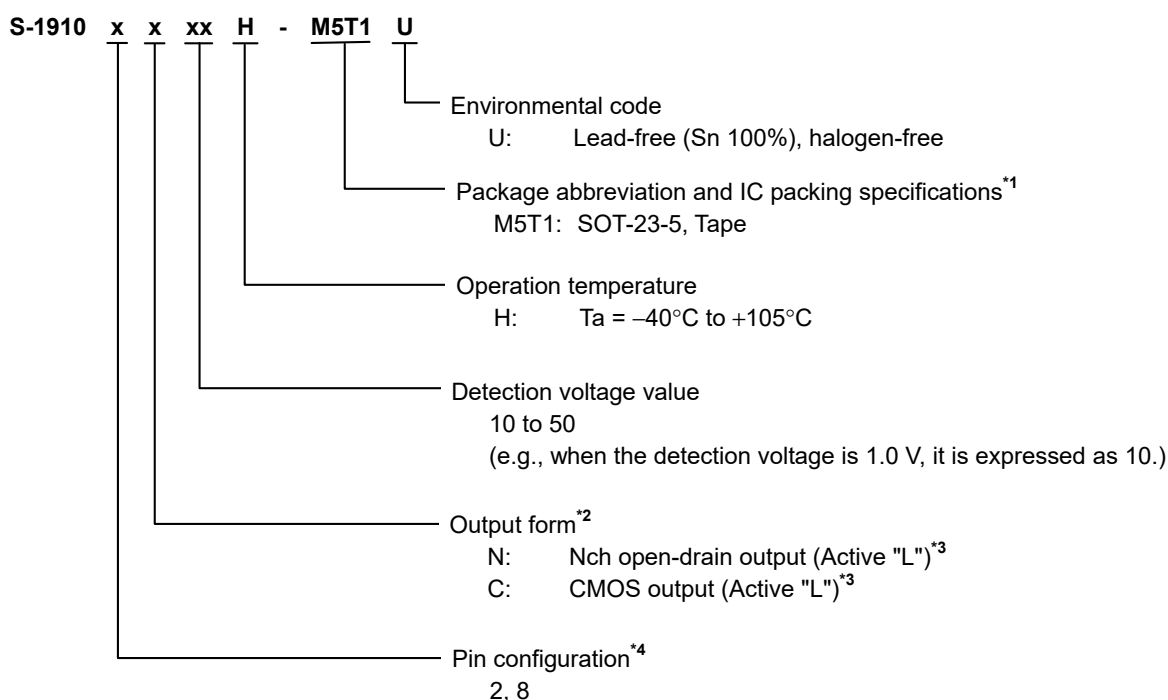| Function | Status |
|---|---|
| Output logic | Active "L" |



**\*1.** Parasitic diode

**Figure 2**

# ■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 2.
Contact our sales representatives for details of AEC-Q100 reliability specification.

# ■ Product Name Structure

Users can select the output form and detection voltage value for the S-19102/19108 Series.
Refer to "**1.   Product name**" regarding the contents of product name, "**2.   Function list of product types**" regarding the product types, "**3.   Package**" regarding the package drawings and "**4.   Product name list**" regarding details of product name.

## 1.   Product name

S-1910   x   x   xx   H   -   **M5T1**   U

Environmental code
    U:    Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications[1]
    M5T1:  SOT-23-5, Tape

Operation temperature
    H:    Ta = −40°C to +105°C

Detection voltage value
    10 to 50
    (e.g., when the detection voltage is 1.0 V, it is expressed as 10.)

Output form[2]
    N:    Nch open-drain output (Active "L")[3]
    C:    CMOS output (Active "L")[3]

Pin configuration[4]
    2, 8

**\*1.**   Refer to the tape drawing.
**\*2.**   Refer to "**2.   Function list of product types**".
**\*3.**   If you request the product with output logic active "H", contact our sales representatives.
**\*4.**   Refer to "**■ Pin Configurations**".

## 2.   Function list of product types

**Table 1**

| Product Type | Output Form | Output Logic | Package |
|---|---|---|---|
| N | Nch open-drain output | Active "L" | SOT-23-5 |
| C | CMOS output | Active "L" | SOT-23-5 |

## 3.   Package

**Table 2   Package Drawing Codes**

| Package Name | Dimension | Tape | Reel |
|---|---|---|---|
| SOT-23-5 | MP005-A-P-SD | MP005-A-C-SD | MP005-A-R-SD |

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## 4. Product name list

### 4. 1　S-19102 Series N type

Output form: Nch open-drain output (Active "L")

**Table 3**

| Detection Voltage | SOT-23-5 |
| --- | --- |
| 1.0 V ± (2.5% + 22 mV) | S-19102N10H-M5T1U |
| 1.1 V ± (2.5% + 22 mV) | S-19102N11H-M5T1U |
| 1.2 V ± (2.5% + 22 mV) | S-19102N12H-M5T1U |
| 1.3 V ± (2.5% + 22 mV) | S-19102N13H-M5T1U |
| 1.4 V ± (2.5% + 22 mV) | S-19102N14H-M5T1U |
| 1.5 V ± (2.5% + 22 mV) | S-19102N15H-M5T1U |
| 1.6 V ± (2.5% + 22 mV) | S-19102N16H-M5T1U |
| 1.7 V ± (2.5% + 22 mV) | S-19102N17H-M5T1U |
| 1.8 V ± (2.5% + 22 mV) | S-19102N18H-M5T1U |
| 1.9 V ± (2.5% + 22 mV) | S-19102N19H-M5T1U |
| 2.0 V ± (2.5% + 22 mV) | S-19102N20H-M5T1U |
| 2.1 V ± (2.5% + 22 mV) | S-19102N21H-M5T1U |
| 2.2 V ± 3.5% | S-19102N22H-M5T1U |
| 2.3 V ± 3.5% | S-19102N23H-M5T1U |
| 2.4 V ± 3.5% | S-19102N24H-M5T1U |
| 2.5 V ± 3.5% | S-19102N25H-M5T1U |
| 2.6 V ± 3.5% | S-19102N26H-M5T1U |
| 2.7 V ± 3.5% | S-19102N27H-M5T1U |
| 2.8 V ± 3.5% | S-19102N28H-M5T1U |
| 2.9 V ± 3.5% | S-19102N29H-M5T1U |
| 3.0 V ± 3.5% | S-19102N30H-M5T1U |
| 3.1 V ± 3.5% | S-19102N31H-M5T1U |
| 3.2 V ± 3.5% | S-19102N32H-M5T1U |
| 3.3 V ± 3.5% | S-19102N33H-M5T1U |
| 3.4 V ± 3.5% | S-19102N34H-M5T1U |
| 3.5 V ± 3.5% | S-19102N35H-M5T1U |
| 3.6 V ± 3.5% | S-19102N36H-M5T1U |
| 3.7 V ± 3.5% | S-19102N37H-M5T1U |
| 3.8 V ± 3.5% | S-19102N38H-M5T1U |
| 3.9 V ± 3.5% | S-19102N39H-M5T1U |
| 4.0 V ± 3.5% | S-19102N40H-M5T1U |
| 4.1 V ± 3.5% | S-19102N41H-M5T1U |
| 4.2 V ± 3.5% | S-19102N42H-M5T1U |
| 4.3 V ± 3.5% | S-19102N43H-M5T1U |
| 4.4 V ± 3.5% | S-19102N44H-M5T1U |
| 4.5 V ± 3.5% | S-19102N45H-M5T1U |
| 4.6 V ± 3.5% | S-19102N46H-M5T1U |
| 4.7 V ± 3.5% | S-19102N47H-M5T1U |
| 4.8 V ± 3.5% | S-19102N48H-M5T1U |
| 4.9 V ± 3.5% | S-19102N49H-M5T1U |
| 5.0 V ± 3.5% | S-19102N50H-M5T1U |

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### 4. 2 S-19102 Series C type

Output form: CMOS output (Active "L")

**Table 4**

| Detection Voltage | SOT-23-5 |
|---|---|
| 1.0 V ± (2.5% + 22 mV) | S-19102C10H-M5T1U |
| 1.1 V ± (2.5% + 22 mV) | S-19102C11H-M5T1U |
| 1.2 V ± (2.5% + 22 mV) | S-19102C12H-M5T1U |
| 1.3 V ± (2.5% + 22 mV) | S-19102C13H-M5T1U |
| 1.4 V ± (2.5% + 22 mV) | S-19102C14H-M5T1U |
| 1.5 V ± (2.5% + 22 mV) | S-19102C15H-M5T1U |
| 1.6 V ± (2.5% + 22 mV) | S-19102C16H-M5T1U |
| 1.7 V ± (2.5% + 22 mV) | S-19102C17H-M5T1U |
| 1.8 V ± (2.5% + 22 mV) | S-19102C18H-M5T1U |
| 1.9 V ± (2.5% + 22 mV) | S-19102C19H-M5T1U |
| 2.0 V ± (2.5% + 22 mV) | S-19102C20H-M5T1U |
| 2.1 V ± (2.5% + 22 mV) | S-19102C21H-M5T1U |
| 2.2 V ± 3.5% | S-19102C22H-M5T1U |
| 2.3 V ± 3.5% | S-19102C23H-M5T1U |
| 2.4 V ± 3.5% | S-19102C24H-M5T1U |
| 2.5 V ± 3.5% | S-19102C25H-M5T1U |
| 2.6 V ± 3.5% | S-19102C26H-M5T1U |
| 2.7 V ± 3.5% | S-19102C27H-M5T1U |
| 2.8 V ± 3.5% | S-19102C28H-M5T1U |
| 2.9 V ± 3.5% | S-19102C29H-M5T1U |
| 3.0 V ± 3.5% | S-19102C30H-M5T1U |
| 3.1 V ± 3.5% | S-19102C31H-M5T1U |
| 3.2 V ± 3.5% | S-19102C32H-M5T1U |
| 3.3 V ± 3.5% | S-19102C33H-M5T1U |
| 3.4 V ± 3.5% | S-19102C34H-M5T1U |
| 3.5 V ± 3.5% | S-19102C35H-M5T1U |
| 3.6 V ± 3.5% | S-19102C36H-M5T1U |
| 3.7 V ± 3.5% | S-19102C37H-M5T1U |
| 3.8 V ± 3.5% | S-19102C38H-M5T1U |
| 3.9 V ± 3.5% | S-19102C39H-M5T1U |
| 4.0 V ± 3.5% | S-19102C40H-M5T1U |
| 4.1 V ± 3.5% | S-19102C41H-M5T1U |
| 4.2 V ± 3.5% | S-19102C42H-M5T1U |
| 4.3 V ± 3.5% | S-19102C43H-M5T1U |
| 4.4 V ± 3.5% | S-19102C44H-M5T1U |
| 4.5 V ± 3.5% | S-19102C45H-M5T1U |
| 4.6 V ± 3.5% | S-19102C46H-M5T1U |
| 4.7 V ± 3.5% | S-19102C47H-M5T1U |
| 4.8 V ± 3.5% | S-19102C48H-M5T1U |
| 4.9 V ± 3.5% | S-19102C49H-M5T1U |
| 5.0 V ± 3.5% | S-19102C50H-M5T1U |

### 4. 3   S-19108 Series N type

Output form: Nch open-drain output (Active "L")

**Table 5**

| Detection Voltage | SOT-23-5 |
|---|---|
| 1.0 V ± (2.5% + 22 mV) | S-19108N10H-M5T1U |
| 1.1 V ± (2.5% + 22 mV) | S-19108N11H-M5T1U |
| 1.2 V ± (2.5% + 22 mV) | S-19108N12H-M5T1U |
| 1.3 V ± (2.5% + 22 mV) | S-19108N13H-M5T1U |
| 1.4 V ± (2.5% + 22 mV) | S-19108N14H-M5T1U |
| 1.5 V ± (2.5% + 22 mV) | S-19108N15H-M5T1U |
| 1.6 V ± (2.5% + 22 mV) | S-19108N16H-M5T1U |
| 1.7 V ± (2.5% + 22 mV) | S-19108N17H-M5T1U |
| 1.8 V ± (2.5% + 22 mV) | S-19108N18H-M5T1U |
| 1.9 V ± (2.5% + 22 mV) | S-19108N19H-M5T1U |
| 2.0 V ± (2.5% + 22 mV) | S-19108N20H-M5T1U |
| 2.1 V ± (2.5% + 22 mV) | S-19108N21H-M5T1U |
| 2.2 V ± 3.5% | S-19108N22H-M5T1U |
| 2.3 V ± 3.5% | S-19108N23H-M5T1U |
| 2.4 V ± 3.5% | S-19108N24H-M5T1U |
| 2.5 V ± 3.5% | S-19108N25H-M5T1U |
| 2.6 V ± 3.5% | S-19108N26H-M5T1U |
| 2.7 V ± 3.5% | S-19108N27H-M5T1U |
| 2.8 V ± 3.5% | S-19108N28H-M5T1U |
| 2.9 V ± 3.5% | S-19108N29H-M5T1U |
| 3.0 V ± 3.5% | S-19108N30H-M5T1U |
| 3.1 V ± 3.5% | S-19108N31H-M5T1U |
| 3.2 V ± 3.5% | S-19108N32H-M5T1U |
| 3.3 V ± 3.5% | S-19108N33H-M5T1U |
| 3.4 V ± 3.5% | S-19108N34H-M5T1U |
| 3.5 V ± 3.5% | S-19108N35H-M5T1U |
| 3.6 V ± 3.5% | S-19108N36H-M5T1U |
| 3.7 V ± 3.5% | S-19108N37H-M5T1U |
| 3.8 V ± 3.5% | S-19108N38H-M5T1U |
| 3.9 V ± 3.5% | S-19108N39H-M5T1U |
| 4.0 V ± 3.5% | S-19108N40H-M5T1U |
| 4.1 V ± 3.5% | S-19108N41H-M5T1U |
| 4.2 V ± 3.5% | S-19108N42H-M5T1U |
| 4.3 V ± 3.5% | S-19108N43H-M5T1U |
| 4.4 V ± 3.5% | S-19108N44H-M5T1U |
| 4.5 V ± 3.5% | S-19108N45H-M5T1U |
| 4.6 V ± 3.5% | S-19108N46H-M5T1U |
| 4.7 V ± 3.5% | S-19108N47H-M5T1U |
| 4.8 V ± 3.5% | S-19108N48H-M5T1U |
| 4.9 V ± 3.5% | S-19108N49H-M5T1U |
| 5.0 V ± 3.5% | S-19108N50H-M5T1U |

### 4. 4   S-19108 Series C type

Output form: CMOS output (Active "L")

**Table 6**

| Detection Voltage | SOT-23-5 |
|---|---|
| 1.0 V ± (2.5% + 22 mV) | S-19108C10H-M5T1U |
| 1.1 V ± (2.5% + 22 mV) | S-19108C11H-M5T1U |
| 1.2 V ± (2.5% + 22 mV) | S-19108C12H-M5T1U |
| 1.3 V ± (2.5% + 22 mV) | S-19108C13H-M5T1U |
| 1.4 V ± (2.5% + 22 mV) | S-19108C14H-M5T1U |
| 1.5 V ± (2.5% + 22 mV) | S-19108C15H-M5T1U |
| 1.6 V ± (2.5% + 22 mV) | S-19108C16H-M5T1U |
| 1.7 V ± (2.5% + 22 mV) | S-19108C17H-M5T1U |
| 1.8 V ± (2.5% + 22 mV) | S-19108C18H-M5T1U |
| 1.9 V ± (2.5% + 22 mV) | S-19108C19H-M5T1U |
| 2.0 V ± (2.5% + 22 mV) | S-19108C20H-M5T1U |
| 2.1 V ± (2.5% + 22 mV) | S-19108C21H-M5T1U |
| 2.2 V ± 3.5% | S-19108C22H-M5T1U |
| 2.3 V ± 3.5% | S-19108C23H-M5T1U |
| 2.4 V ± 3.5% | S-19108C24H-M5T1U |
| 2.5 V ± 3.5% | S-19108C25H-M5T1U |
| 2.6 V ± 3.5% | S-19108C26H-M5T1U |
| 2.7 V ± 3.5% | S-19108C27H-M5T1U |
| 2.8 V ± 3.5% | S-19108C28H-M5T1U |
| 2.9 V ± 3.5% | S-19108C29H-M5T1U |
| 3.0 V ± 3.5% | S-19108C30H-M5T1U |
| 3.1 V ± 3.5% | S-19108C31H-M5T1U |
| 3.2 V ± 3.5% | S-19108C32H-M5T1U |
| 3.3 V ± 3.5% | S-19108C33H-M5T1U |
| 3.4 V ± 3.5% | S-19108C34H-M5T1U |
| 3.5 V ± 3.5% | S-19108C35H-M5T1U |
| 3.6 V ± 3.5% | S-19108C36H-M5T1U |
| 3.7 V ± 3.5% | S-19108C37H-M5T1U |
| 3.8 V ± 3.5% | S-19108C38H-M5T1U |
| 3.9 V ± 3.5% | S-19108C39H-M5T1U |
| 4.0 V ± 3.5% | S-19108C40H-M5T1U |
| 4.1 V ± 3.5% | S-19108C41H-M5T1U |
| 4.2 V ± 3.5% | S-19108C42H-M5T1U |
| 4.3 V ± 3.5% | S-19108C43H-M5T1U |
| 4.4 V ± 3.5% | S-19108C44H-M5T1U |
| 4.5 V ± 3.5% | S-19108C45H-M5T1U |
| 4.6 V ± 3.5% | S-19108C46H-M5T1U |
| 4.7 V ± 3.5% | S-19108C47H-M5T1U |
| 4.8 V ± 3.5% | S-19108C48H-M5T1U |
| 4.9 V ± 3.5% | S-19108C49H-M5T1U |
| 5.0 V ± 3.5% | S-19108C50H-M5T1U |

## ■ Pin Configurations

### 1. S-19102 Series

#### 1. 1 SOT-23-5

Top view
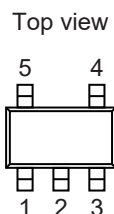


**Figure 3**

**Table 7**

| Pin No. | Symbol | Description |
|---------|--------|-------------|
| 1 | OUT | Voltage detection output pin |
| 2 | VDD | Power supply pin |
| 3 | VSS | GND pin |
| 4 | NC*1 | No connection |
| 5 | SENSE | Detection voltage input pin |

**\*1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

### 2. S-19108 Series

#### 2. 1 SOT-23-5

Top view
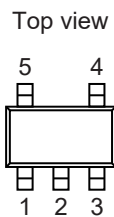


**Figure 4**

**Table 8**

| Pin No. | Symbol | Description |
|---------|--------|-------------|
| 1 | OUT | Voltage detection output pin |
| 2 | VSS | GND pin |
| 3 | VDD | Power supply pin |
| 4 | SENSE | Detection voltage input pin |
| 5 | NC*1 | No connection |

**\*1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

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## ■ Absolute Maximum Ratings

**Table 9**

(Ta = −40°C to +105°C unless otherwise specified)

| Item | | Symbol | Absolute Maximum Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | | $V_{DD} - V_{SS}$ | 12.0 | V |
| SENSE pin input voltage | | $V_{SENSE}$ | $V_{SS} - 0.3$ to 12.0 | V |
| Output voltage | Nch open-drain output product | $V_{OUT}$ | $V_{SS} - 0.3$ to 12.0 | V |
| | CMOS output product | | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| Output current | | $I_{OUT}$ | 50 | mA |
| Operation ambient temperature | | $T_{opr}$ | −40 to +105 | °C |
| Storage temperature | | $T_{stg}$ | −40 to +125 | °C |

**Caution** **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

## ■ Thermal Resistance Value

**Table 10**

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Junction-to-ambient thermal resistance[1] | $\theta_{JA}$ | SOT-23-5 | Board A | – | 192 | – | °C/W |
| | | | Board B | – | 160 | – | °C/W |
| | | | Board C | – | – | – | °C/W |
| | | | Board D | – | – | – | °C/W |
| | | | Board E | – | – | – | °C/W |

**[1].** Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

## ■ Electrical Characteristics

### 1. Nch open-drain output product

**Table 11**

(Ta = −40°C to +105°C unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage[*1] | −$V_{DET}$ | 0.95 V ≤ $V_{DD}$ ≤ 10.0 V | 1.0 V ≤ −$V_{DET(S)}$ < 2.2 V | −$V_{DET(S)}$ × 0.975 − 0.022 | −$V_{DET(S)}$ | −$V_{DET(S)}$ × 1.025 + 0.022 | V | 1 |
| | | | 2.2 V ≤ −$V_{DET(S)}$ ≤ 5.0 V | −$V_{DET(S)}$ × 0.965 | −$V_{DET(S)}$ | −$V_{DET(S)}$ × 1.035 | V | 1 |
| Hysteresis width | $V_{HYS}$ | – | | −$V_{DET}$ × 0.03 | −$V_{DET}$ × 0.05 | −$V_{DET}$ × 0.07 | V | 1 |
| Current consumption[*2] | $I_{SS}$ | $V_{DD}$ = 10.0 V, $V_{SENSE}$ = −$V_{DET(S)}$ + 1.0 V | | – | 0.50 | 0.90 | μA | 2 |
| Operation voltage | $V_{DD}$ | – | | 0.95 | – | 10.0 | V | 1 |
| Output current | $I_{OUT}$ | Output transistor Nch $V_{DS}$[*3] = 0.5 V $V_{SENSE}$ = 0.0 V | $V_{DD}$ = 0.95 V | 0.50 | 1.00 | – | mA | 3 |
| | | | $V_{DD}$ = 1.2 V | 0.73 | 1.33 | – | mA | 3 |
| | | | $V_{DD}$ = 2.4 V | 1.17 | 2.39 | – | mA | 3 |
| | | | $V_{DD}$ = 4.8 V | 1.49 | 2.50 | – | mA | 3 |
| Leakage current | $I_{LEAK}$ | Output transistor Nch $V_{DD}$ = 10.0 V, $V_{DS}$[*3] = 10.0 V, $V_{SENSE}$ = 10.0 V | | – | – | 1.2 | μA | 3 |
| Detection delay time[*4] | $t_{DET}$ | $V_{DD}$ = 5.0 V | | – | 40 | – | μs | 4 |
| Release delay time[*5] | $t_{RESET}$ | $V_{DD}$ = 5.0 V | −$V_{DET(S)}$ ≤ 2.4 V | – | 40 | – | μs | 4 |
| | | | 2.4 V < −$V_{DET(S)}$ | – | 80 | – | μs | 4 |
| SENSE pin resistance | $R_{SENSE}$ | 1.0 V ≤ −$V_{DET(S)}$ < 1.2 V | | 4.0 | 19.0 | 72.0 | MΩ | 2 |
| | | 1.2 V ≤ −$V_{DET(S)}$ ≤ 5.0 V | | 4.8 | 30.0 | 189.0 | MΩ | 2 |

**\*1.** −$V_{DET}$: Actual detection voltage value, −$V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 3** or **Table 5**)

**\*2.** The current flowing through the SENSE pin resistance is not included.

**\*3.** $V_{DS}$: Drain-to-source voltage of the output transistor

**\*4.** The time period from when the pulse voltage of 6.0 V → −$V_{DET(S)}$ − 2.0 V or 0 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2, after the output pin is pulled up to 5.0 V by the resistance of 470 kΩ.

**\*5.** The time period from when the pulse voltage of 0 V → −$V_{DET(S)}$ + 2.0 V or 6.0 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2, after the output pin is pulled up to 5.0 V by the resistance of 470 kΩ.

## 2. CMOS output product

**Table 12**

(Ta = −40°C to +105°C unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage[*1] | $-V_{DET}$ | 0.95 V ≤ $V_{DD}$ ≤ 10.0 V | 1.0 V ≤ $-V_{DET(S)}$ < 2.2 V | $-V_{DET(S)}$ × 0.975 − 0.022 | $-V_{DET(S)}$ | $-V_{DET(S)}$ × 1.025 + 0.022 | V | 1 |
| | | | 2.2 V ≤ $-V_{DET(S)}$ ≤ 5.0 V | $-V_{DET(S)}$ × 0.965 | $-V_{DET(S)}$ | $-V_{DET(S)}$ × 1.035 | V | 1 |
| Hysteresis width | $V_{HYS}$ | − | | $-V_{DET}$ × 0.03 | $-V_{DET}$ × 0.05 | $-V_{DET}$ × 0.07 | V | 1 |
| Current consumption[*2] | $I_{SS}$ | $V_{DD}$ = 10.0 V, $V_{SENSE}$ = $-V_{DET(S)}$ + 1.0 V | | − | 0.50 | 2.10 | µA | 2 |
| Operation voltage | $V_{DD}$ | − | | 0.95 | − | 10.0 | V | 1 |
| Output current | $I_{OUT}$ | Output transistor Nch $V_{DS}$[*3] = 0.5 V $V_{SENSE}$ = 0.0 V | $V_{DD}$ = 0.95 V | 0.50 | 1.00 | − | mA | 3 |
| | | | $V_{DD}$ = 1.2 V | 0.73 | 1.33 | − | mA | 3 |
| | | | $V_{DD}$ = 2.4 V | 1.17 | 2.39 | − | mA | 3 |
| | | | $V_{DD}$ = 4.8 V | 1.49 | 2.50 | − | mA | 3 |
| | | Output transistor Pch $V_{DS}$[*3] = 0.5 V $V_{SENSE}$ = 10.0 V | $V_{DD}$ = 4.8 V | 1.62 | 2.60 | − | mA | 5 |
| | | | $V_{DD}$ = 6.0 V | 1.78 | 2.86 | − | mA | 5 |
| Detection delay time[*4] | $t_{DET}$ | $V_{DD}$ = 5.0 V | | − | 40 | − | µs | 4 |
| Release delay time[*5] | $t_{RESET}$ | $V_{DD}$ = 5.0 V | $-V_{DET(S)}$ ≤ 2.4 V | − | 40 | − | µs | 4 |
| | | | 2.4 V < $-V_{DET(S)}$ | − | 80 | − | µs | 4 |
| SENSE pin resistance | $R_{SENSE}$ | 1.0 V ≤ $-V_{DET(S)}$ < 1.2 V | | 4.0 | 19.0 | 72.0 | MΩ | 2 |
| | | 1.2 V ≤ $-V_{DET(S)}$ ≤ 5.0 V | | 4.8 | 30.0 | 189.0 | MΩ | 2 |

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 4** or **Table 6**)

***2.** The current flowing through the SENSE pin resistance is not included.

***3.** $V_{DS}$: Drain-to-source voltage of the output transistor

***4.** The time period from when the pulse voltage of 6.0 V → $-V_{DET(S)}$ − 2.0 V or 0 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2.

***5.** The time period from when the pulse voltage of 0 V → $-V_{DET(S)}$ + 2.0 V or 6.0 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2.

## ■ Test Circuits
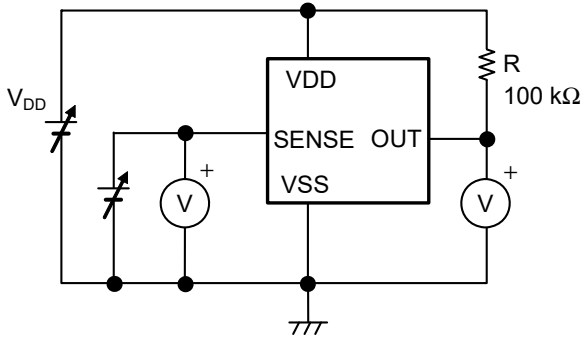
**Figure 5    Test Circuit 1**
**(Nch open-drain output product)**
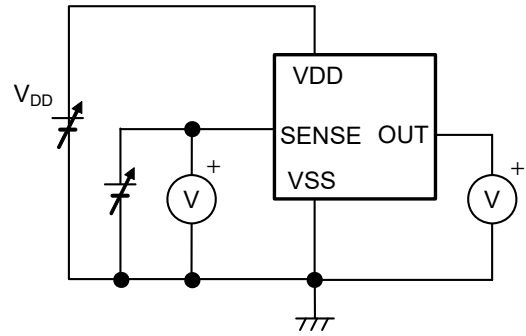
**Figure 6    Test Circuit 1**
**(CMOS output product)**
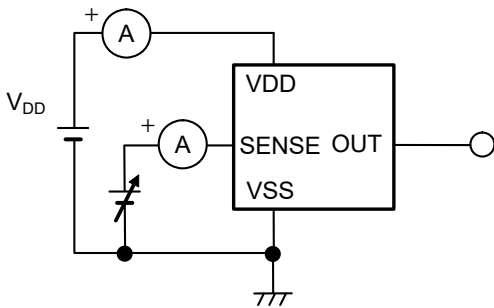
**Figure 7    Test Circuit 2**
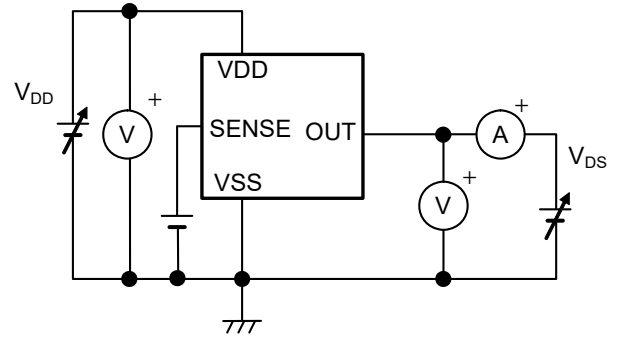
**Figure 8    Test Circuit 3**
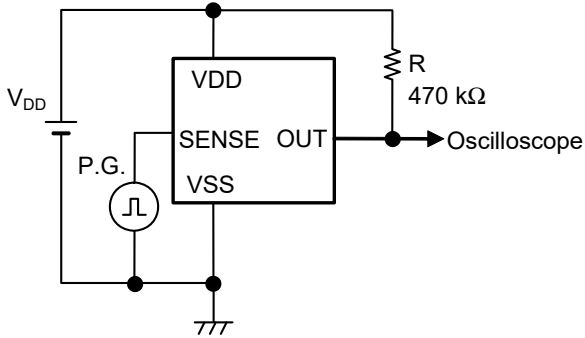
**Figure 9    Test Circuit 4**
**(Nch open-drain output product)**
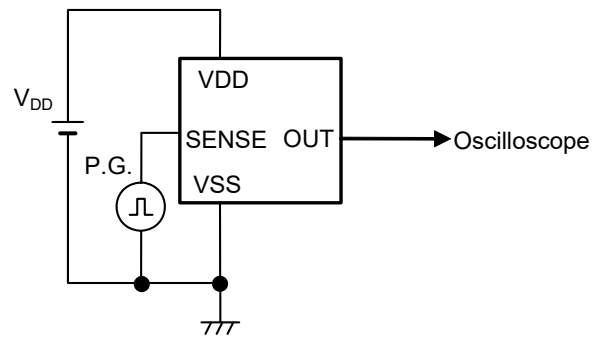
**Figure 10    Test Circuit 4**
**(CMOS output product)**
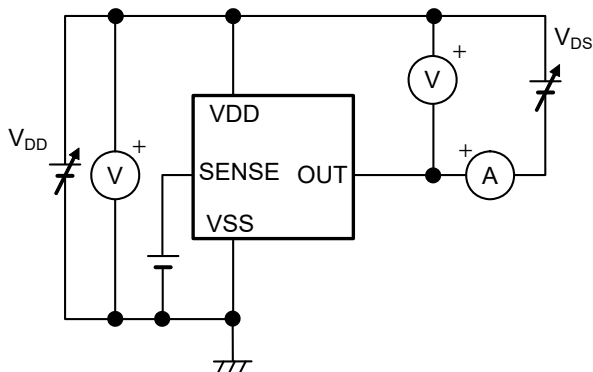
**Figure 11    Test Circuit 5**

# ■ Standard Circuits

**1. Nch open-drain output product**
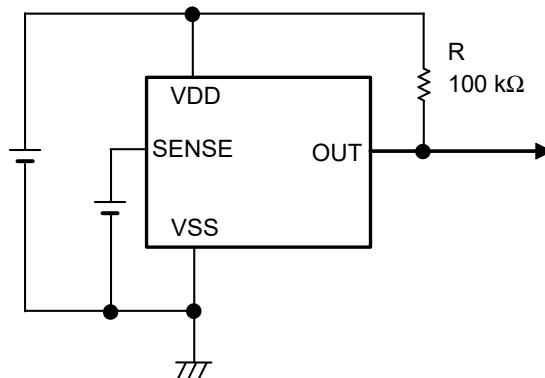


**Figure 12**

**2. CMOS output product**
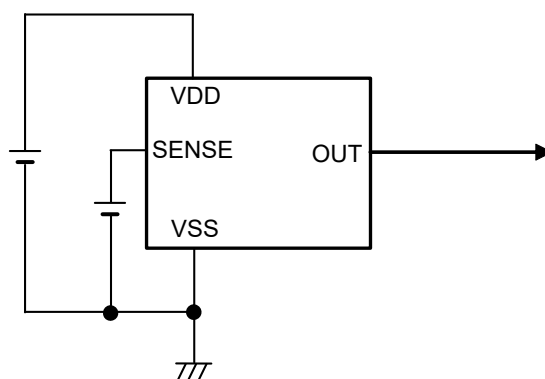


**Figure 13**

**Caution    The above connection diagram and constant will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constant.**

# ■ Explanation of Terms

### 1. Detection voltage (−V$_{DET}$)

The detection voltage is a voltage at which the output in **Figure 16** or **Figure 17** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum (−V$_{DET}$ min.) and the maximum (−V$_{DET}$ max.) is called the detection voltage range (Refer to **Figure 14**).

Example: In the S-19102C18, the detection voltage is either one in the range of 1.733 V ≤ −V$_{DET}$ ≤ 1.867 V.
This means that some S-19102C18 have −V$_{DET}$ = 1.733 V and some have −V$_{DET}$ = 1.867 V.

### 2. Release voltage (+V$_{DET}$)

The release voltage is a voltage at which the output in **Figure 16** or **Figure 17** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum (+V$_{DET}$ min.) and the maximum (+V$_{DET}$ max.) is called the release voltage range (Refer to **Figure 15**). The range is calculated from the actual detection voltage (−V$_{DET}$) of a product and is in the range of −V$_{DET}$ × 1.03 ≤ +V$_{DET}$ ≤ −V$_{DET}$ × 1.07.

Example: For the S-19102C18, the release voltage is either one in the range of 1.785 V ≤ +V$_{DET}$ ≤ 1.997 V.
This means that some S-19102C18 have +V$_{DET}$ = 1.785 V and some have +V$_{DET}$ = 1.997 V.
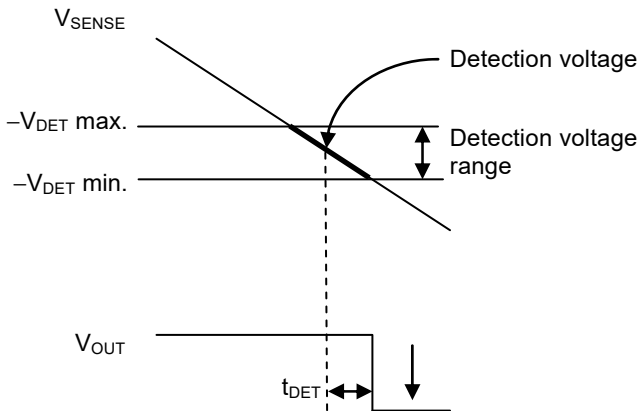
**Figure 14  Detection Voltage**
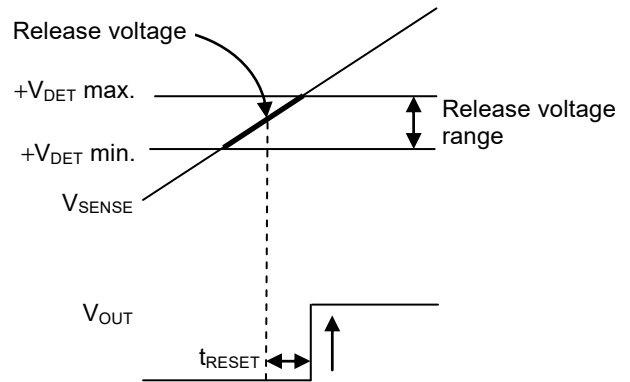
**Figure 15  Release Voltage**
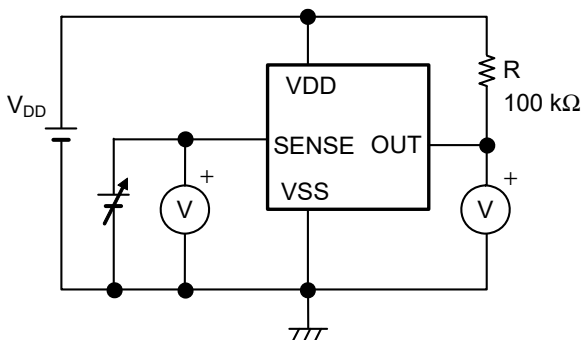
**Figure 16  Test Circuit of Detection Voltage
and Release Voltage
(Nch open-drain output product)**
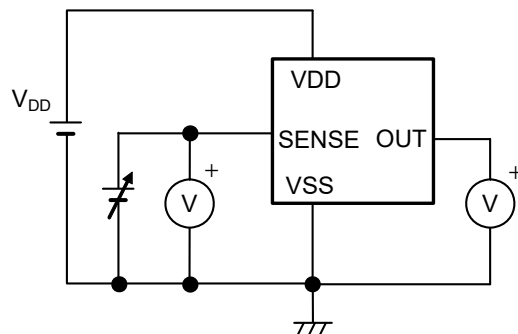
**Figure 17  Test Circuit of Detection Voltage
and Release Voltage
(CMOS output product)**

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### 3. Hysteresis width (V_HYS)

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point B − the voltage at point A = $V_{HYS}$ in "**Figure 20　Timing Chart of S-19102/19108 Series N Type**" and "**Figure 22　Timing Chart of S-19102/19108 Series C Type**"). Setting the hysteresis width between the detection voltage and the release voltage prevents malfunction caused by noise on the input voltage.

### 4. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector. The feed-through current is large in CMOS output product, small in Nch open-drain output product.

### 5. Oscillation

In applications where an input resistor is connected (**Figure 18**), taking a CMOS output (active "L") product for example, the feed-through current which is generated when the output goes from "L" to "H" (at the time of release) causes a voltage drop equal to [feed-through current] × [input resistance]. Since the VDD pin and the SENSE pin are shorted as in **Figure 18**, the SENSE pin voltage drops at the time of release. Then the SENSE pin voltage drops below the detection voltage and the output goes from "H" to "L". In this status, the feed-through current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The feed-through current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.
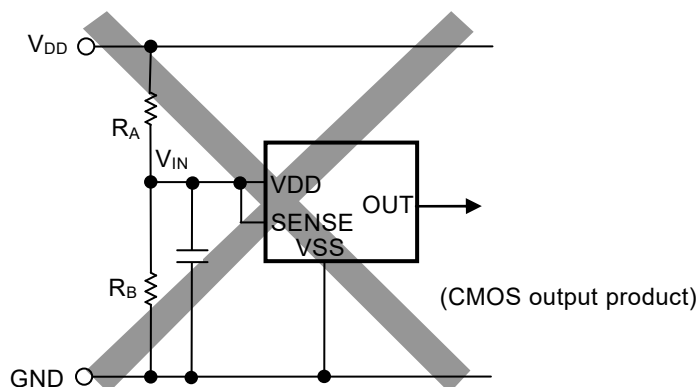


**Figure 18　Example for Bad Implementation Due to Detection Voltage Change**

# ■ Operation

## 1. Basic operation

### 1. 1  S-19102/19108 Series N type

(1) When the power supply voltage ($V_{DD}$) is the minimum operation voltage or higher, and the SENSE pin voltage ($V_{SENSE}$) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off to output $V_{DD}$ ("H") when the output is pulled up. Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\dfrac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) Even if $V_{SENSE}$ decreases to $+V_{DET}$ or lower, $V_{DD}$ is output when $V_{SENSE}$ is higher than the detection voltage ($-V_{DET}$).
   When $V_{SENSE}$ decreases to $-V_{DET}$ or lower (point A in **Figure 20**), the Nch transistor is turned on. And then $V_{SS}$ ("L") is output from the OUT pin after the elapse of the detection delay time ($t_{DET}$).

   At this time, N1 is turned on, and the input voltage to the comparator is $\dfrac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if $V_{SENSE}$ further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when $V_{DD}$ is minimum operation voltage or higher.

(4) Even if $V_{SENSE}$ exceeds $-V_{DET}$, $V_{SS}$ is output when $V_{SENSE}$ is lower than $+V_{DET}$.

(5) When $V_{SENSE}$ increases to $+V_{DET}$ or higher (point B in **Figure 20**), the Nch transistor is turned off. And then $V_{DD}$ is output from the OUT pin after the elapse of the release delay time ($t_{RESET}$) when the output is pulled up.
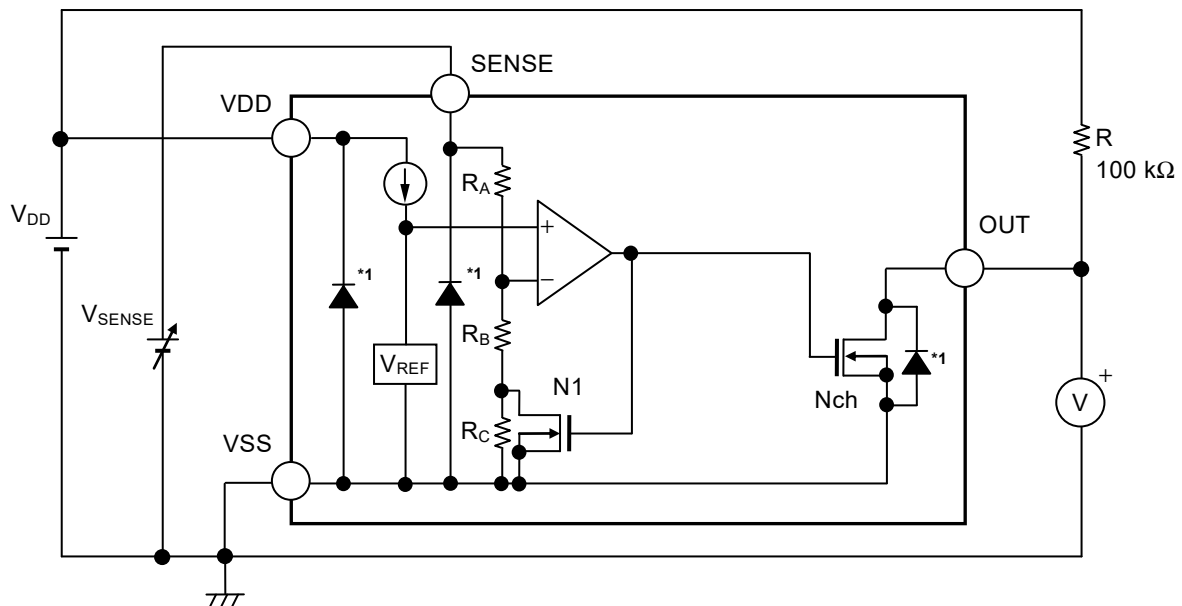


**\*1.**  Parasitic diode

**Figure 19   Operation of S-19102/19108 Series N Type**



**Figure 20   Timing Chart of S-19102/19108 Series N Type**

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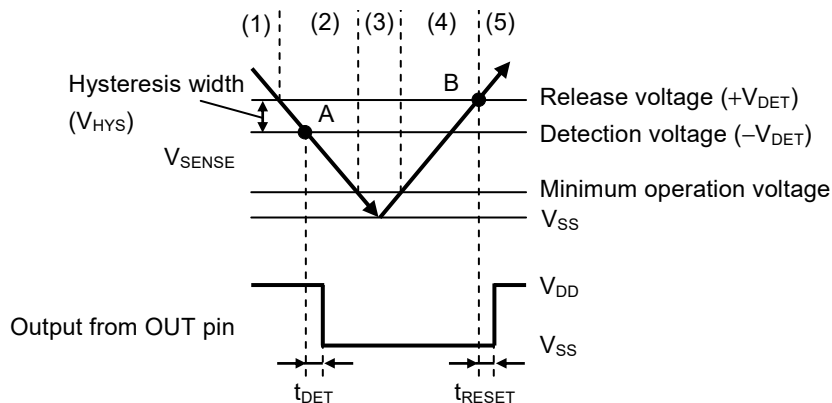
### 1. 2   S-19102/19108 Series C type

(1) When the power supply voltage ($V_{DD}$) is the minimum operation voltage or higher, and the SENSE pin voltage ($V_{SENSE}$) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off and the Pch transistor is turned on to output $V_{DD}$ ("H"). Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\dfrac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) Even if $V_{SENSE}$ decreases to $+V_{DET}$ or lower, $V_{DD}$ is output when $V_{SENSE}$ is higher than the detection voltage ($-V_{DET}$).
When $V_{SENSE}$ decreases to $-V_{DET}$ or lower (point A in **Figure 22**), the Nch transistor is turned on and the Pch transistor is turned off. And then $V_{SS}$ ("L") is output from the OUT pin after the elapse of the detection delay time ($t_{DET}$).

At this time, N1 is turned on, and the input voltage to the comparator is $\dfrac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if $V_{SENSE}$ further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when $V_{DD}$ is minimum operation voltage or higher.

(4) Even if $V_{SENSE}$ exceeds $-V_{DET}$, $V_{SS}$ is output when $V_{SENSE}$ is lower than $+V_{DET}$.

(5) When $V_{SENSE}$ increases to $+V_{DET}$ or higher (point B in **Figure 22**), the Nch transistor is turned off and the Pch transistor is turned on. And then $V_{DD}$ is output from the OUT pin after the elapse of the release delay time ($t_{RESET}$).
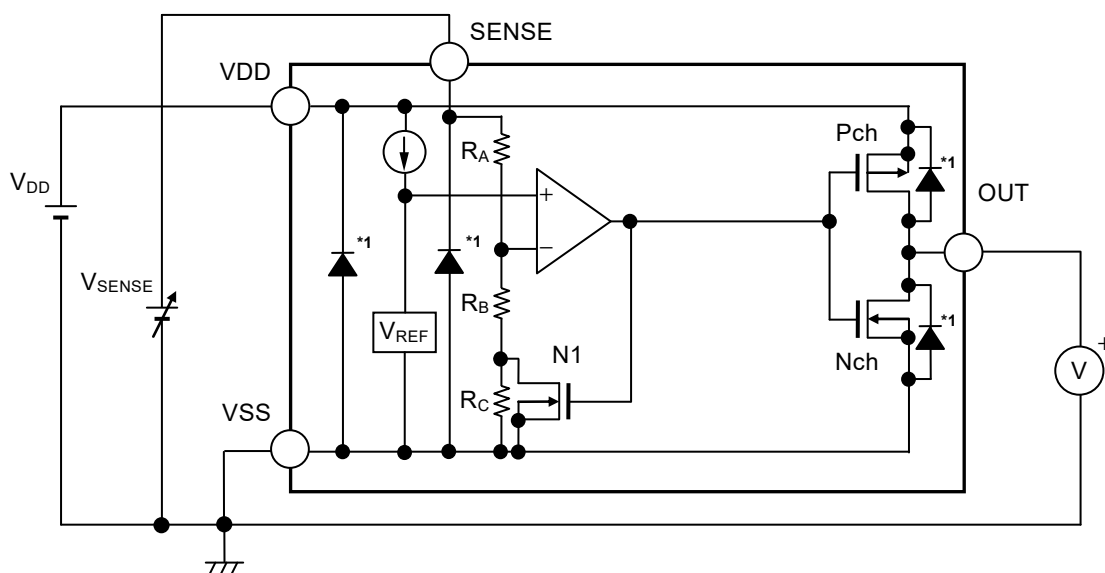


**\*1.**   Parasitic diode

**Figure 21   Operation of S-19102/19108 Series C Type**
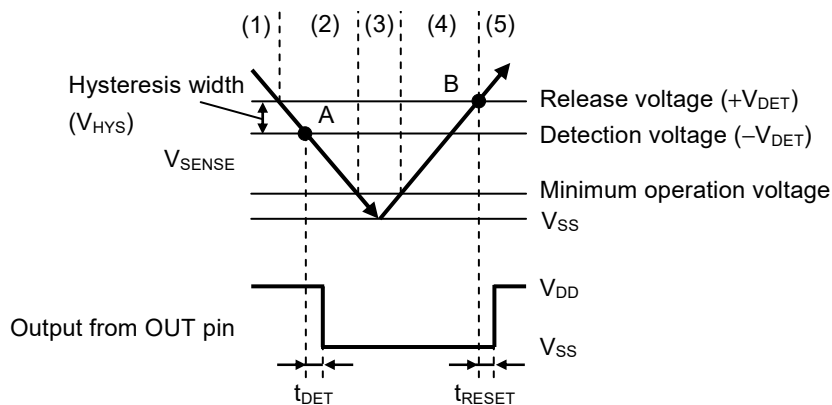


**Figure 22   Timing Chart of S-19102/19108 Series C Type**

## 2. SENSE pin

### 2. 1 Error when detection voltage is set externally

By connecting a node that was resistance-divided by the resistor ($R_A$) and the resistor ($R_B$) to the SENSE pin as seen in **Figure 23**, the detection voltage can be set externally.

For conventional products without the SENSE pin, $R_A$ cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if $R_A$ is large, problems such as oscillation or larger error in the hysteresis width may occur.

In the S-19102/19108 Series, $R_A$ and $R_B$ are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance ($R_{SENSE}$) that will occur.

Although $R_{SENSE}$ in the S-19102/19108 Series is large (4 MΩ min.) to make the error small, $R_A$ and $R_B$ should be selected such that the error is within the allowable limits.

### 2. 2 Selection of $R_A$ and $R_B$

In **Figure 23**, the relation between the external setting detection voltage ($V_{DX}$) and the actual detection voltage ($-V_{DET}$) is ideally calculated by the equation below.

$$V_{DX} = -V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) \qquad \cdots (1)$$

However, in reality there is an error in the current flowing through $R_{SENSE}$.
When considering this error, the relation between $V_{DX}$ and $-V_{DET}$ is calculated as follows.

$$
\begin{aligned}
V_{DX} &= -V_{DET} \times \left(1 + \frac{R_A}{R_B \parallel R_{SENSE}}\right) \\
&= -V_{DET} \times \left(1 + \frac{R_A}{\dfrac{R_B \times R_{SENSE}}{R_B + R_{SENSE}}}\right) \\
&= -V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times -V_{DET} \qquad \cdots (2)
\end{aligned}
$$

By using equations (1) and (2), the error is calculated as $-V_{DET} \times \dfrac{R_A}{R_{SENSE}}$.

The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

$$\frac{R_A \times R_B}{R_{SENSE} \times (R_A + R_B)} \times 100 \ [\%] = \frac{R_A \parallel R_B}{R_{SENSE}} \times 100 \ [\%] \qquad \cdots (3)$$

As seen in equation (3), the smaller the resistance values of $R_A$ and $R_B$ compared to $R_{SENSE}$, the smaller the error rate becomes.

Also, the relation between the external setting hysteresis width ($V_{HX}$) and the hysteresis width ($V_{HYS}$) is calculated by equation below. Error due to $R_{SENSE}$ also occurs to the relation in a similar way to the detection voltage.

$$V_{HX} = V_{HYS} \times \left(1 + \frac{R_A}{R_B}\right) \qquad \cdots (4)$$
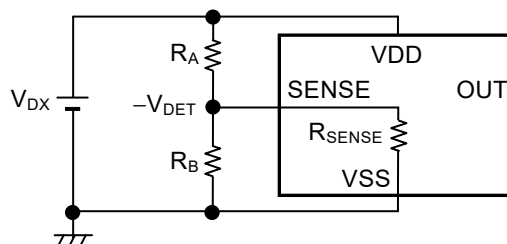


**Figure 23  Detection Voltage External Setting Circuit**

**Caution**   If $R_A$ and $R_B$ are large, the SENSE pin input impedance becomes higher and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.

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### 2. 3   Power on sequence

Apply power in the order, the VDD pin then the SENSE pin.
As seen in **Figure 24**, when $V_{SENSE} \geq +V_{DET}$, the OUT pin output ($V_{OUT}$) rises and the S-19102/19108 Series becomes the release status (normal operation).
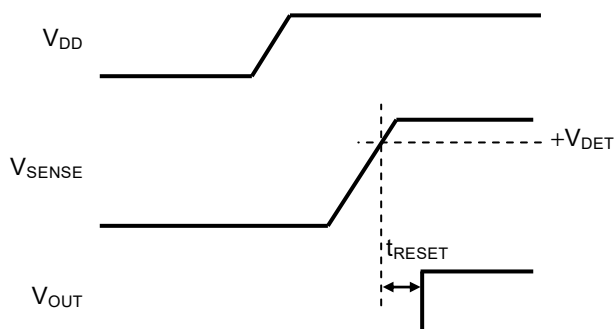
**Figure 24**

**Caution**     **If power is applied in the order the SENSE pin then the VDD pin, an erroneous release may occur even if $V_{SENSE} < +V_{DET}$.**

### 2. 4   Precautions when shorting between the VDD pin and the SENSE pin

#### 2. 4. 1   Input resistor

Do not connect the input resistor ($R_A$) when shorting between the VDD pin and the SENSE pin.
A feed-through current flows through the VDD pin at the time of release. When connecting the circuit shown as **Figure 25**, the feed-through current of the VDD pin flowing through $R_A$ will cause a drop in $V_{SENSE}$ at the time of release.
At that time, oscillation may occur if $V_{SENSE} \leq -V_{DET}$.
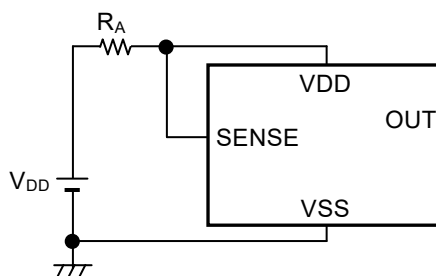
**Figure 25**

#### 2. 4. 2   Parasitic resistance and parasitic capacitance

Due to the difference in parasitic resistance and parasitic capacitance of the VDD pin and the SENSE pin, power may be applied to the SENSE pin first.
Note that an erroneous release may occur if this happens (refer to "**2. 3   Power on sequence**").

**Caution**     **In CMOS output product, make sure that the VDD pin input impedance does not become too high, regardless of the above. Since a feed-through current is large, a malfunction may occur if the VDD pin voltage changes greatly at the time of release.**

### 2. 5 Malfunction when $V_{DD}$ falls

As seen in **Figure 26**, note that if the VDD pin voltage ($V_{DD}$) drops steeply below 1.2 V when $-V_{DET} < V_{SENSE} < +V_{DET}$, erroneous detection may occur.
When $V_{DD\_Low} \geq 1.2$ V, erroneous detection does not occur.
When $V_{DD\_Low} < 1.2$ V, the more the $V_{DD}$ falling amplitude increases or the shorter the falling time becomes, the easier the erroneous detection.
Perform thorough evaluation in actual application.
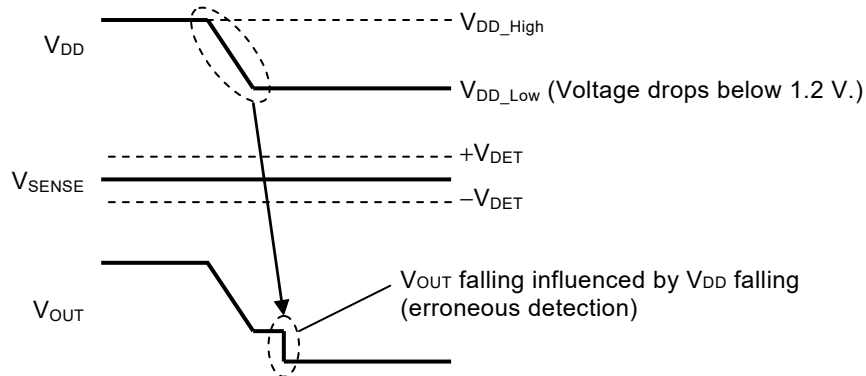


**Figure 26**

The S-19102C50 example in **Figure 27** shows an example of erroneous detection boundary conditions.
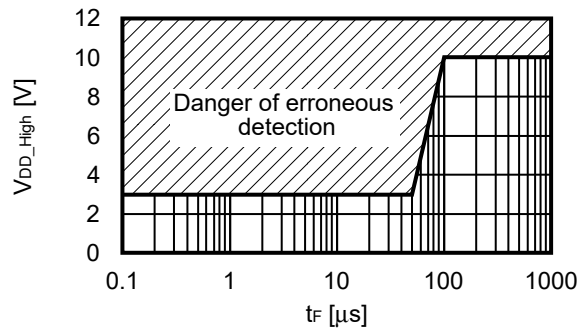


**Figure 27**

**Remark** Test conditions
Product name: S-19102C50
$V_{SENSE}$: $-V_{DET(S)} + 0.1$ V
$V_{DD\_High}$: VDD pin voltage before falling
$V_{DD\_Low}$: VDD pin voltage after falling (0.95 V)
$\Delta V_{DD}$: $V_{DD\_High} - V_{DD\_Low}$
$t_F$: Falling time of $V_{DD}$ from $V_{DD\_High} - \Delta V_{DD} \times 10\%$ to $V_{DD\_Low} + \Delta V_{DD} \times 10\%$



**Figure 28**

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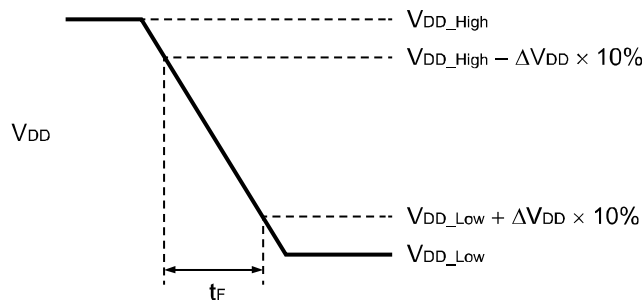
# ■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- In CMOS output product of the S-19102/19108 Series, the feed-through current flows at the time of detection and release. If the VDD pin input impedance is high, malfunction may occur due to the voltage drop by the feed-through current when releasing.

- In CMOS output product, oscillation may occur if a pull-down resistor is connected and falling speed of the SENSE pin voltage ($V_{SENSE}$) is slow near the detection voltage when the VDD pin and the SENSE pin are shorted.

- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

## ■ Characteristics (Typical Data)

### 1. Detection voltage (−$V_{DET}$), Release voltage (+$V_{DET}$) vs. Temperature (Ta)

S-19102C10                                  $V_{DD}$ = 5.0 V

S-19102C24                                  $V_{DD}$ = 5.0 V

S-19102C50                                  $V_{DD}$ = 5.0 V
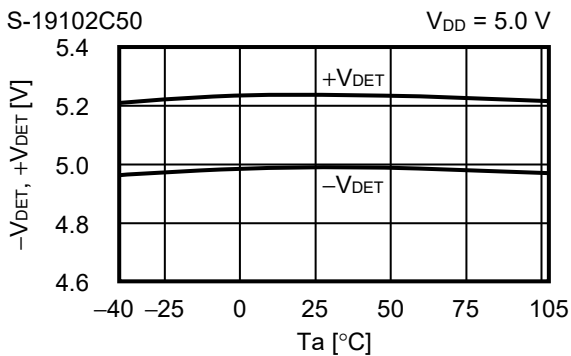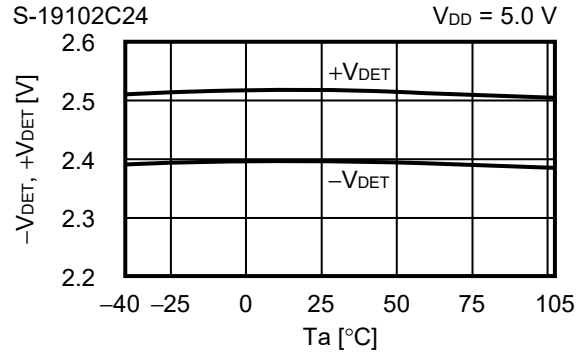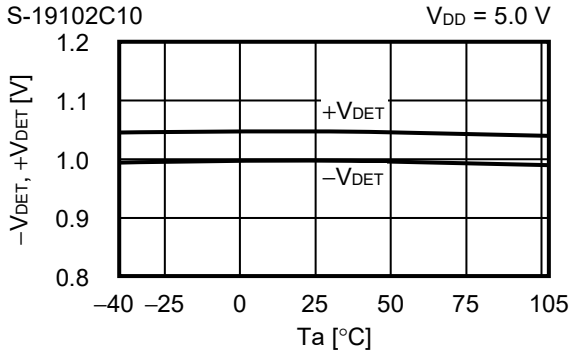
### 2. Hysteresis width ($V_{HYS}$) vs. Temperature (Ta)

S-19102C10                                  $V_{DD}$ = 5.0 V

S-19102C24                                  $V_{DD}$ = 5.0 V

S-19102C50                                  $V_{DD}$ = 5.0 V
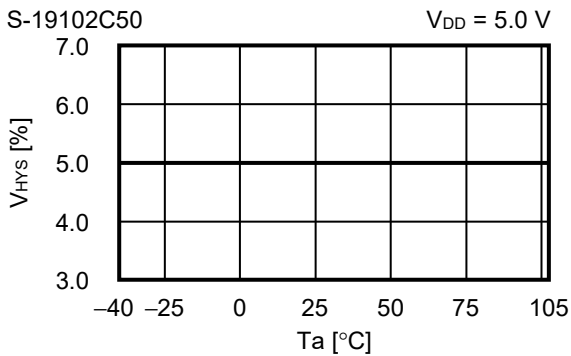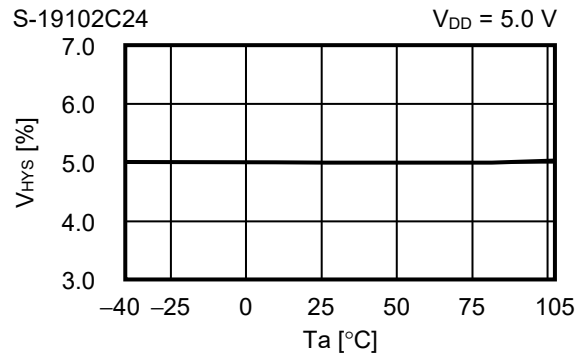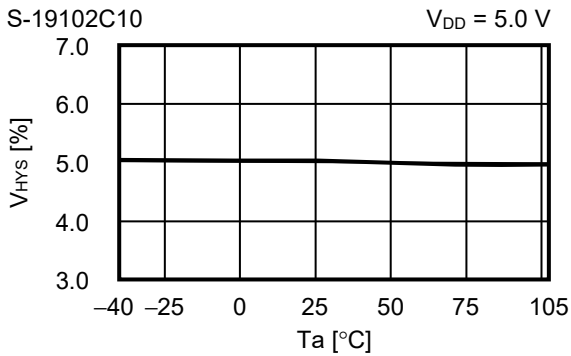
### 3. Detection voltage (−$V_{DET}$) vs. Power supply voltage ($V_{DD}$)

S-19102C10



S-19102C24
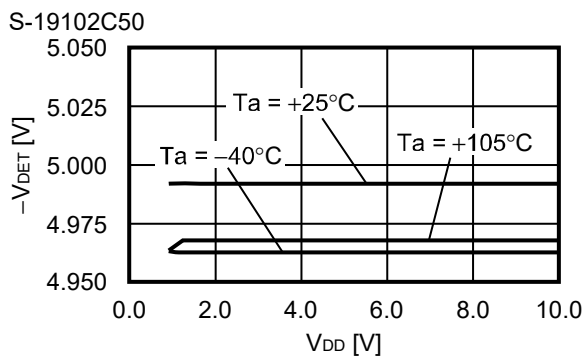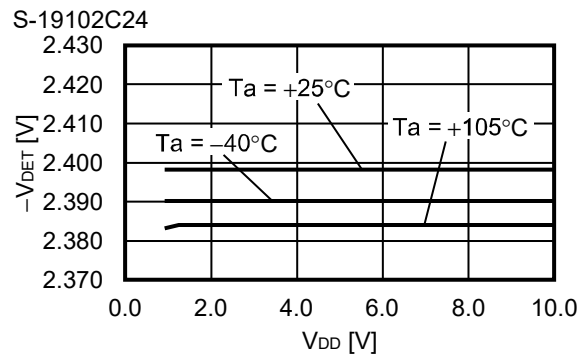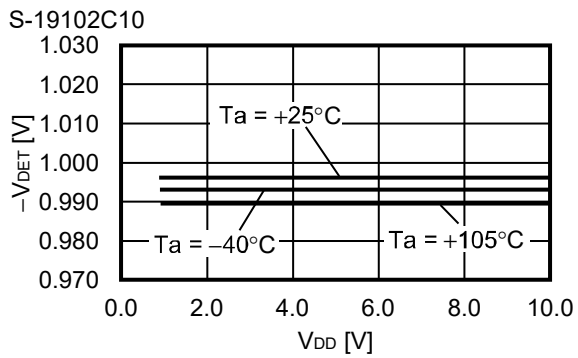


S-19102C50



### 4. Hysteresis width ($V_{HYS}$) vs. Power supply voltage ($V_{DD}$)

S-19102C10



S-19102C24
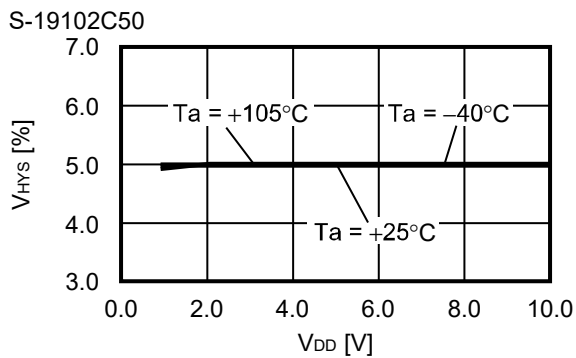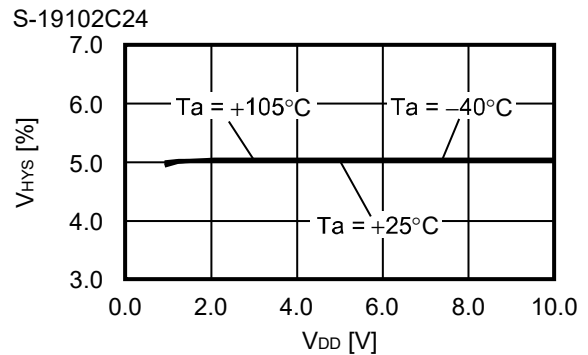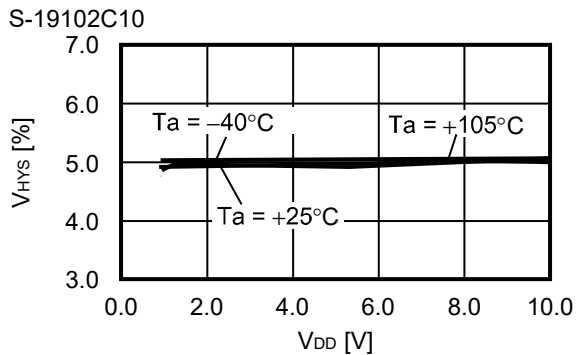


S-19102C50

5. **Current consumption (I$_{SS}$) vs. Power supply voltage (V$_{DD}$)**

S-19102C10

V$_{SENSE}$ = −V$_{DET(S)}$ − 0.1 V (during detection)



S-19102C10

V$_{SENSE}$ = −V$_{DET(S)}$ + 1.0 V (during release)



S-19102C24

V$_{SENSE}$ = −V$_{DET(S)}$ − 0.1 V (during detection)



S-19102C24

V$_{SENSE}$ = −V$_{DET(S)}$ + 1.0 V (during release)



S-19102C50

V$_{SENSE}$ = −V$_{DET(S)}$ − 0.1 V (during detection)



S-19102C50

V$_{SENSE}$ = −V$_{DET(S)}$ + 1.0 V (during release)

ABLIC Inc.
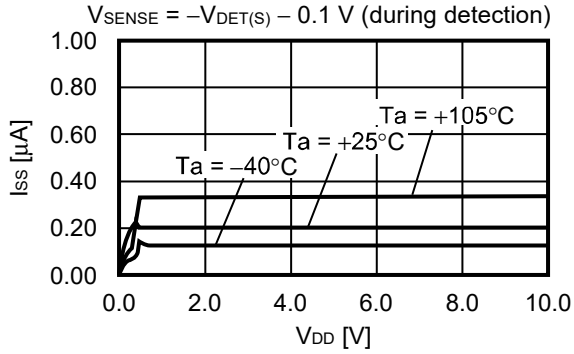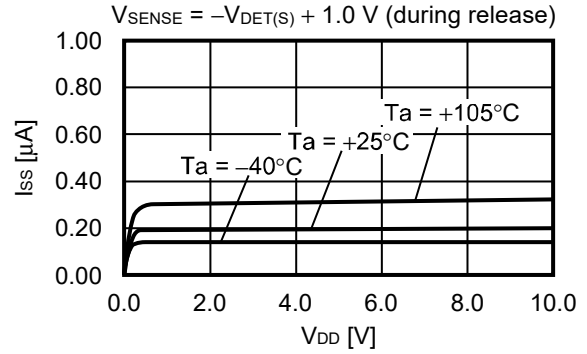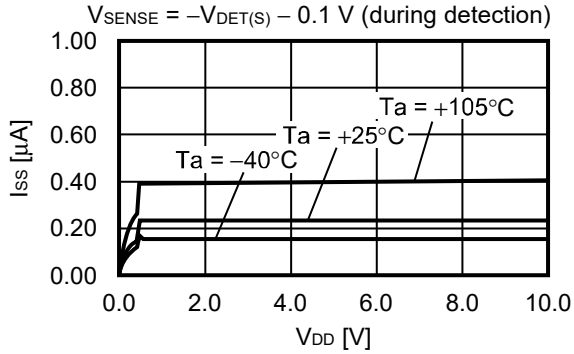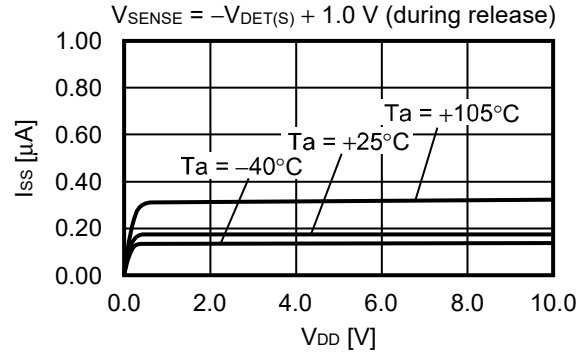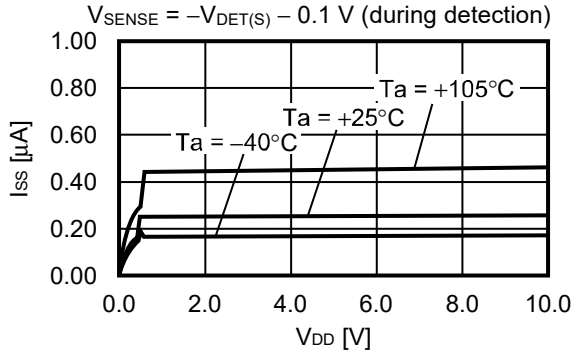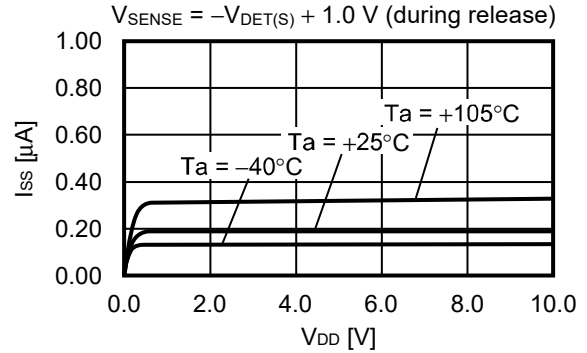
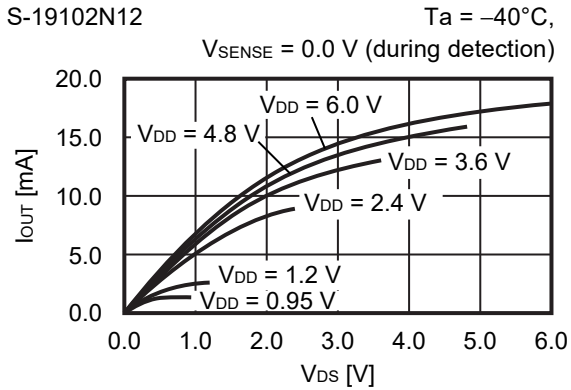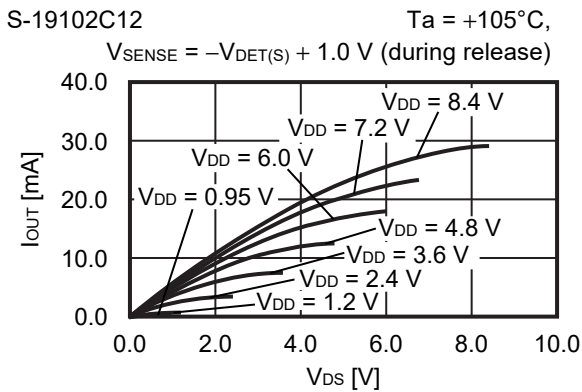**6.   Current consumption ($I_{SS}$) vs. SENSE pin input voltage ($V_{SENSE}$)**

S-19102C10

$V_{DD} = -V_{DET(S)} + 1.0$ V, $V_{SENSE} = 0.0$ V $\rightarrow$ 10.0 V
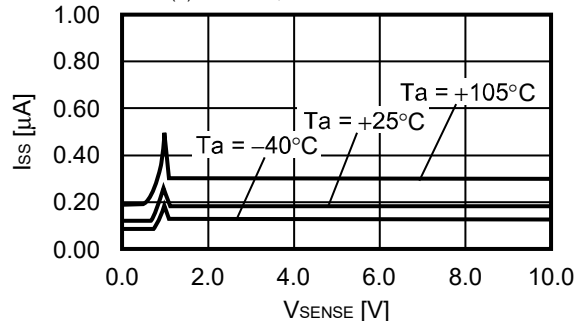
S-19102C24

$V_{DD} = -V_{DET(S)} + 1.0$ V, $V_{SENSE} = 0.0$ V $\rightarrow$ 10.0 V
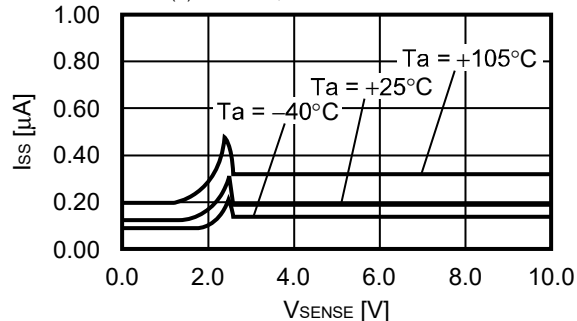
S-19102C50

$V_{DD} = -V_{DET(S)} + 1.0$ V, $V_{SENSE} = 0.0$ V $\rightarrow$ 10.0 V
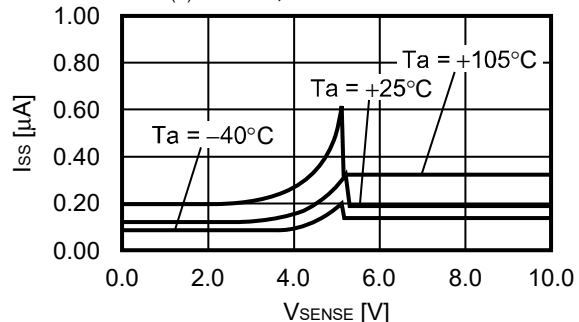
**7.   Current consumption ($I_{SS}$) vs. Temperature (Ta)**

S-19102C10                     $V_{DD} = -V_{DET(S)} + 1.0$ V,

$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)
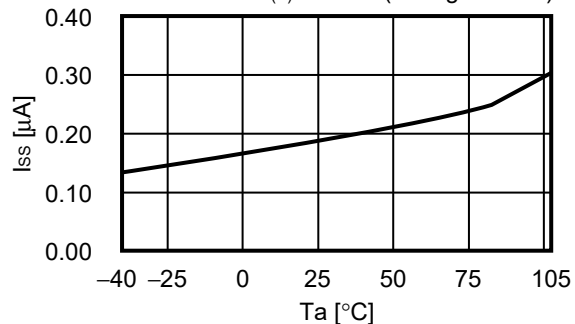
S-19102C24                     $V_{DD} = -V_{DET(S)} + 1.0$ V,

$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)
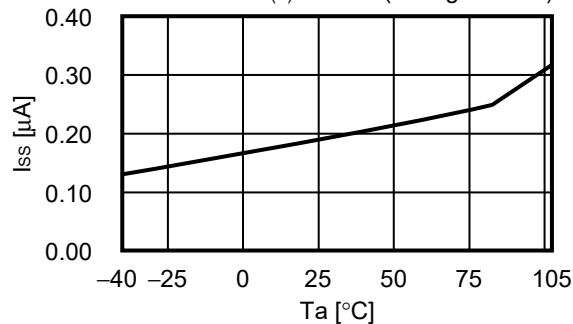
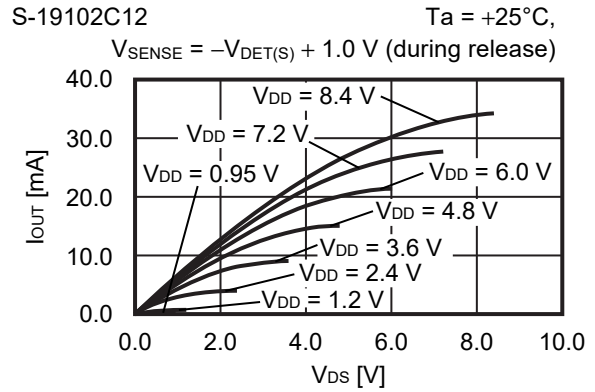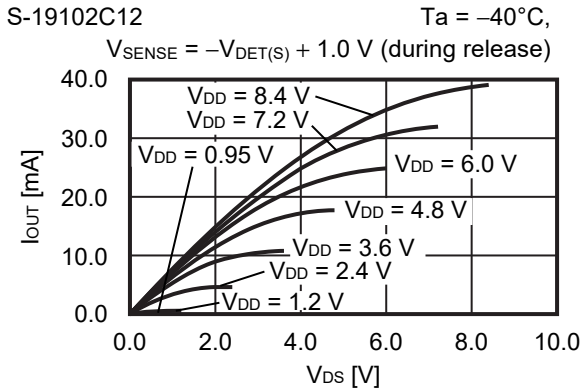S-19102C50                     $V_{DD} = -V_{DET(S)} + 1.0$ V,
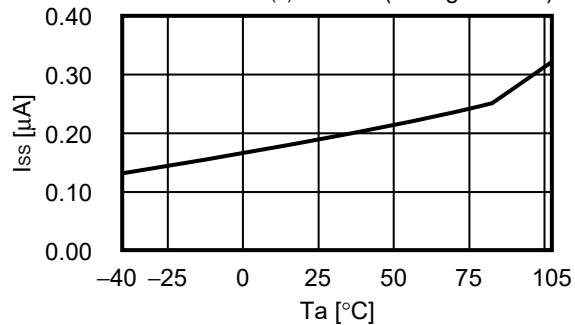
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)

## 8. Nch transistor output current ($I_{OUT}$) – $V_{DS}$
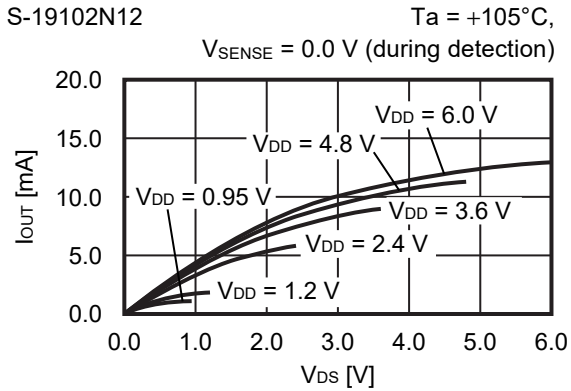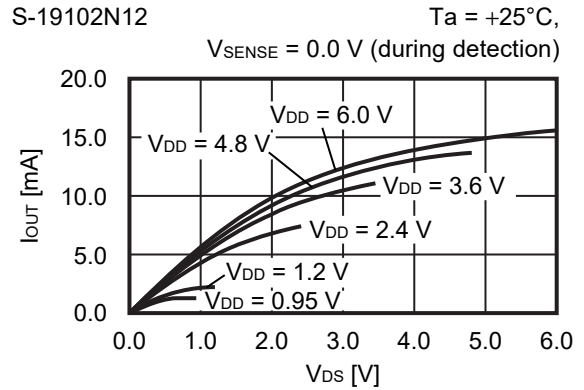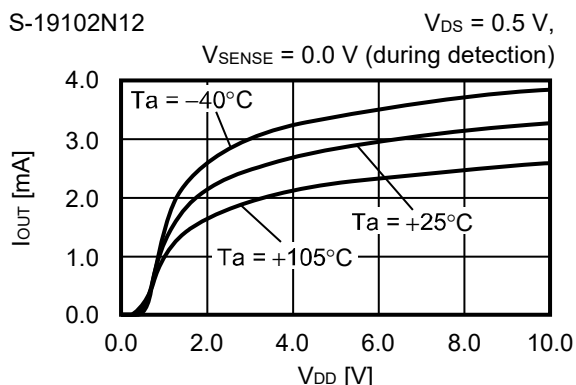
S-19102N12                                      Ta = −40°C,
$V_{SENSE}$ = 0.0 V (during detection)



S-19102N12                                      Ta = +25°C,
$V_{SENSE}$ = 0.0 V (during detection)



S-19102N12                                      Ta = +105°C,
$V_{SENSE}$ = 0.0 V (during detection)



## 9. Pch transistor output current ($I_{OUT}$) – $V_{DS}$

S-19102C12                                      Ta = −40°C,
$V_{SENSE}$ = $-V_{DET(S)}$ + 1.0 V (during release)



S-19102C12                                      Ta = +25°C,
$V_{SENSE}$ = $-V_{DET(S)}$ + 1.0 V (during release)



S-19102C12                                      Ta = +105°C,
$V_{SENSE}$ = $-V_{DET(S)}$ + 1.0 V (during release)



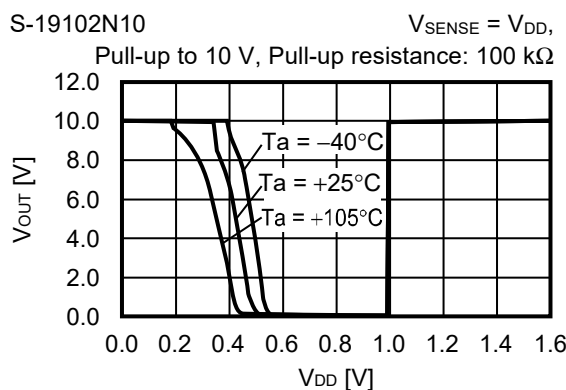**Remark**   $V_{DS}$: Drain-to-source voltage of the output transistor

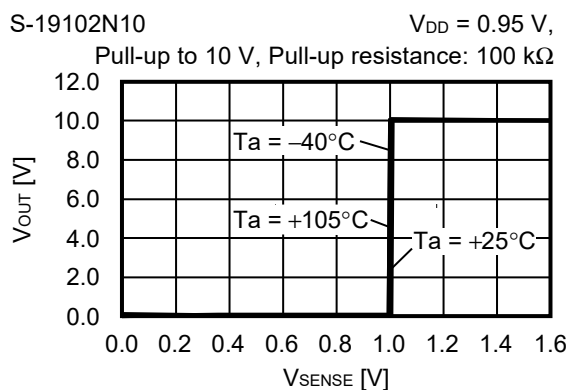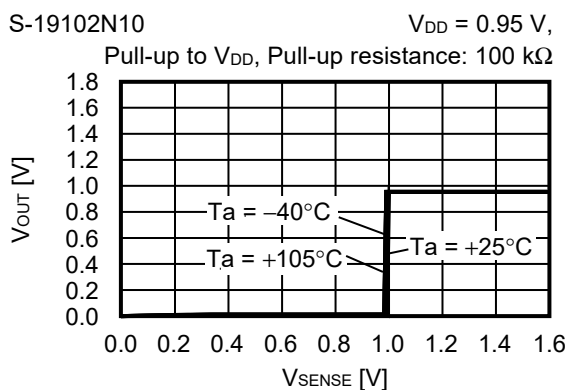**10.  Nch transistor output current ($I_{OUT}$) vs. Power supply voltage ($V_{DD}$)**

S-19102N12 — $V_{DS}$ = 0.5 V, $V_{SENSE}$ = 0.0 V (during detection)



**11.  Pch transistor output current ($I_{OUT}$) vs. Power supply voltage ($V_{DD}$)**

S-19102C12 — $V_{DS}$ = 0.5 V, $V_{SENSE}$ = −$V_{DET(S)}$ + 1.0 V (during release)
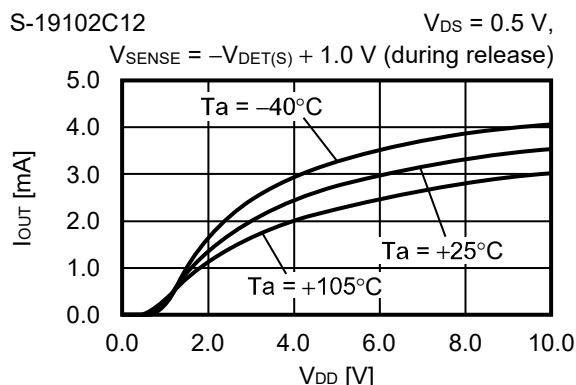


**12.  Minimum operation voltage ($V_{OUT}$) vs. Power supply voltage ($V_{DD}$)**

S-19102N10 — $V_{SENSE}$ = $V_{DD}$, Pull-up to $V_{DD}$, Pull-up resistance: 100 kΩ



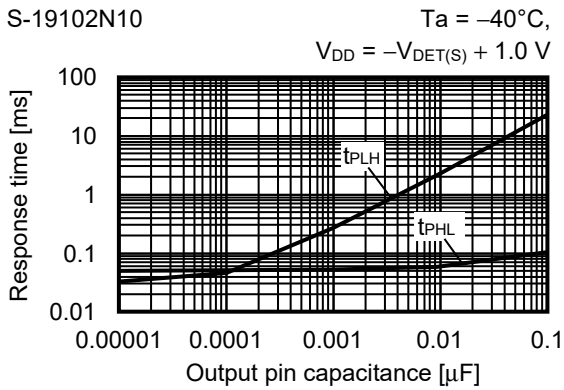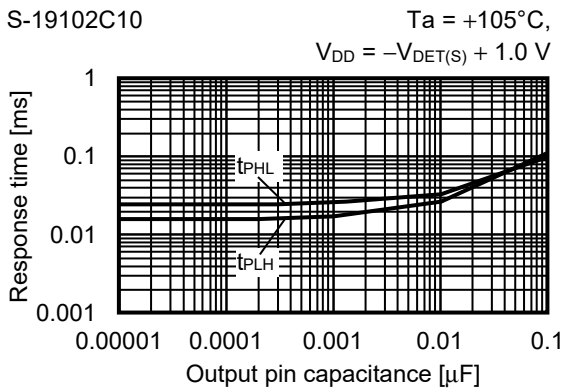S-19102N10 — $V_{SENSE}$ = $V_{DD}$, Pull-up to 10 V, Pull-up resistance: 100 kΩ
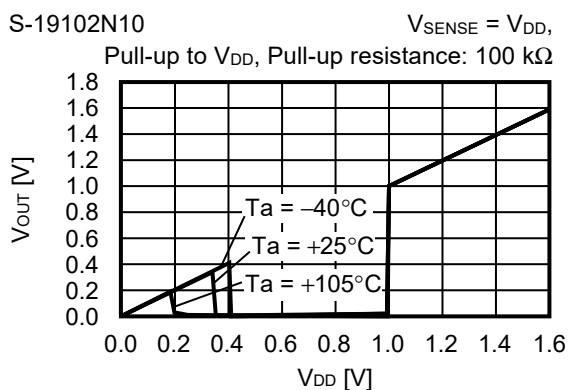


**13.  Minimum operation voltage ($V_{OUT}$) vs. SENSE pin input voltage ($V_{SENSE}$)**

S-19102N10 — $V_{DD}$ = 0.95 V, Pull-up to $V_{DD}$, Pull-up resistance: 100 kΩ



S-19102N10 — $V_{DD}$ = 0.95 V, Pull-up to 10 V, Pull-up resistance: 100 kΩ



**Remark**   $V_{DS}$: Drain-to-source voltage of the output transistor

### 14. Dynamic response vs. Output pin capacitance (C_OUT)
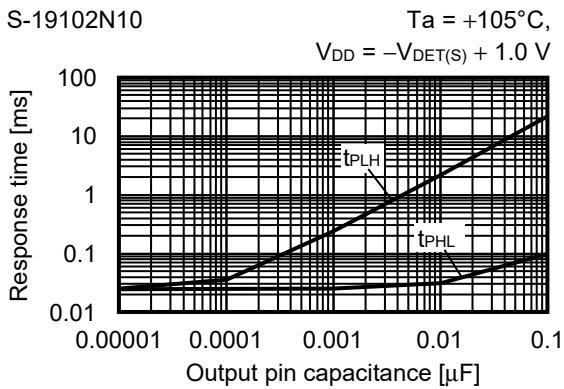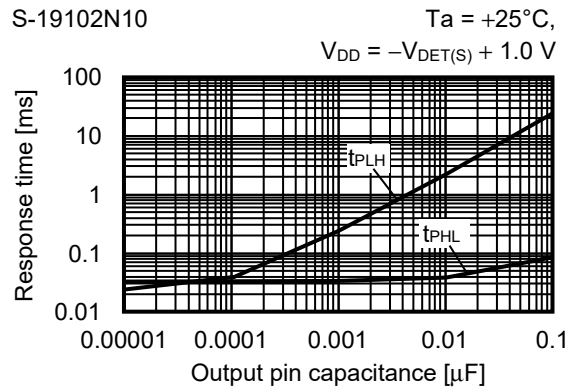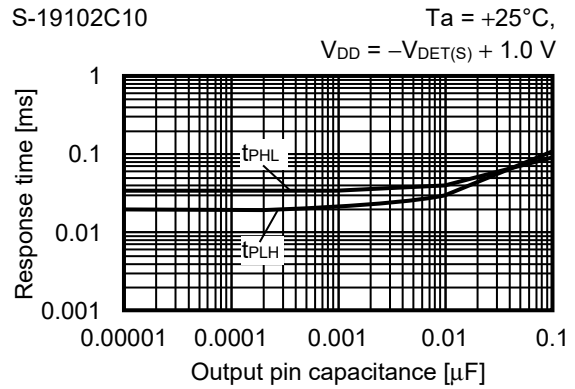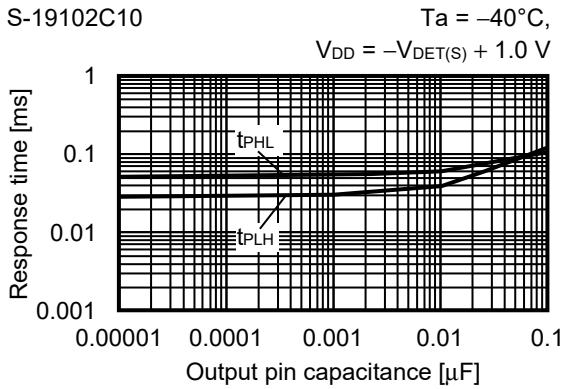
S-19102C10      Ta = −40°C, V_DD = −V_DET(S) + 1.0 V



S-19102C10      Ta = +25°C, V_DD = −V_DET(S) + 1.0 V



S-19102C10      Ta = +105°C, V_DD = −V_DET(S) + 1.0 V



S-19102N10      Ta = −40°C, V_DD = −V_DET(S) + 1.0 V



S-19102N10      Ta = +25°C, V_DD = −V_DET(S) + 1.0 V



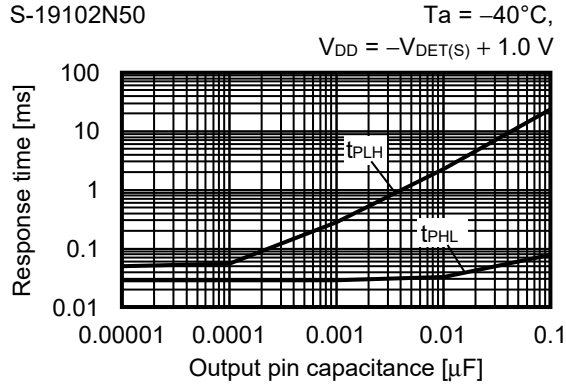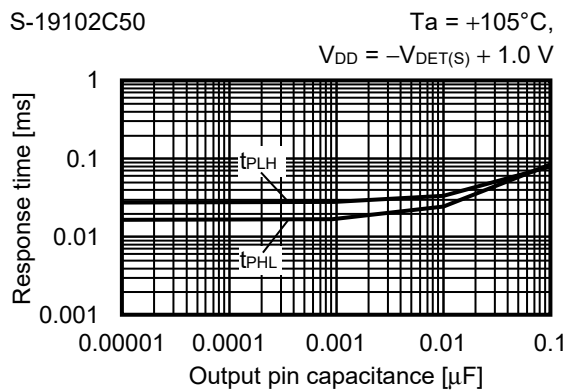S-19102N10      Ta = +105°C, V_DD = −V_DET(S) + 1.0 V

S-19102C50      Ta = −40°C, $V_{DD}$ = −$V_{DET(S)}$ + 1.0 V

S-19102C50      Ta = +25°C, $V_{DD}$ = −$V_{DET(S)}$ + 1.0 V

S-19102C50      Ta = +105°C, $V_{DD}$ = −$V_{DET(S)}$ + 1.0 V

S-19102N50      Ta = −40°C, $V_{DD}$ = −$V_{DET(S)}$ + 1.0 V

S-19102N50      Ta = +25°C, $V_{DD}$ = −$V_{DET(S)}$ + 1.0 V

S-19102N50      Ta = +105°C, $V_{DD}$ = −$V_{DET(S)}$ + 1.0 V

*1. $V_{IH}$ = 10 V
*2. $V_{IL}$ = 0.95 V

**Figure 29   Test Condition of Response Time**



**Figure 30   Test Circuit of Response Time**
**(Nch open-drain output product)**



**Figure 31   Test Circuit of Response Time**
**(CMOS output product)**

**Caution    The above connection diagram and constant will not guarantee successful operation.**
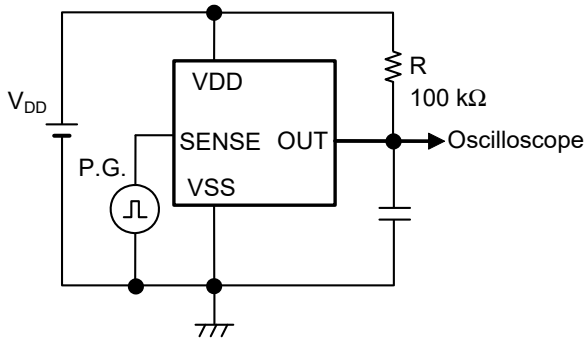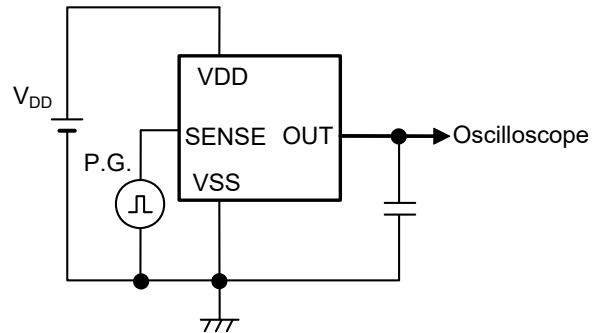**Perform thorough evaluation using the actual application to set the constant.**

# ■ Application Circuit Examples

## 1. Microcomputer reset circuits

In microcomputers, when the power supply voltage is lower than the minimum operation voltage, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to the normal level, the microcomputer needs to be initialized. Otherwise, the microcomputer may malfunction after that. Reset circuits to protect microcomputer in the event of current being momentarily switched off or lowered.

Using the S-19102/19108 Series which has the low minimum operation voltage, the high-accuracy detection voltage and the hysteresis width, reset circuits can be easily constructed as seen in **Figure 32** and **Figure 33**.



**Figure 32   Example of Reset Circuit
(Nch open-drain output product)**

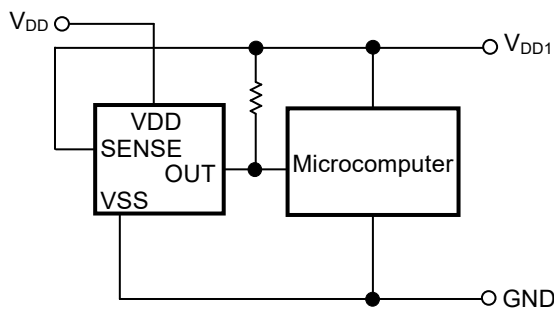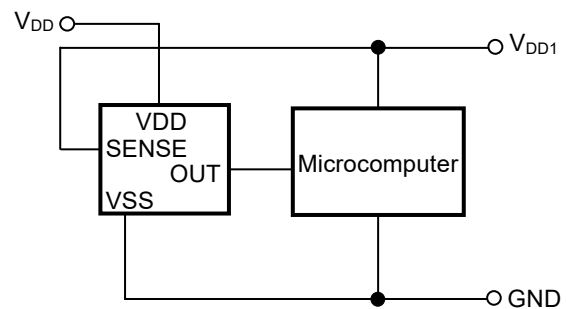**Figure 33   Example of Reset Circuit
(CMOS output product)**

**Caution    The above connection diagram and constant will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constant.**

## 2. Change of detection voltage

If there is not a product with a specified detection voltage value in the S-19102/19108 Series, the detection voltage can be changed by using a resistance divider or a diode, as seen in **Figure 34** to **Figure 37**.
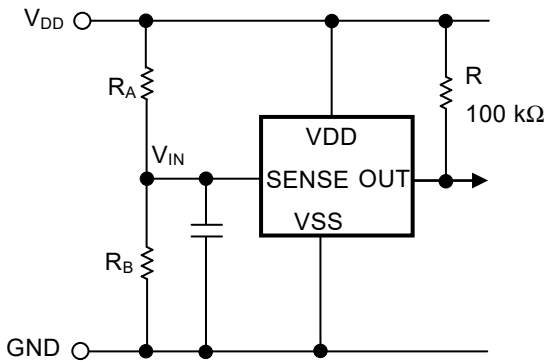In **Figure 34** and **Figure 35**, hysteresis width also changes.



**Figure 34   Detection voltage change**
**when using a resistance divider**
**(Nch open-drain output product)**
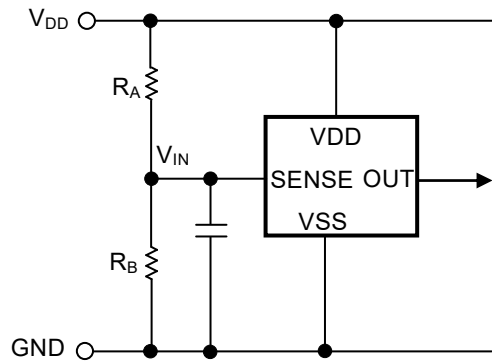


**Figure 35   Detection voltage change**
**when using a resistance divider**
**(CMOS output product)**

**Remark**   Detection voltage = $\dfrac{R_A + R_B}{R_B} \bullet -V_{DET}$

Hysteresis width = $\dfrac{R_A + R_B}{R_B} \bullet V_{HYS}$
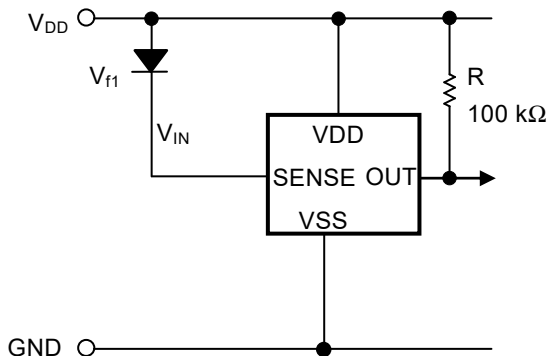


**Figure 36   Detection voltage change**
**when using a diode**
**(Nch open-drain output product)**
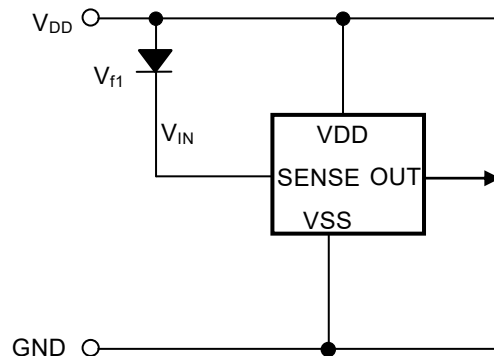


**Figure 37   Detection voltage change**
**when using a diode**
**(CMOS output product)**

**Remark**   Detection voltage = $V_{f1} + (-V_{DET})$

**Caution 1.   The above connection diagram and constant will not guarantee successful operation.**
**Perform thorough evaluation using the actual application to set the constant.**
**2.   Set the constants referring to "2. 1   Error when detection voltage is set externally" in**
**"■ Operation".**

## ■ Power Dissipation

**SOT-23-5**

$T_j$ = +125°C max.
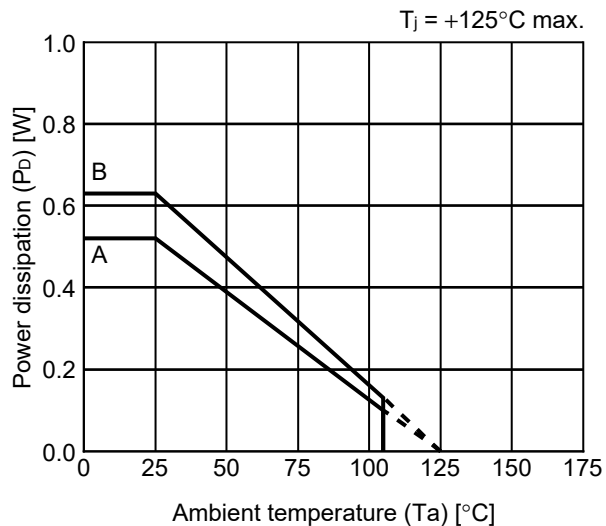


| Board | Power Dissipation ($P_D$) |
|:-----:|:-------------------------:|
| A     | 0.52 W                    |
| B     | 0.63 W                    |
| C     | –                         |
| D     | –                         |
| E     | –                         |

# SOT-23-3/3S/5/6  Test Board

⬭ IC Mount Area

**(1) Board A**
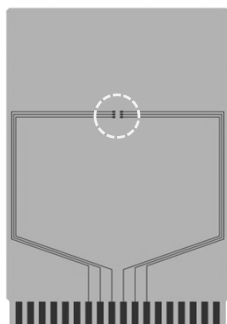
| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 2 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | - |
| | 3 | - |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

**(2) Board B**
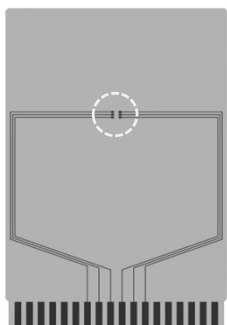
| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

No. SOT23x-A-Board-SD-2.0

ABLIC Inc.

2.9±0.2

1.9±0.2

5　　　4

1　2　3

1.6

2.8 +0.2 -0.3

0.45

0.16 +0.1 -0.06

1.1±0.1

1.3max.

0.95±0.1

0.4±0.1

0 to 0.15
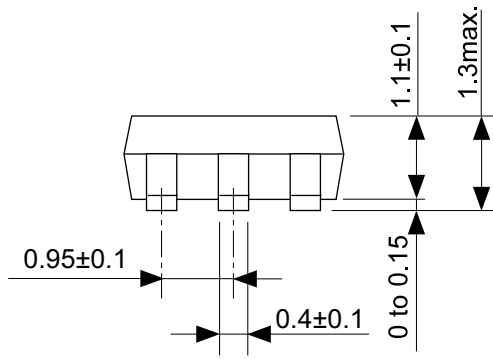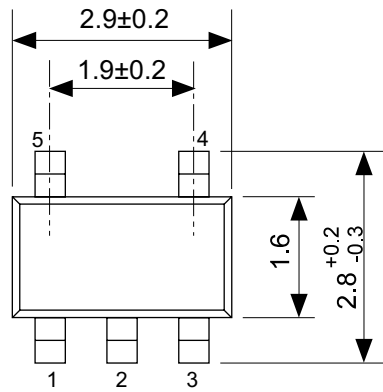
No. MP005-A-P-SD-1.3

| TITLE | SOT235-A-PKG Dimensions |
|---|---|
| No. | MP005-A-P-SD-1.3 |
| ANGLE | ⊕ ⊏ |
| UNIT | mm |
| | |

**ABLIC Inc.**

ø1.5 +0.1 -0

2.0±0.05

4.0±0.1(10 pitches:40.0±0.2)

1.75±0.1

0.25±0.1

3.5±0.05

8.0±0.2

3.25±0.15

ø1.0 +0.2 -0

4.0±0.1

1.4±0.2

3.2±0.2

3 2 1

4 5

Feed direction

No. MP005-A-C-SD-2.1

| TITLE | SOT235-A-Carrier Tape |
|-------|----------------------|
| No. | MP005-A-C-SD-2.1 |
| ANGLE | |
| UNIT | mm |
| | |

**ABLIC Inc.**

12.5max.

$\varnothing 60^{+1}_{-0}$  $\varnothing 180^{+0}_{-3}$

9.0±0.3

Enlarged drawing in the central part

$\varnothing 21±0.5$  $\varnothing 13±0.2$

2±0.2

(60°)  (60°)

No. MP005-A-R-SD-1.1

| TITLE | SOT235-A-Reel | | |
|---|---|---|---|
| No. | MP005-A-R-SD-1.1 | | |
| ANGLE | | QTY. | 3,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |

# Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.

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3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.

4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.

5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.

6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.

7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.

8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.

9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.

10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.

11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.

12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.

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14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.

15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

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