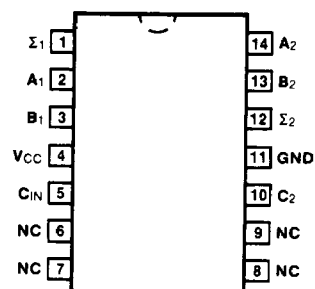


✓ **54/7482** 010002  
**2-BIT FULL ADDER**

**CONNECTION DIAGRAM**  
**PINOUT A**

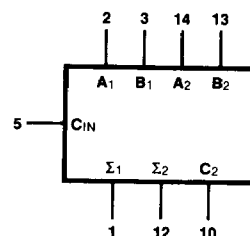


**DESCRIPTION** — The '82 is a full adder which performs the addition of two 2-bit binary numbers. The sum ( $\Sigma$ ) outputs are provided for each bit and the resultant carry ( $C_2$ ) is obtained from the second bit. Designed for medium to high speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high speed, high fan-out TTL. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

**ORDERING CODE:** See Section 9

| PKGS               | PIN<br>OUT | COMMERCIAL GRADE   | MILITARY GRADE   | PKG<br>TYPE |
|--------------------|------------|--|--|-------------|
|                    |            | $V_{CC} = +5.0 \text{ V} \pm 5\%$ ,<br>$T_A = 0^\circ \text{C to } +70^\circ \text{C}$ | $V_{CC} = +5.0 \text{ V} \pm 10\%$ ,<br>$T_A = -55^\circ \text{C to } +125^\circ \text{C}$ |             |
| Plastic<br>DIP (P) | A          | 7482PC   |  | 9A          |
| Ceramic<br>DIP (D) | A          | 7482DC   | 5482DM   | 6A          |
| Flatpak<br>(F)     | A          | 7482FC   | 5482FM   | 3I          |

**LOGIC SYMBOL**



$V_{CC}$  = Pin 14  
 GND = Pin 11  
 NC = Pins 6,7,8,9

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

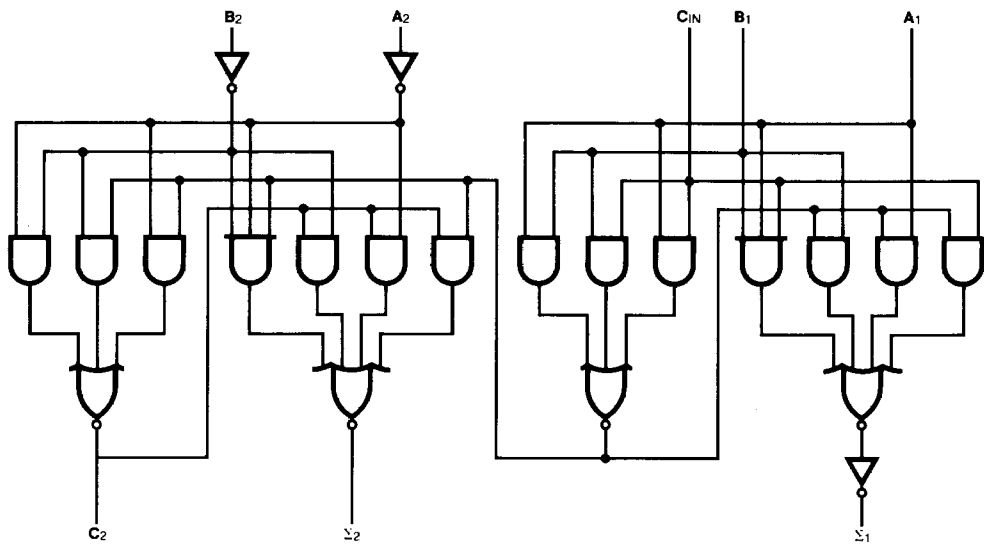
| PIN NAMES                       | DESCRIPTION          | 54/74 (U.L.)<br>HIGH/LOW |
|---------------------------------|----------------------|--------------------------|
| A <sub>1</sub> , B <sub>1</sub> | Bit 1 Operand Inputs | 4.0/4.0                  |
| A <sub>2</sub> , B <sub>2</sub> | Bit 2 Operand Inputs | 1.0/1.0                  |
| C <sub>IN</sub>                 | Bit 1 Carry Input    | 4.0/4.0                  |
| $\Sigma_1$                      | Bit 1 Sum Output     | 10/10                    |
| $\Sigma_2$                      | Bit 2 Sum Output     | 10/10                    |
| C <sub>2</sub>                  | Bit 2 Carry Output   | 5.0/5.0                  |

TRUTH TABLE

| INPUTS |       |       |       | OUTPUTS      |            |       |              |            |       |
|--------|-------|-------|-------|--------------|------------|-------|--------------|------------|-------|
|        |       |       |       | $C_{IN} = 0$ |            |       | $C_{IN} = 1$ |            |       |
| $A_1$  | $B_1$ | $A_2$ | $B_2$ | $\Sigma_1$   | $\Sigma_2$ | $C_2$ | $\Sigma_1$   | $\Sigma_2$ | $C_2$ |
| L      | L     | L     | L     | L            | L          | L     | H            | L          | L     |
| H      | L     | L     | L     | H            | L          | L     | L            | H          | L     |
| L      | H     | L     | L     | H            | L          | L     | L            | H          | L     |
| H      | H     | L     | L     | L            | H          | L     | H            | H          | L     |
| L      | L     | H     | L     | L            | H          | L     | H            | H          | L     |
| H      | L     | H     | L     | H            | H          | L     | L            | L          | H     |
| L      | H     | H     | L     | H            | H          | L     | L            | L          | H     |
| H      | H     | H     | L     | L            | L          | H     | H            | L          | H     |
| L      | L     | L     | H     | L            | H          | L     | H            | H          | L     |
| H      | L     | L     | H     | H            | H          | L     | L            | L          | H     |
| L      | H     | L     | H     | H            | H          | L     | L            | L          | H     |
| H      | H     | L     | H     | L            | L          | H     | H            | L          | H     |
| L      | L     | H     | H     | L            | L          | H     | H            | L          | H     |
| H      | L     | H     | H     | H            | L          | H     | L            | H          | H     |
| L      | H     | H     | H     | L            | L          | H     | L            | H          | H     |
| H      | H     | H     | H     | L            | H          | H     | H            | H          | H     |

H = HIGH Voltage Level  
L = LOW Voltage Level

LOGIC DIAGRAM



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL          | PARAMETER                                      |    | 54/74 |     | UNITS | CONDITIONS  |
|-----------------|--|----|-------|-----|-------|---|
|                 |  |    | Min   | Max |       |   |
| I <sub>os</sub> | Output Short Circuit Current at $\Sigma_n$     | XM | -20   | -55 | mA    | V <sub>CC</sub> = Max   |
|                 |  | XC | -18   | -55 |       |   |
| I <sub>os</sub> | Output Short Circuit Current at C <sub>2</sub> | XM | -20   | -70 | mA    | V <sub>CC</sub> = Max   |
|                 |  | XC | -18   | -70 |       |   |
| I <sub>CC</sub> | Power Supply Current                           | XM |       | 50  | mA    | V <sub>CC</sub> = Max;<br>A <sub>1</sub> , A <sub>2</sub> , C <sub>IN</sub> = 4.5 V;<br>B <sub>1</sub> , B <sub>2</sub> = Gnd |
|                 |  | XC |       | 58  |       |   |

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C (See Section 3 for waveforms and load configurations)

| SYMBOL                               | PARAMETER  | 54/74  |     | UNITS | CONDITIONS                               |
|--------------------------------------|--|--|-----|-------|--|
|                                      |  | C <sub>L</sub> = 15 pF<br>R <sub>L</sub> = 400 Ω |     |       |  |
|                                      |  | Min  | Max |       |  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>C <sub>IN</sub> to Σ <sub>1</sub> | 34<br>40   |     | ns    | Figs. 3-1, 3-20                          |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>B <sub>2</sub> to Σ <sub>2</sub>  | 40<br>35   |     | ns    | Figs. 3-1, 3-20                          |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>C <sub>IN</sub> to Σ <sub>2</sub> | 38<br>42   |     | ns    | Figs. 3-1, 3-20                          |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>C <sub>IN</sub> to C <sub>2</sub> | 19<br>27   |     | ns    | Figs. 3-1, 3-5<br>R <sub>L</sub> = 780 Ω |