



Achieving EMV Electrical Compliance with the Teridian 73S8024RN

1 Introduction

This application note highlights particular testing considerations required to achieve compliance for payment systems smart card interfaces in accordance with the EMV2000 version 4.0 specification when using the TERIDIAN 73S8024RN integrated circuit. This note details in particular the EMV2000 test suite for the electrical section.

Reference document is the “EMVCo Type Approval Terminal Level 1 Test Cases” which can be downloaded from the EMVCo website at “www.emvco.com”.

2 Design Guide

2.1 Typical Electrical Schematic and Bill of Materials

The electrical schematic recommended for a typical EMV2000 compliant smart card interface implementation is given in Figure 3-1 and its corresponding Bill of Materials is in Table 3-1.

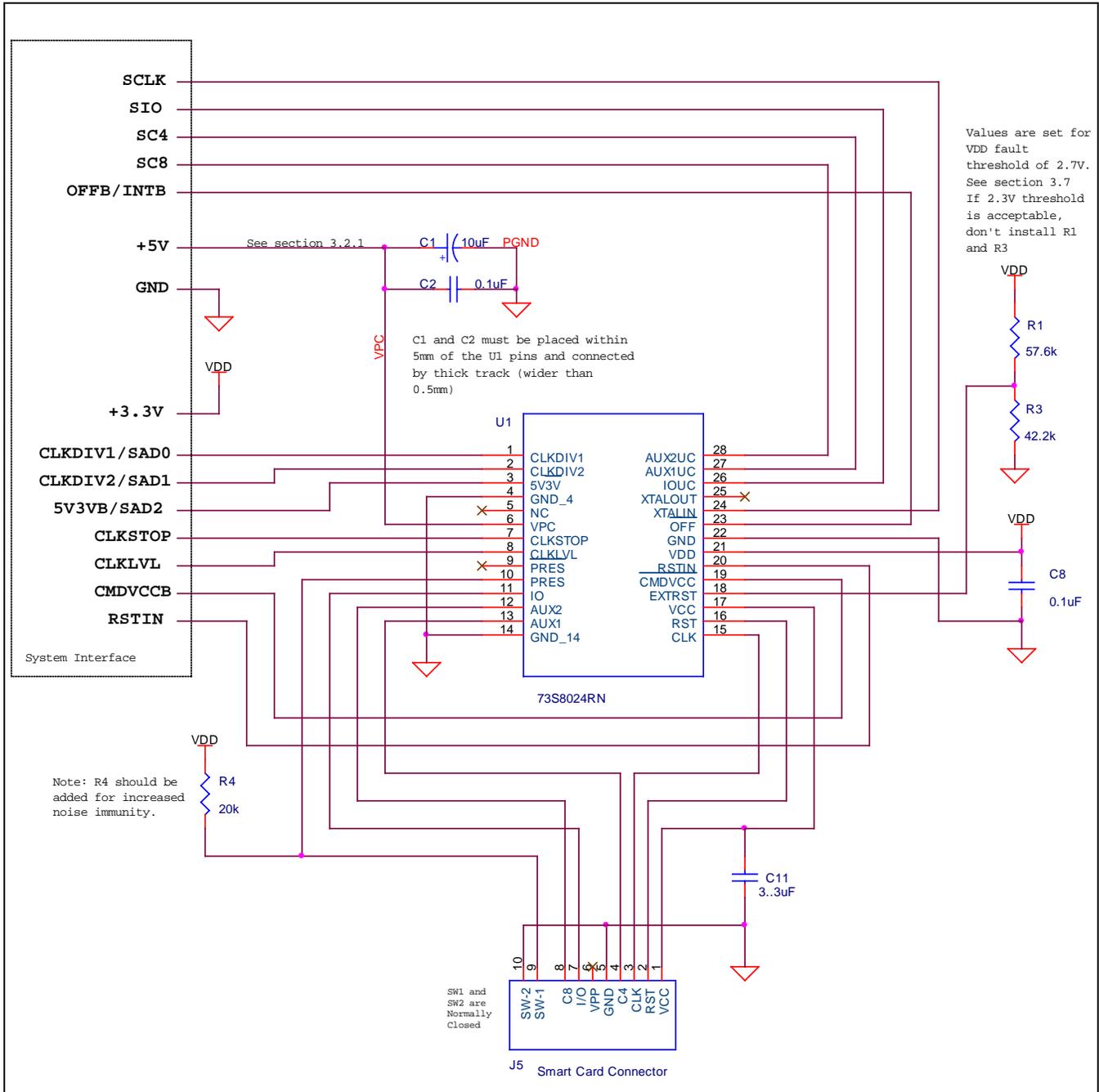


Figure 2-1: Typical Schematic using the 73S8024RN for EMV Applications

Item	Quantity	Reference	Part	PCB Foot print (see attached zip file)	Digikey part number	Part number	Manufacturer
1	1	C1	10 μ F	805	445-1363-1-ND	C2012X5R0J106M	TDK
2	1	C11	3.3 μ F	805	PCC1925CT-ND	ECJ-2YB0J335K	Panasonic
3	2	C2,C8	0.1 μ F	603	445-1317-1-ND	C1608X7R1C104K	TDK
4	1	J5	Smart Card Connector	ITT_CCM02-2504	ccm02-2504-ND	ccm02-2504	ITTCannon
5	1	R4	20k	603	P20KGCT-ND	ERJ-3GEYJ203V	Panasonic
6	1	U1	73S8024RN	28SOP	X	73S8024RN	TDK

Table 2-1: BOM for EMV-compliant configuration

2.2 Power Supply:

2.2.1 Analog Power Supply V_{PC} :

The 73S8024RN incorporates a Low-Drop-Out voltage regulator to generate the card power supply V_{CC} . The VPC pin is the power supply input of this regulator, and the correct V_{PC} voltage must be asserted on this pin in order to ensure proper generation of V_{CC} to the card.

Depending on the card voltage required, the V_{PC} power supply input can eventually be different, as follows:

Power supply V_{PC} , to support both 3V and 5V smart cards:

V_{PC} must be 5V nominal, and the following condition must be respected: **$4.75V \leq V_{PC} \leq 5.5V$**

Decoupling and PCB Layout:

The 73S8024RN reference schematic has 2 decoupling capacitors on V_{PC} . The larger capacitor is 10 μ F and the small capacitor is 0.1 μ F (respectively C1 and C2). The smaller capacitor should be placed very close to the 73S8024RN. V_{PC} should be routed on a plane for best results. If no plane is possible, the larger capacitor should be as close as possible to the 73S8024RN. Keep the VCC trace as short as possible. Make the trace a minimum of 0.5mm thick. Also, keep VCC away from other traces especially RST and CLK. The ground connections and the decoupling capacitor grounds should be routed directly to the ground plane.

2.2.2 Digital Power Supply:

The 73S8024RN has a separate power supply input V_{DD} , that powers the internal digital circuitry. V_{DD} is also the reference voltage to interface with the host microcontroller. V_{DD} should be decoupled with a small capacitor of 0.1 μ F to ground. Operating V_{DD} voltage for implementing the 73S8024RN in EMV applications is **$2.7V \leq V_{DD} \leq 5.5V$**

2.3 Card Interface Guidelines

In order to achieve EMV certification, the following smart card interface guidelines should be followed:

1. Route auxiliary signals away from card interface signals.
2. Keep CLK signal as short as possible and with a minimal number of bends in the trace. Keep routing of the CLK trace to one layer (avoid vias between other layers). Keep the CLK trace away from other traces especially RST and VCC. Filtering of the CLK trace is allowed for noise purposes. Up to 30pF to ground is allowed at the CLK pin of the smart card connector. Also, a resistor can be inserted in series on the CLK signal to provide additional filtering (no more than 100 Ω).
3. Keep RST trace away from VCC and CLK traces. Up to 30pF to ground is allowed for filtering
4. Keep 3.3 μ F Vcc capacitor close to VCC pin of the smart card connector and take the other end of the capacitor directly to ground

3 EMV Test Conditions

The EMV test suite is configured for 5V smart cards only.

3.1 Loads for electrical tests

The EMV electrical tests require loads on the smart card interface pins. These are specified as follows.

	CLK Load	I/O Load	RST Load
To GND	100K Ω /30pF	250K Ω /30pF	100K Ω /30pF
To Vcc	100K Ω	100K Ω	100K Ω

Vcc Load (Icc) = 20mA \pm 5mA

Note: Resistive loads are considered worst case and are calculated for nominal VCC.

3.2 Operating Temperature:

The operating temperature range for implementing the 73S8024RN in EMV applications is between 0°C and 50°C. Reference EMV2000 Book1 section 1.2.1. Note: This temperature range corresponds to the ambient temperature of the unit under test. Internal temperatures of the unit under test may be higher. The 8024RN maximum operating temperature is 85 degrees C.

4 Electrical Tests.

The following section describes each electrical test called out in “EMVCo Type Approval Terminal Level 1Test Cases.” All tests are run over temperature unless otherwise noted.

The 8024RN supply voltages are nominal (3.3V for V_{DD} and 5.0V for V_{PC}) unless otherwise noted.

There are several scope captures of the signals under test. The captures are for reference only and were taken at ambient temperature using the loads indicated in section 3.1. When a voltage test is called, the scope is configured to average the repetitive signal to get the value. When a perturbation test is indicated, the scope is configured in an envelope capture configuration to indicate the full range of the signal. Each test allows for a small amount of error for the test equipment. This is typically 25mV for most voltage measurements unless otherwise noted. This error margin comes into play with the scope probe used to take the measurements used in this document. The following table shows the error when referenced to an accurate DVM.

Source	DVM	Scope Probe Offset	
0	-0.000004	-0.0122	-0.0122
3	2.9911	2.9857	-0.0054
5	4.9986	4.9952	-0.0034

4.1 Short circuit resilience - Test No. 1CB.001.0x

The objective of this test is to ensure that the 8024RN is not damaged by inter card slot contact short circuits or by short circuits between any 8024RN contacts and GND. The 8024RN was designed with this protection built in. This capability has been proven through testing.

4.2 V_{PP} Isolation - Test No. 1CB.002.00

The objective of this test is to ensure that the contact (C6) is isolated for new model terminals. V_{PP} is not implemented on the 8024RN. This test is not applicable.

4.3 V_{PP} Voltage - Test No. 1CB.003.0x

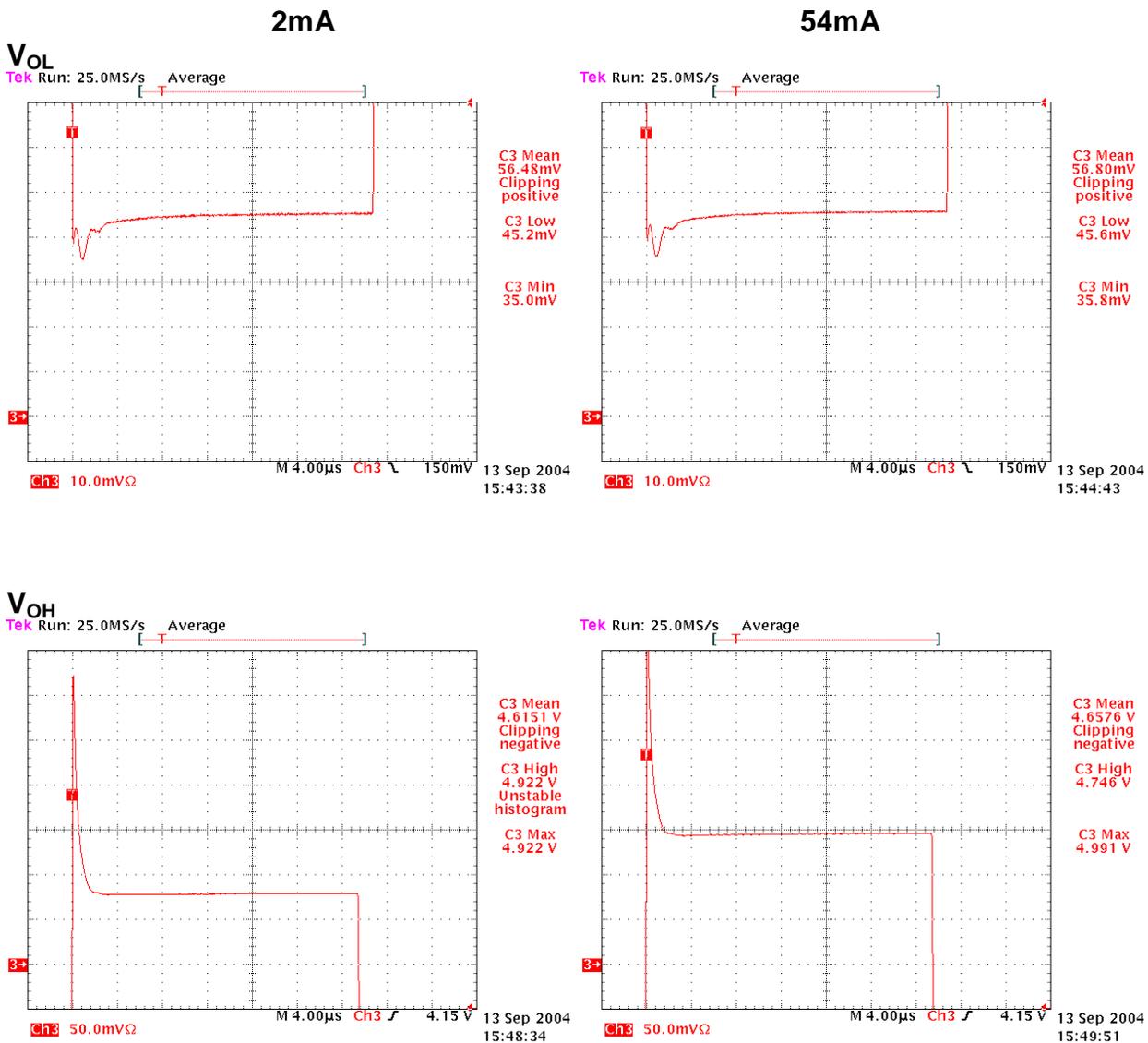
The objective of this test is to ensure that the voltage does not exceed the specified limit throughout a card session. V_{PP} is not implemented on the 8024RN. This test is not applicable.

4.4 I/O Current - Test No. 1CB.004.0x

The objective of this test is to ensure that the 8024RN limits the current flowing into or out of the I/O contact to specified limits. This test will place a 33Ω load from I/O to ground and V_{cc} (separately) while processing a command sequence (after successful reception of the ATR response). The current drawn through this resistor can't exceed 15mA before the card is de-activated (as a result of this increased load). This test is repeated for a steady state load on the card supply (V_{cc}) of 2mA and 54mA. The 8024RN data sheet specifies the maximum current for the I/O line at 15 mA with a load of 33Ω to both ground and V_{cc}.

4.5 I/O Transmission voltage - Test No. 1CB.005.0x

The objective of this test is to ensure that the signal high and low voltages are within specified limits. Like the I/O current test, this test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA while processing a command sequence. The I/O voltage is monitored and can't exceed $(0.8 \times V_{CC}) \leq V_{OH} \leq V_{CC}$ and $0V \leq V_{OL} \leq 0.4V$. The 8024RN data sheet specifies the limits as $(0.75 \times V_{CC}) \leq V_{OH} \leq V_{CC} + 0.1V$ and $V_{OL} \leq 0.3V$. Note: The datasheet spec is outside the EMV spec in regards to the min V_{OH} , however with the tighter constraints with regard to EMV (tighter temp range, 5V only card setting, etc.), the EMV specification has been met and proven through testing. This specification discrepancy applies to some other tests and has been shown to pass those EMV specs.



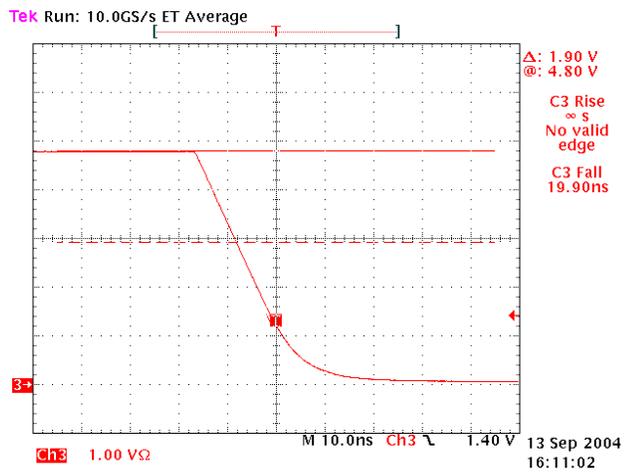
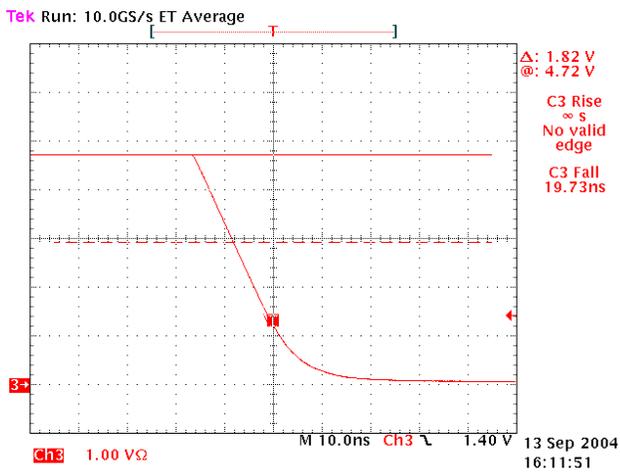
4.6 I/O Transmission rise and fall time - Test No. 1CB.006.0x

The objective of this test is to ensure that the signal rise and fall times are within specified limits. This test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA and while processing a command sequence. The rise and fall times are measured between 10% and 90% of each edge. The limits are $t_R/ t_F \leq 0.8\mu s$. The 8024RN data sheet specifies the limits as $t_R/ t_F \leq 0.1\mu s$.

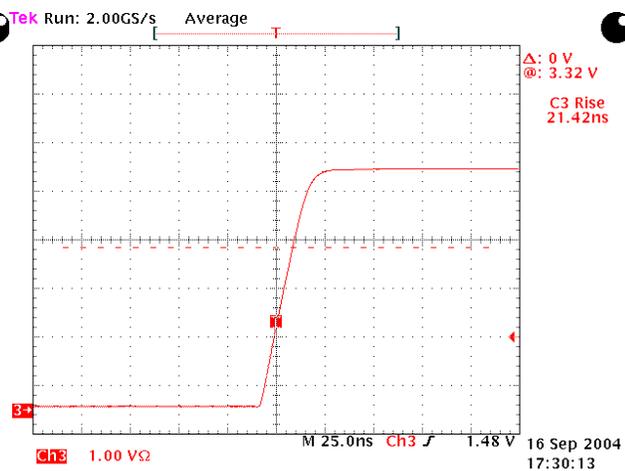
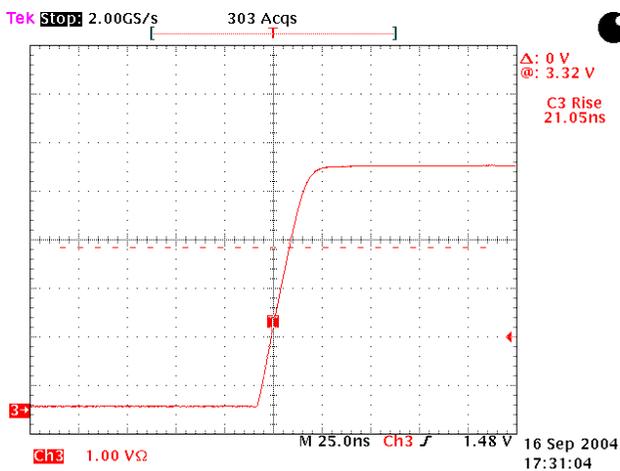
2mA

54mA

t_f

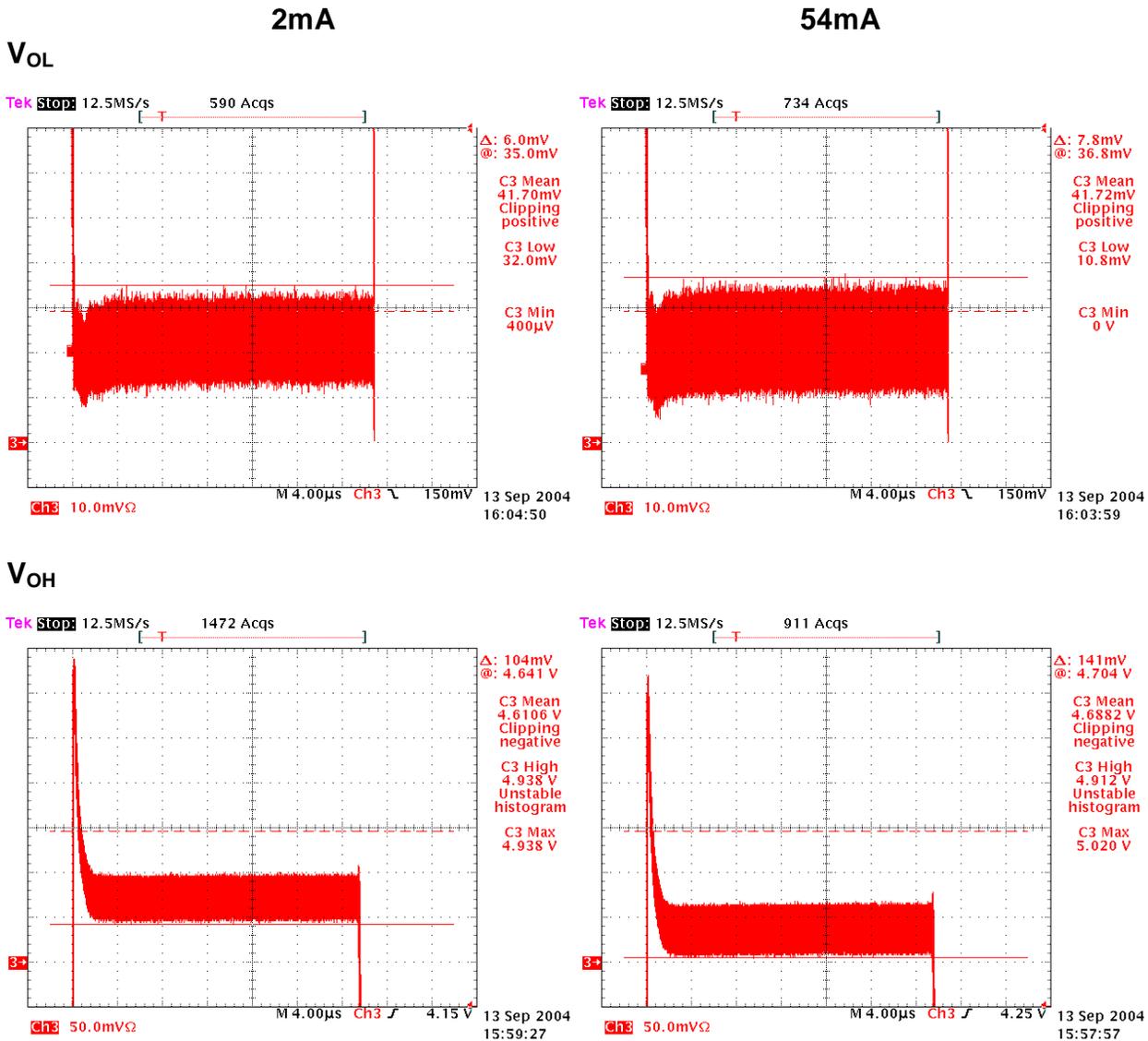


t_r



4.7 I/O transmission signal perturbations - Test No. 1CB.007.0x

The objective of this test is to ensure that the signal perturbations are within specified limits. This test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA and while processing a command sequence. The I/O voltage is monitored and can't exceed $(0.8 \times V_{cc}) \leq V_{OHinst} \leq (V_{cc} + 0.25V)$ and $-0.25V \leq V_{OLinst} \leq 0.4V$. The 8024RN data sheet specifies the limits as $(0.75 \times V_{cc}) \leq V_{OH} \leq V_{cc} + 0.1V$ and (not specified) $\leq V_{OL} \leq 0.3V$.

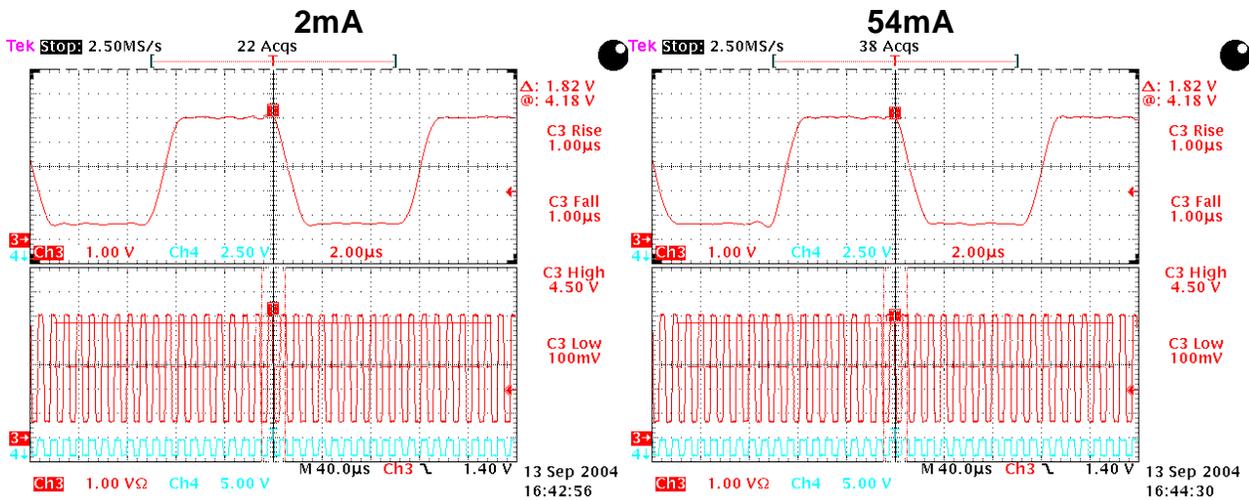


4.8 I/O reception voltage - Test No. 1CB.008.0x

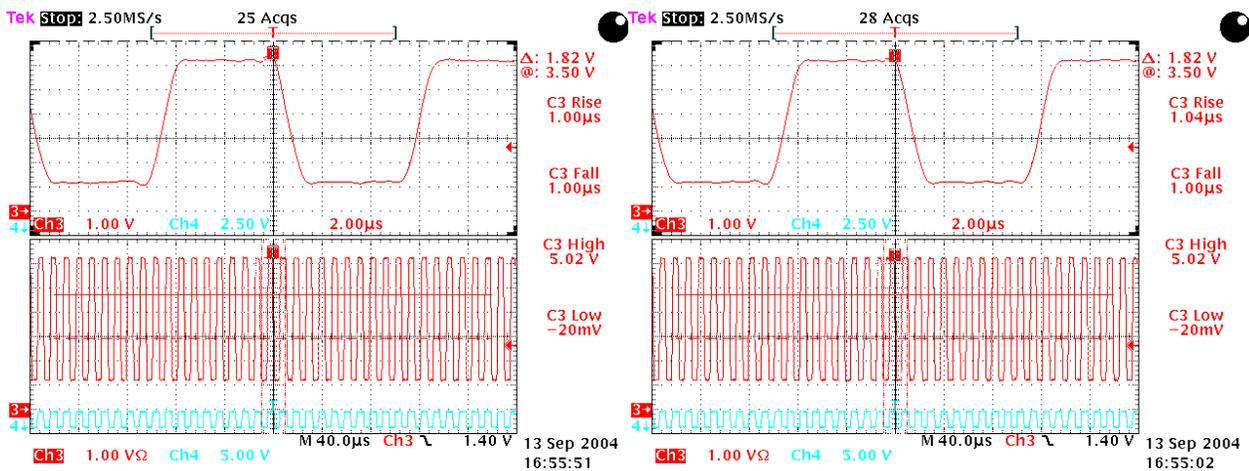
The objective of this test is to ensure that the 8024RN correctly interprets the I/O signals from the card interface. This test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA and while processing a command sequence. The card interface will simulate a command sequence with the following conditions:

The following diagrams show the I/O input (top) and I/OUC output (bottom) of the lower half of the capture. There are no missed I/O pulses on the I/OUC output. The upper half is a zoom on the I/O input that reflects the input conditions specified.

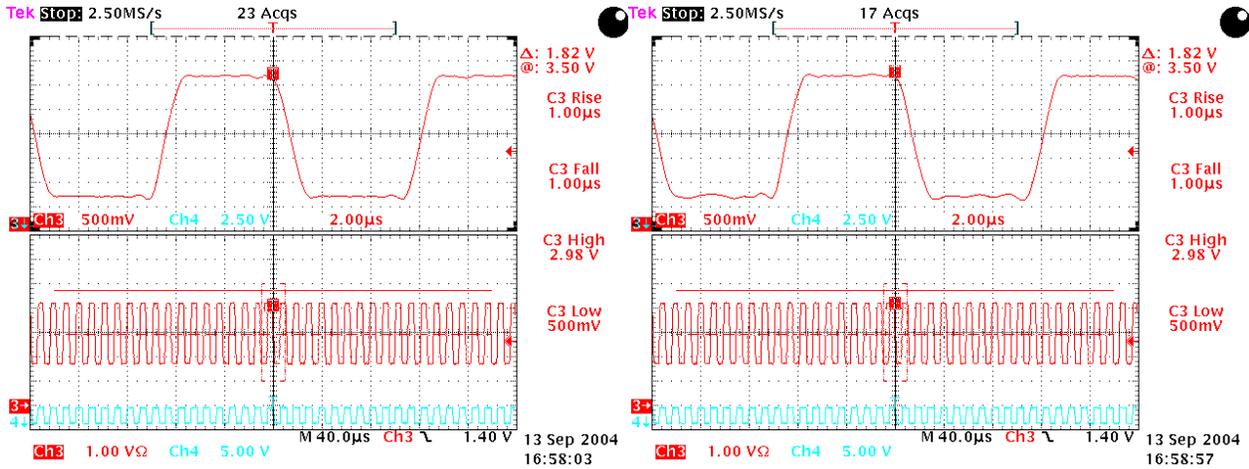
- $V_{IH} = (0.9 \times V_{cc})$ and $V_{IL} = 0.1V$ ($t_R/t_F < 0.1\mu s$)



- $V_{IH} = V_{cc}$ and $V_{IL} = 0V$ ($t_R/t_F < 0.1\mu s$)



- $V_{IH} = (0.6 \times V_{CC})$ and $V_{IL} = 0.5V$ ($t_R / t_F < 0.1\mu s$)

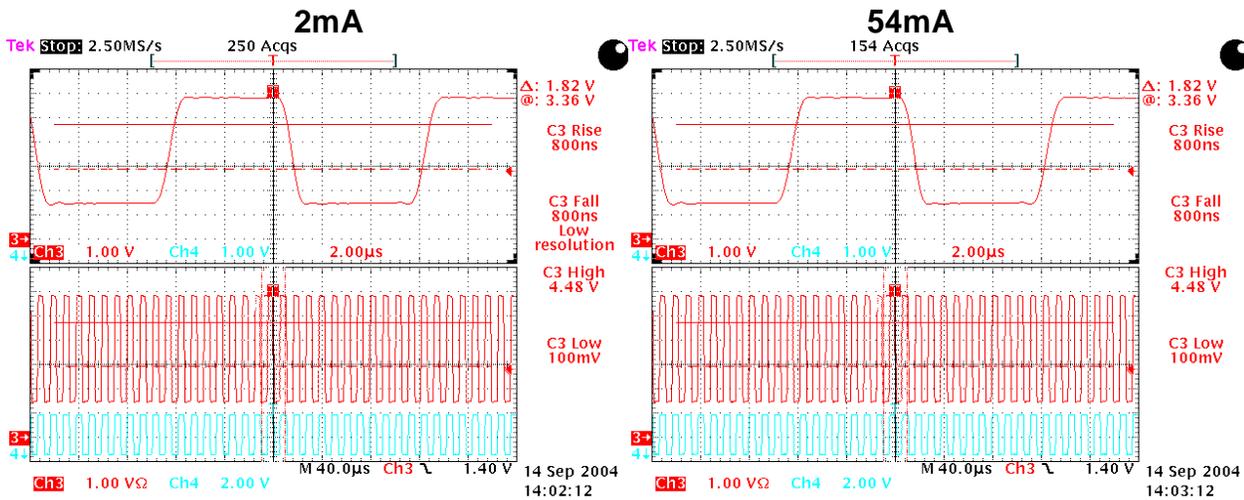


This test passes when the command sequence is properly executed with these logic levels. The 8024RN data sheet specifies the limits as $1.8V \leq V_{IH} \leq V_{CC}$ and $-0.3V \leq V_{IL} \leq 0.8V$

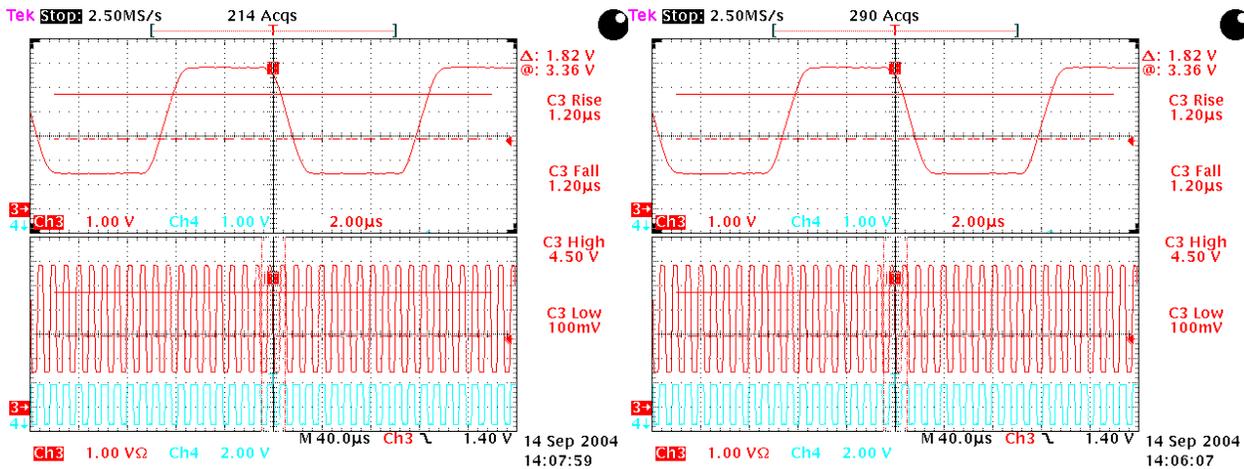
4.9 I/O reception rise and fall times - Test No. 1CB.009.0x

The objective of this test is to ensure that the 8024RN correctly interprets (as logic high or low as appropriate) signals from the card interface having rise and fall times as defined below. This test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA and while processing a command sequence.

- t_R & $t_F \leq 0.1\mu s$ ($\pm 0.01\mu s$), $V_{IH} = (0.9 \times V_{CC})$ and $V_{IL} = 0.1V$



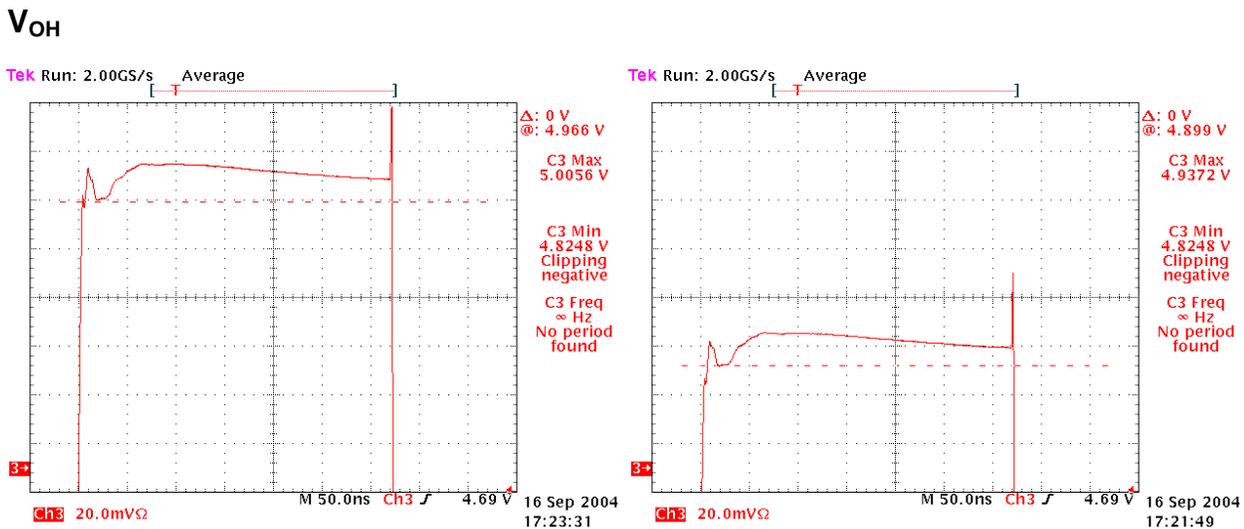
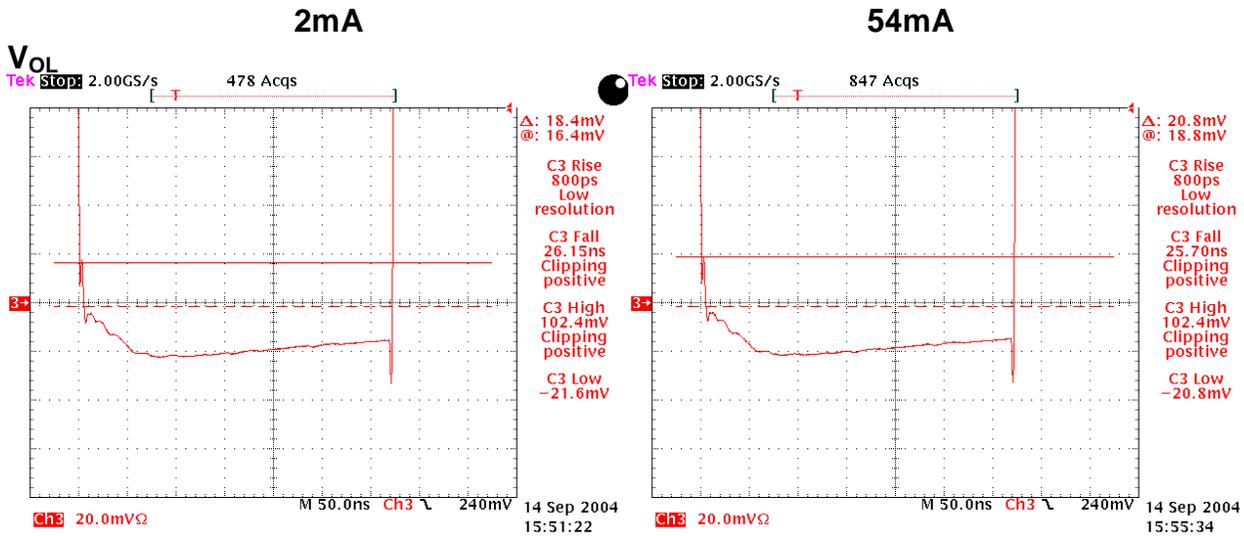
- t_R & $t_F = 1.2\mu s$ ($\pm 0.01\mu s$), $V_{IH} = (0.9 \times V_{CC})$ and $V_{IL} = 0.1V$



This test passes when the command sequence is properly executed with these logic levels. The 8024RN data sheet specifies the limits as t_R & $t_F \leq 1\mu s$.

4.10 CLK voltage - Test No. 1CB.010.0x

The objective of this test is to ensure that the signal high and low voltages generated by the 8024RN are within specified limits. This test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA and while processing a command sequence. The CLK voltage is monitored and can't exceed $(V_{cc} - 0.5V) \leq V_{OH} \leq V_{cc}$ and $0V \leq V_{OL} \leq 0.4V$. The 8024RN data sheet specifies the limits as $0.9 V_{cc} \leq V_{OH} \leq V_{cc}$ and $0v \leq V_{OL} \leq 0.3V$.



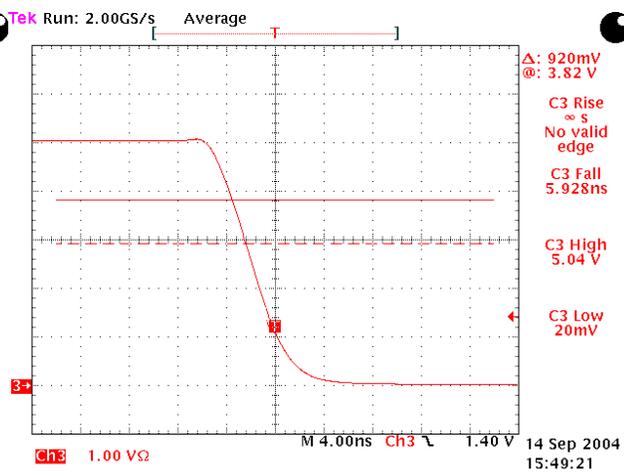
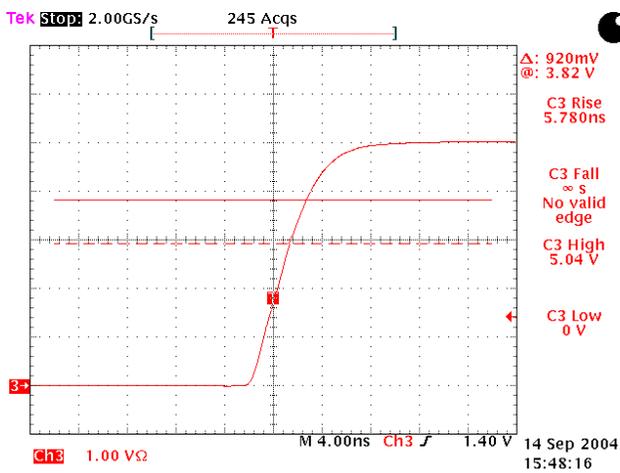
4.11 CLK rise and fall times - Test No. 1CB.011.0x

The objective of this test is to ensure that the signal rise and fall times are within specified limits. This test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA and while processing a command sequence. The rise and fall times are measured between 10% and 90% of each edge. The limits are $t_R/t_F \leq 8\%$ of the clock period. The 8024RN data sheet specifies the limits as $t_R/t_F \leq 8$ ns. If for example, the clock is running at 5MHz (EMV max.), then 8% of the clock period is 16ns.

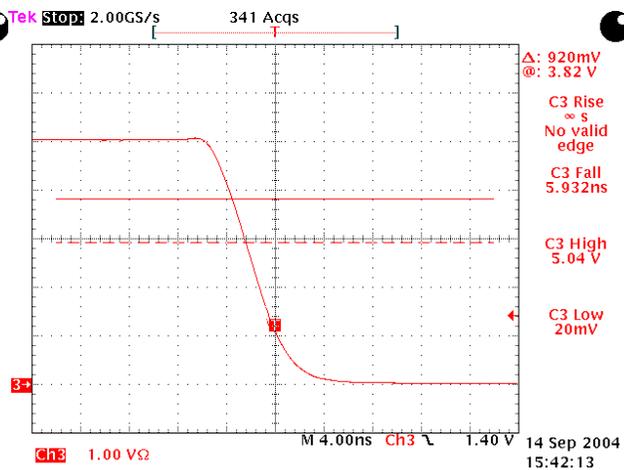
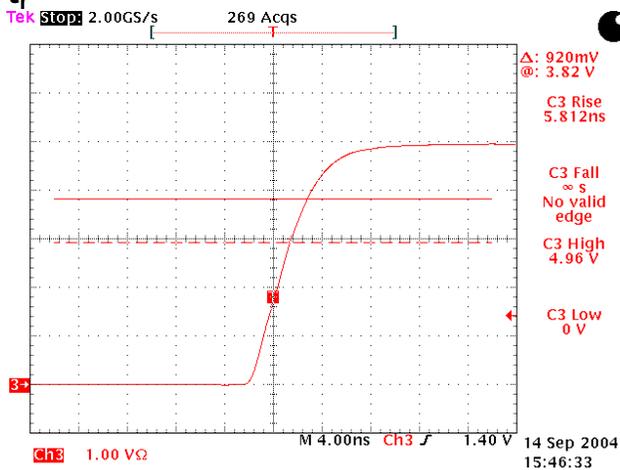
2mA

54mA

t_f

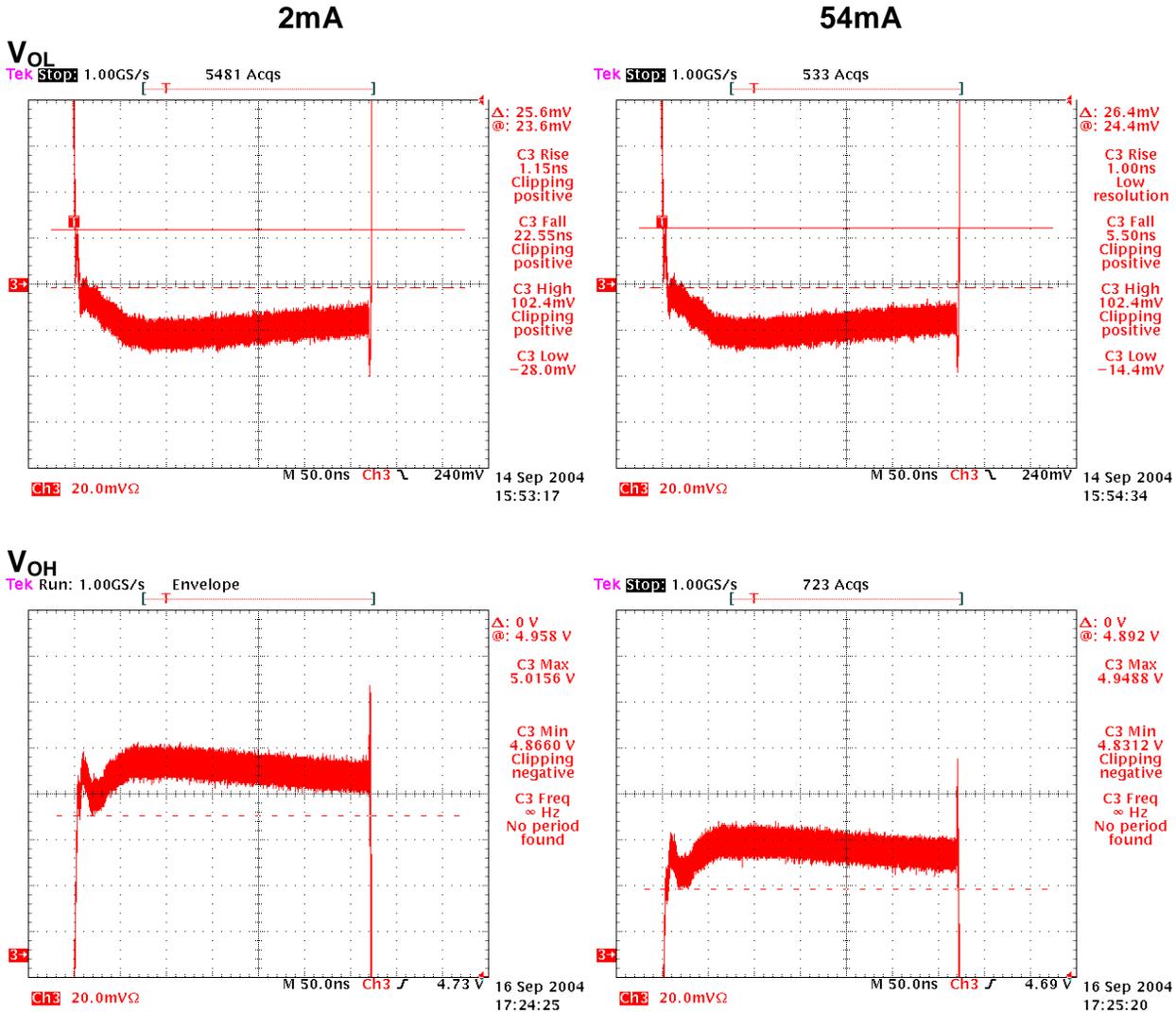


t_r



4.12 CLK signal perturbations - Test No. 1CB.012.0x

The objective of this test is to ensure that the signal perturbations are within specified limits. This test is run with a steady state load on the card supply (V_{cc}) of 2mA and 54mA and while processing a command sequence. The CLK voltage is monitored and can't exceed $(V_{cc} - 0.5V) \leq V_{OHinst} \leq (V_{cc} + 0.25V)$ and $-0.25V \leq V_{OLinst} \leq 0.4V$. The 8024RN data sheet specifies the limits as $(0.9 \times V_{cc}) \leq V_{OH} \leq V_{cc}$ and $0V \leq V_{OL} \leq 0.3V$.



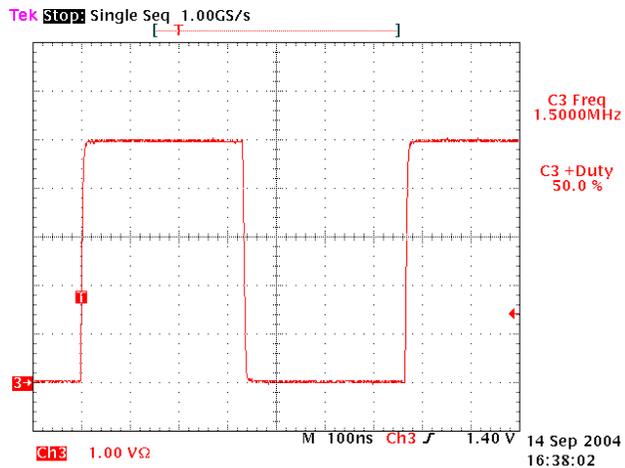
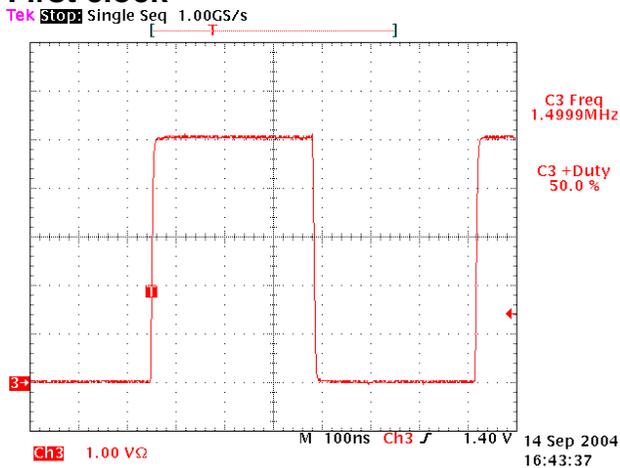
4.13 CLK Frequency and duty cycles - Test No. 1CB.013.0x

The objective of this test is to ensure that the clock frequency, stability, and duty cycle are within specified limits. This test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA and while processing a command sequence. This test measures frequency and duty cycle 10 times at 50ms intervals from CLK start. The CLK frequency should be in the range of $1\text{MHz} \leq \text{average frequency} \leq 5\text{MHz}$ with a frequency variation $\leq 1\%$ of the average frequency. The duty cycle should be between 45% and 55% of the signal period. The 8024RN data sheet specifies the limits as up to 20 MHz with a duty cycle between 45% and 55%.

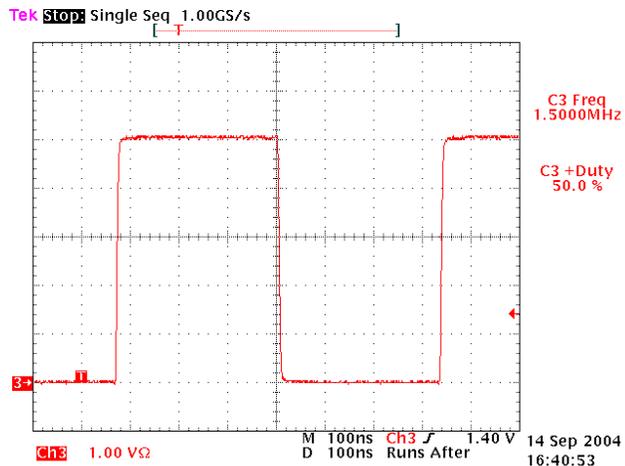
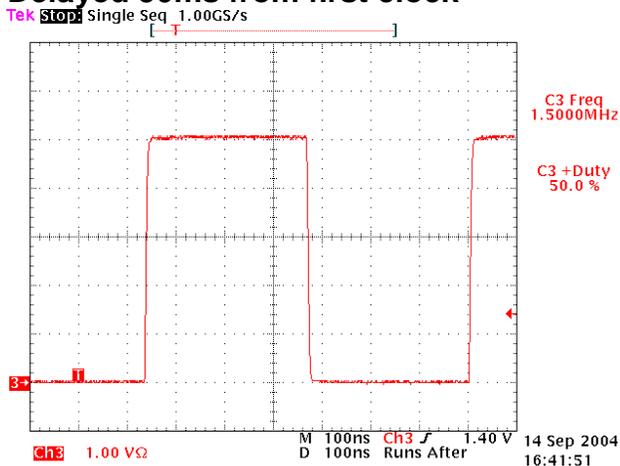
2mA

54mA

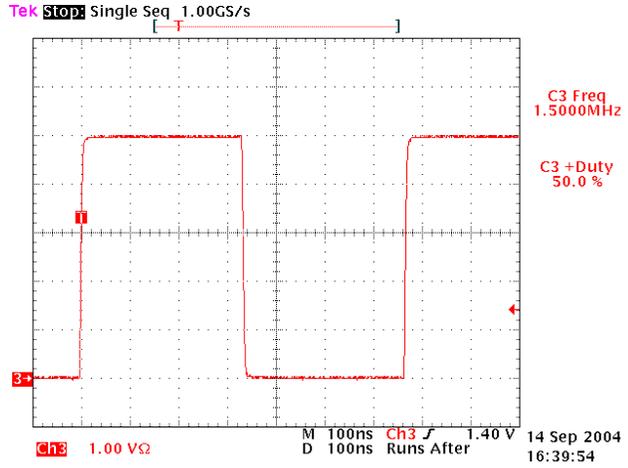
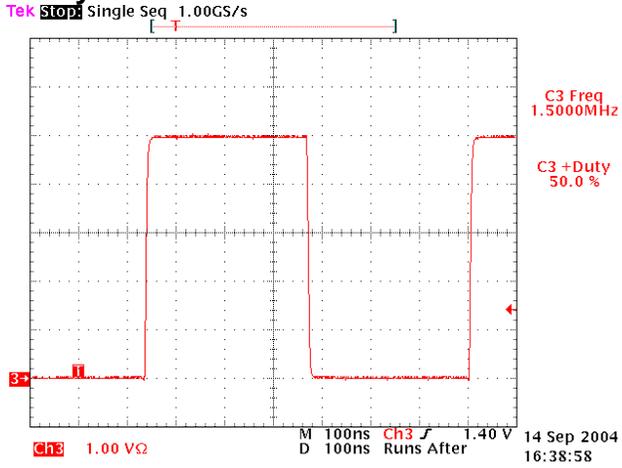
First clock



Delayed 50ms from first clock

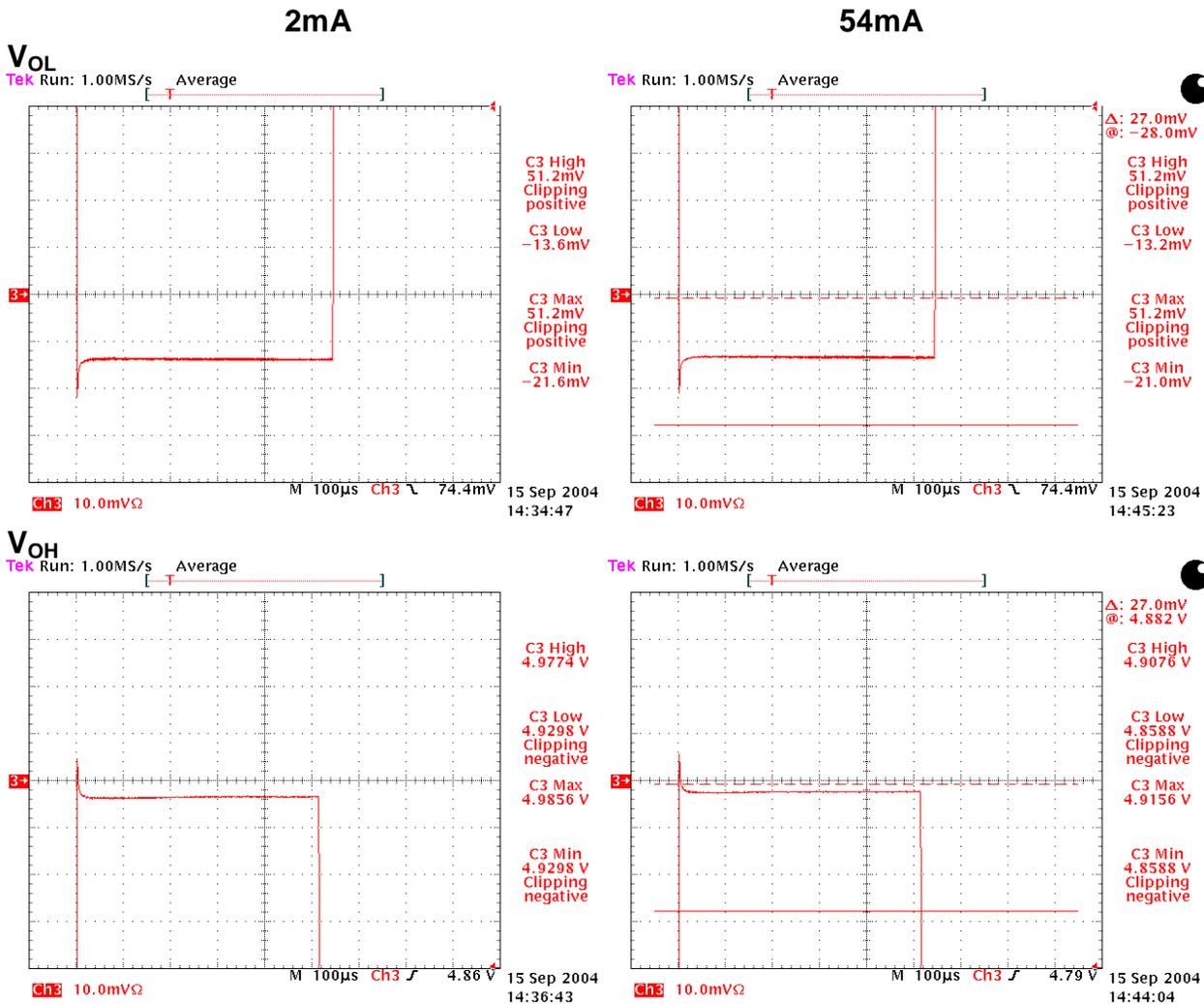


Delayed 500ms from first clock



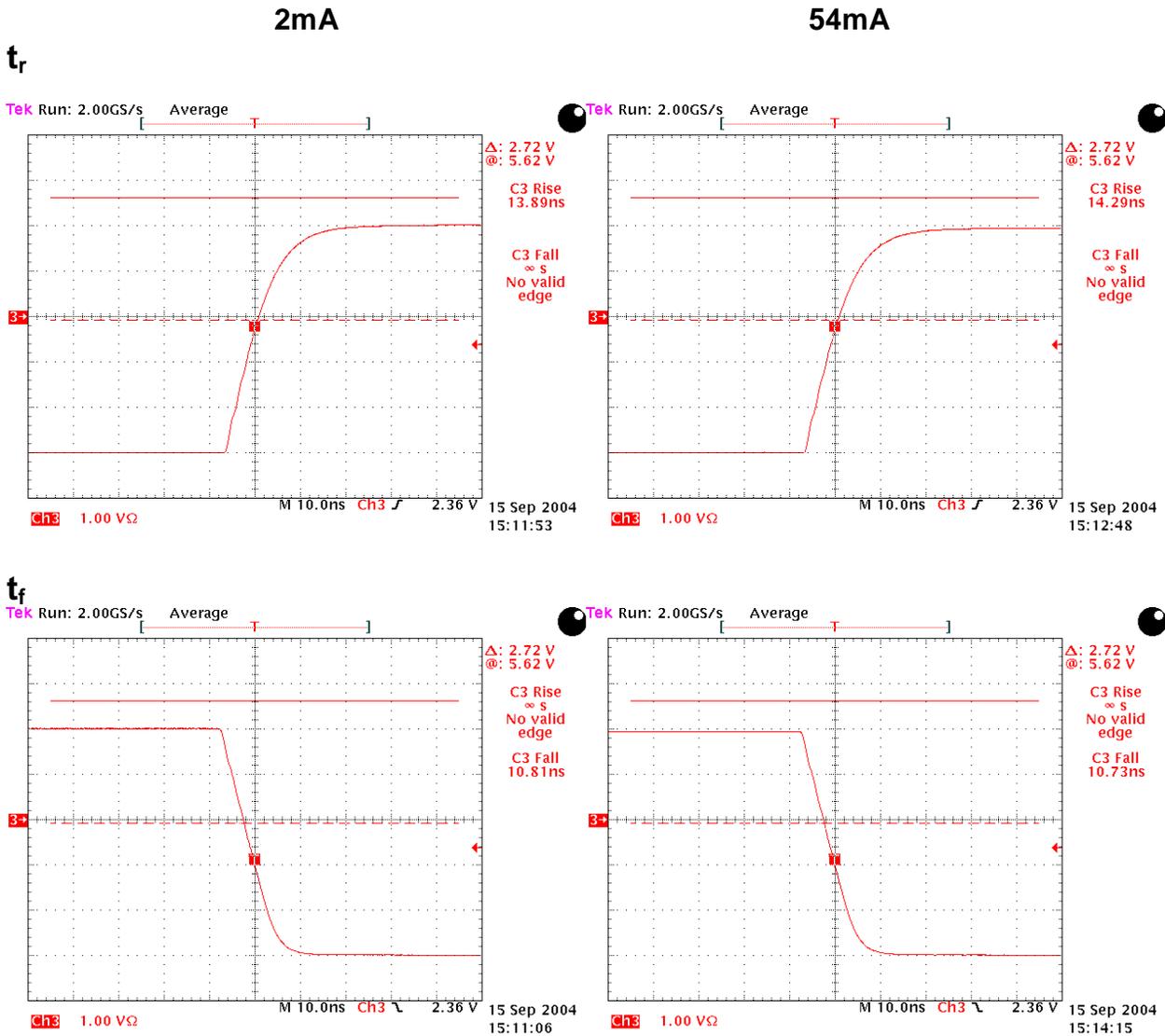
4.14 RST voltage - Test No. 1CB.014.0x

The objective of this test is to ensure that the steady state signal low and high voltages generated by the 8024RN are within specified limits. This test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA and while processing a command sequence. This test monitors VOL before RST low to high transition and VOH afterwards. The RST voltage is monitored and can't exceed $(V_{cc} - 0.5V) \leq V_{OH} \leq V_{cc}$ and $0V \leq V_{OL} \leq 0.4V$. The 8024RN data sheet specifies the limits as $0.9 V_{cc} \leq V_{OH} \leq V_{cc}$ and $0v \leq V_{OL} \leq 0.3V$.



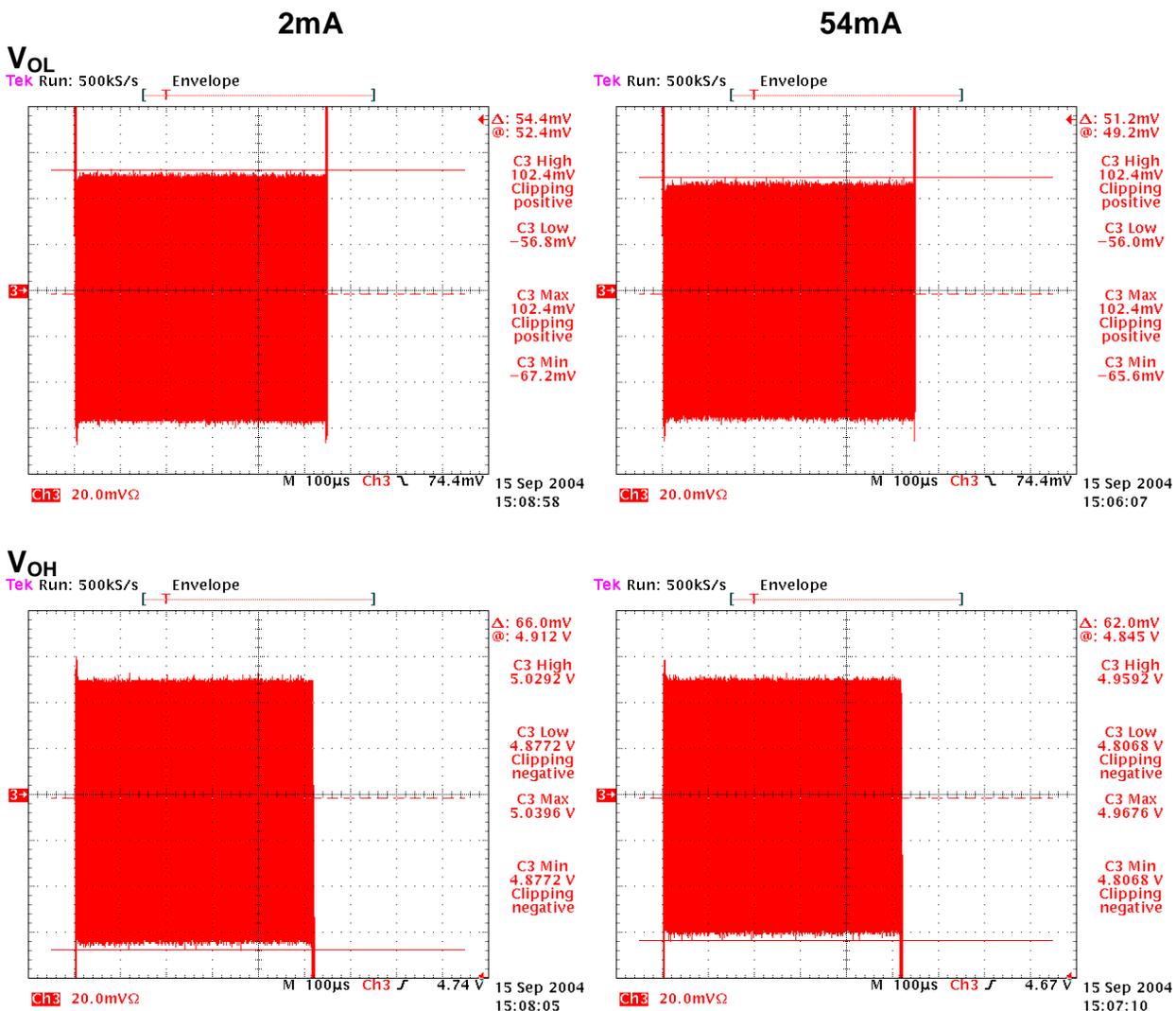
4.15 RST rise and fall times - Test No. 1CB.015.0x

The objective of this test is to ensure that the signal rise and fall times are within specified limits. This test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA. The rise and fall times are measured between 10% and 90% of each edge. This test is repeated 10 times for all conditions. The limits are $t_R/t_F \leq 0.8 \mu s$. The 8024RN data sheet specifies the limits as $t_R/t_F \leq 100 ns$.



4.16 RST signal perturbations - Test No. 1CB.016.0x

The objective of this test is to ensure that the signal perturbations are within specified limits. This test is run with a steady state load on the card supply (V_{CC}) of 2mA and 54mA. A low to high transition is initiated on RST. Its voltage is monitored for $5\mu s$ (+5%) from the 90% point of the rising edge. It can't exceed $(V_{CC} - 0.5V) \leq V_{OHinst} \leq (V_{CC} + 0.25V)$. A high to low transition is initiated on RST. Its voltage is monitored for $5\mu s$ (+5%) from the 10% point of the falling edge. It can't exceed $-0.25V \leq V_{OLinst} \leq 0.4V$. This will initiate an ATR. After the ATR completes, a command sequence needs to be initiated. RST is monitored for V_{OHinst} during reception of the first two bytes of the ATR and must not exceed $(V_{CC} - 0.5V) \leq V_{OHinst} \leq (V_{CC} + 0.25V)$. RST is monitored for V_{OHinst} during transmission of the first two bytes of the command header and must not exceed $(V_{CC} - 0.5V) \leq V_{OHinst} \leq (V_{CC} + 0.25V)$. This test is repeated 10 times for all conditions. The 8024RN data sheet specifies the limits as $(0.9 \times V_{CC}) \leq V_{OH} \leq V_{CC}$ and $0V \leq V_{OL} \leq 0.3V$.



4.17 VCC Contact voltage - Test No. 1CB.017.0x

The objective of this test is to ensure that the supply voltage generated by the IUT remains within specified limits over a range of applied load conditions. This test is run with a steady state load on the card supply (Vcc) of 1mA, 25mA and 54mA and while processing a command sequence. Vcc is tested with the VPC voltage at 4.75, 5.0 and 5.5 volts. Monitor Vcc throughout the processing of the command sequence and verify that it doesn't exceed $0V \leq V_{cc} \leq 0.4V$ when off and $4.6V \leq V_{cc} \leq 5.4V$ when on. The 8024RN data sheet specifies the limits as $0V \leq V_{cc} \leq 0.4V$ when inactive and $4.6V \leq V_{cc} \leq 5.25V$ when active.

Vcc -Off	1mA		25mA		54mA	
Vpc	min (mV)	max (mV)	min (mV)	max (mV)	min (mV)	max (mV)
4.75	-27.2	-2	-28	-3.2	-27.2	-2.8
5	-28	-2	-28	-3.2	-28	-2.8
5.5	-28	-3.2	-28	-3.2	-28	-2.8

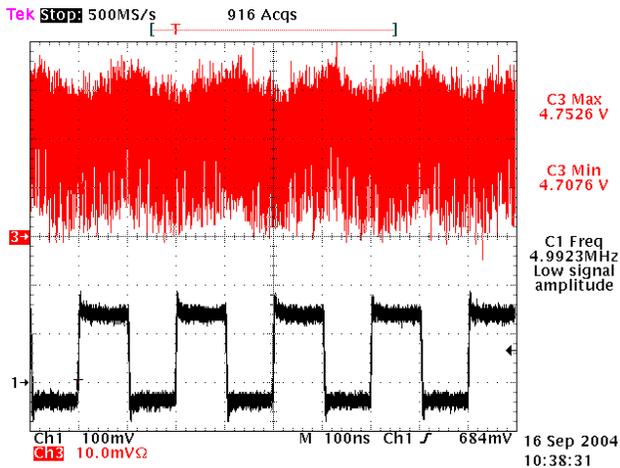
Vcc -On	1mA		25mA		54mA	
Vpc	min (V)	max (V)	min (V)	max (V)	min (V)	max (V)
4.75	4.704	4.781	4.682	4.751	4.655	4.700
5	4.954	5.006	4.865	4.956	4.755	4.922
5.5	4.981	5.048	4.865	5.001	4.816	4.986

4.18 Transients neutralization on VCC - Test No. 1CB.018.0x

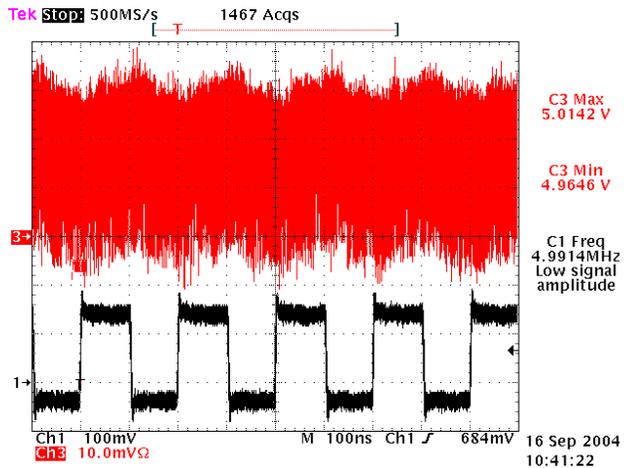
The objective of this test is to ensure that the supply voltage generated by the IUT remains within specified limits under dynamic load conditions. This test is run with a load on the card supply (Vcc) of 1mA, 25mA and 54mA and while processing a command sequence. A transient load is modulated with a square wave current drain pulses of 20 mA at a frequency of 5 MHz with a duty cycle of 50 %. It is also modulated at peak of 95 mA of fixed 400ns duration, activated at a frequency, which vary with an asynchronous sequence at 2 kHz. Monitor Vcc throughout the processing of the command sequence and verify that it doesn't exceed $0V \leq V_{cc} \leq 0.4V$ when off and $4.6V \leq V_{cc} \leq 5.4V$ when on. The 8024RN data sheet specifies the limits as $0V \leq V_{cc} \leq 0.4V$ when inactive and $4.6V \leq V_{cc} \leq 5.25V$ when active.

Only the ON states are shown. The upper signal is VCC and the lower signal is the modulating signal for the load current. This modulation is run at 5MHz.

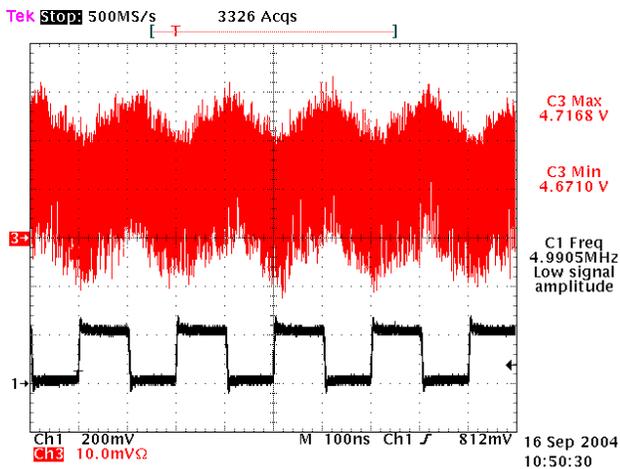
1mA/20mA @ 4.75V



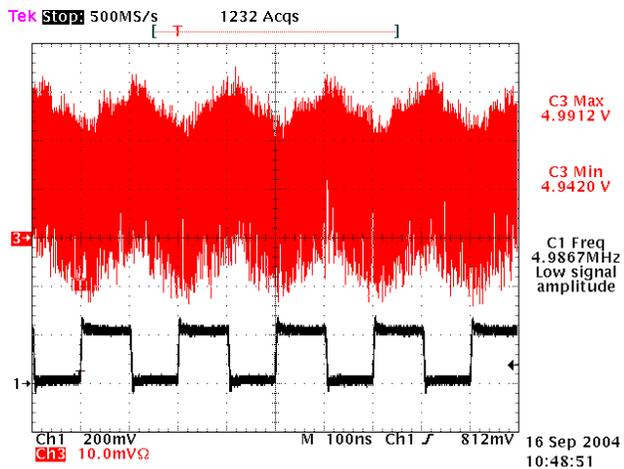
54mA/20mA @ 4.75V



1mA/20mA @ 5.5V

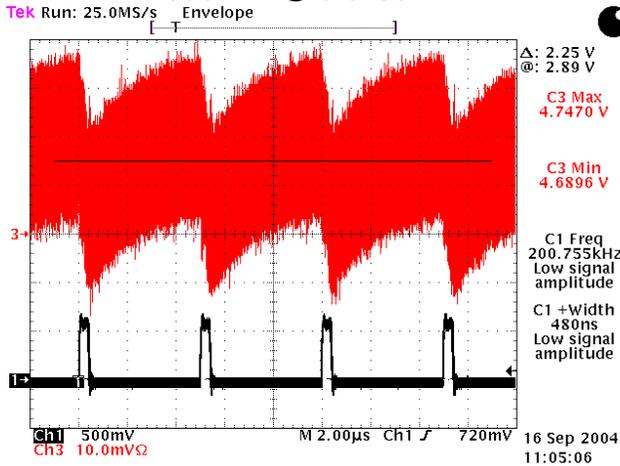


54mA/20mA @ 5.5V

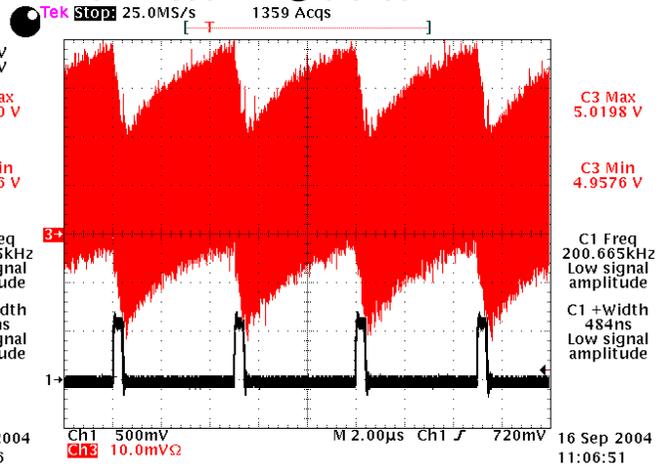


The upper signal is VCC and the lower signal is the modulating signal for the load current. This modulation is run at 2KHz with a pulse width of 400ns. Note the pulse width on the captures is shown higher than 400ns. This is because of the envelope mode of the scope causes it to appear wider than it actually is.

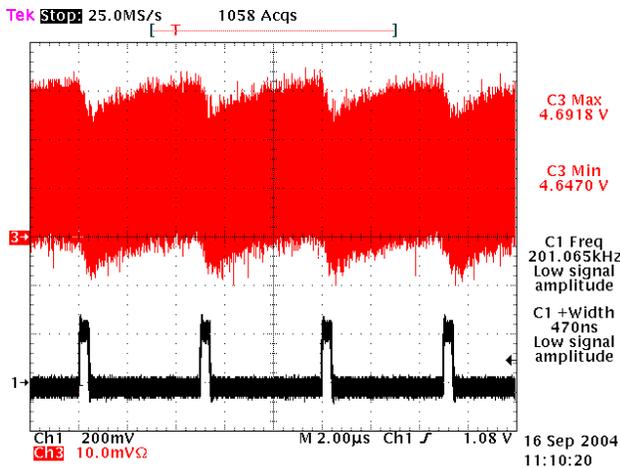
1mA/95mA @ 5.5V/5MHz



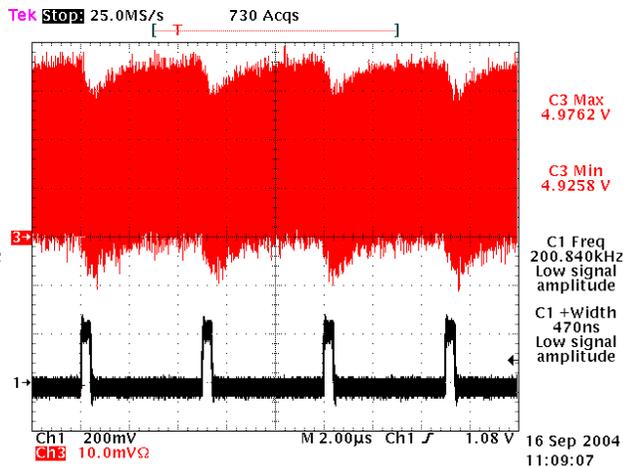
54mA/95mA @ 5.5V/5MHz



1mA/95mA @ 5.5V



54mA/95mA @ 5.5V



5 Card Session Tests

5.1 Contact Activation Sequence - Test No. 1CC.001.0x

The objective of this test is to ensure that the 8024RN signals are activated according to the defined sequence when a card is inserted into the card interface. This test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA. The test will initiate a cold reset for the activation sequence.

- V_{RST} , V_{CLK} and $V_{I/O}$ are monitored for $\geq 1ms$ prior to $V_{CC} \geq 0.4V$. These voltages shall not exceed $0V \leq V_{RST} \leq 0.4V$, $0V \leq V_{CLK} \leq 0.4V$, and $0V \leq V_{I/O} \leq 0.4V$. Measurement T1
- V_{RST} , V_{CLK} and $V_{I/O}$ are monitored from $V_{CC} \geq 0.4V$ until $V_{CC} \geq 4.6V$. These voltages shall not exceed $0V \leq V_{RST} \leq 0.4V$, $0V \leq V_{CLK} \leq 0.4V$ and $0V \leq V_{I/O} \leq V_{CC}$. Measurement T2
- V_{CC} , V_{RST} and $V_{I/O}$ are monitored from $V_{CC} \geq 4.6V$ until $V_{CLK} \geq 0.4V$ (for the first CLK transition). These voltages shall not exceed $4.6V \leq V_{CC} \leq 5.4V$, $0V \leq V_{RST} \leq 0.4V$ and $0V \leq V_{I/O} \leq V_{CC}$. Measurement T3
- V_{CC} , V_{RST} and $V_{I/O}$ are monitored for a time period equivalent to 200 CLK cycles from $V_{CLK} \geq 4.6V$ (for the first CLK transition). These voltages shall not exceed $4.6V \leq V_{CC} \leq 5.4V$, $0V \leq V_{RST} \leq 0.4V$, $0V \leq V_{I/O} \leq V_{CC}$, $4.6V \leq V_{CLK} \leq 0.4V$. Measurement T4
- V_{CC} and $V_{I/O}$ are monitored after 200 CLK cycles from $V_{CLK} \geq 4.6V$ (for the first CLK transition) until $V_{RST} \geq 0.4V$. These voltages shall not exceed $4.6V \leq V_{CC} \leq 5.4V$ and $(0.8 \times V_{CC}) \leq V_{I/O} \leq V_{CC}$, $4.6V \leq V_{CLK} \leq 0.4V$. Measurement T5

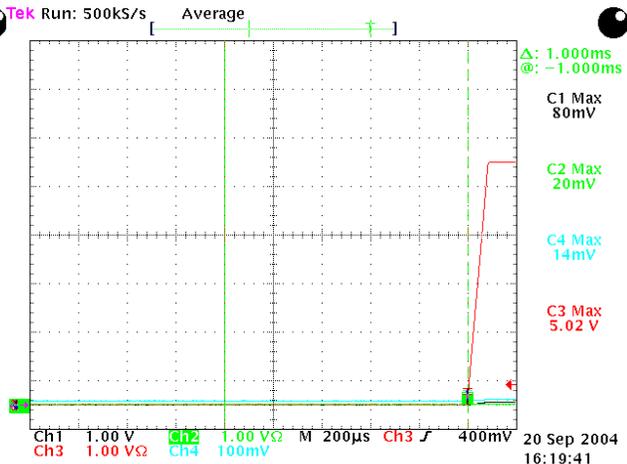
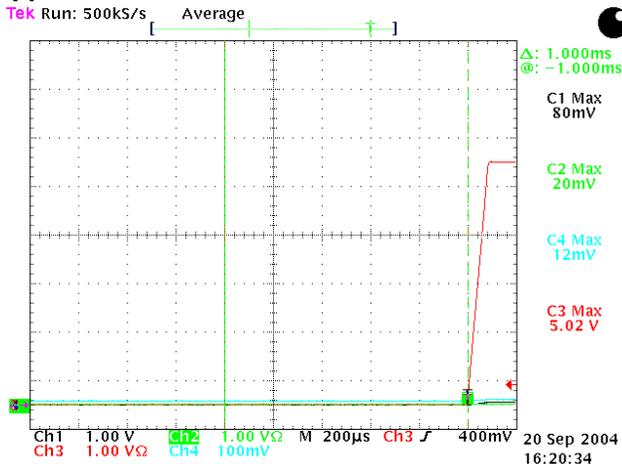
The test is repeated 10 times for all combinations of temperature and load current.

Black – I/O
 Green – CLK
 Blue – RST
 Red - Vcc

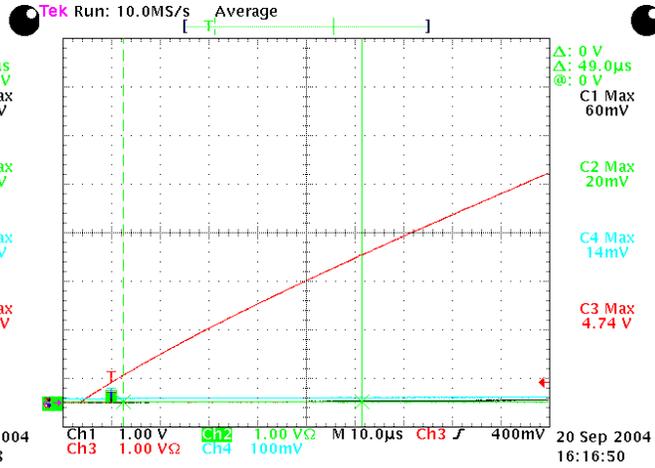
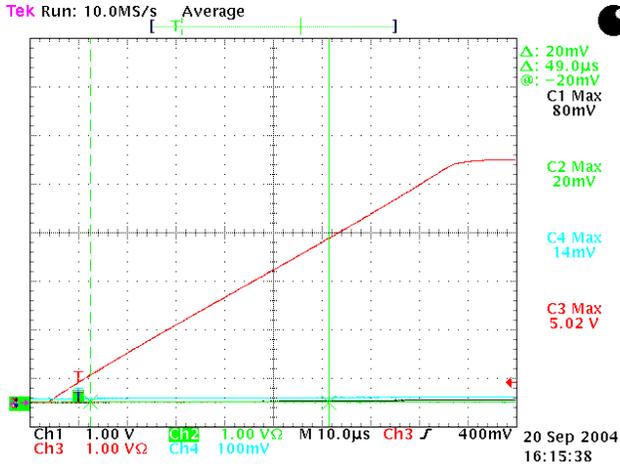
2mA

54mA

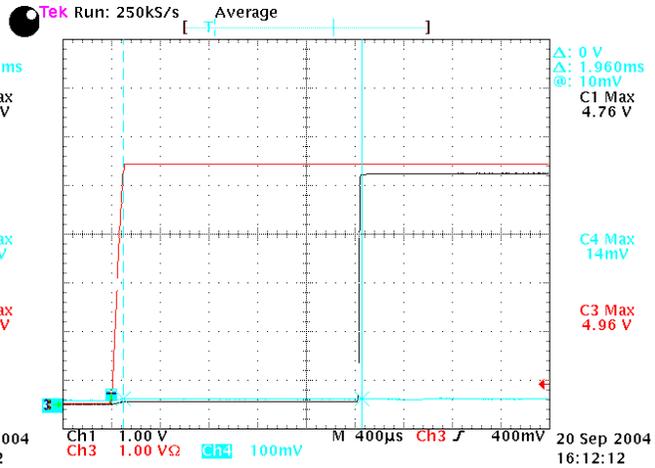
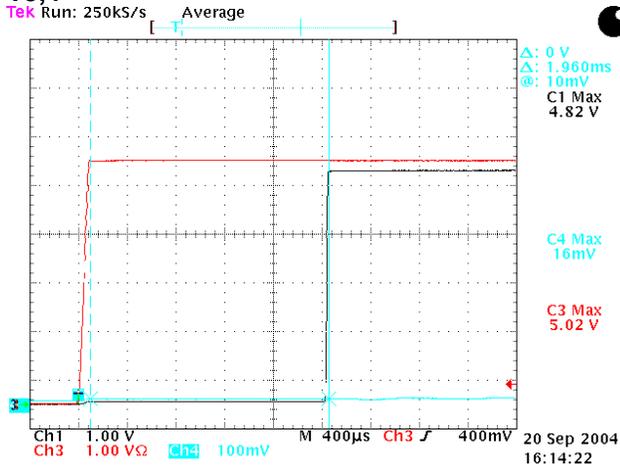
T1



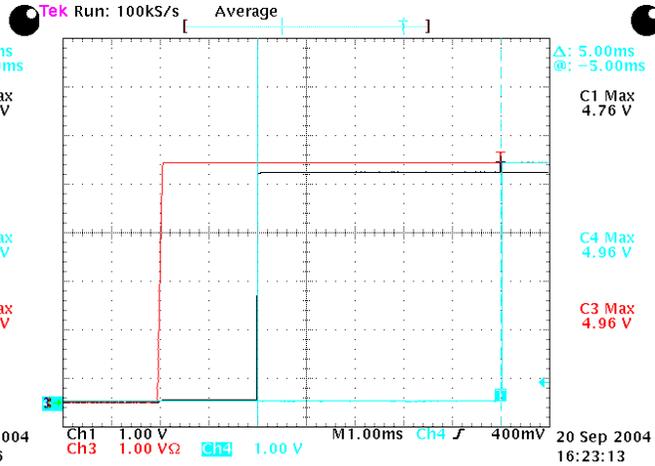
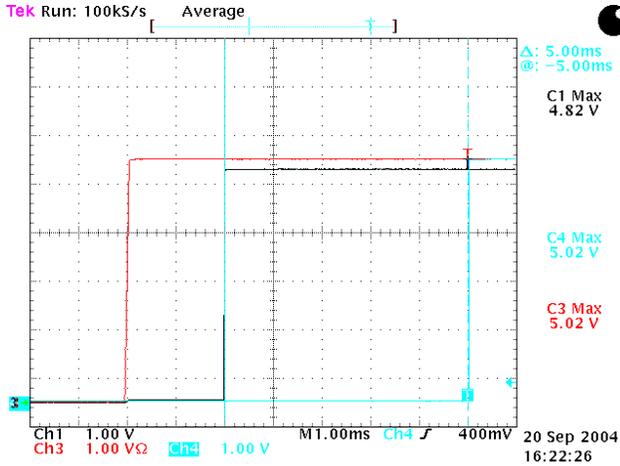
T2



T3,4



T5



5.2 Contact Deactivation Sequence - Test No. 1CC.002.0x

The objective of this test is to ensure that the 8024RN signals are deactivated according to the defined sequence. This test is run with a steady state load on the card supply (Vcc) of 2mA and 54mA. The test will initiate a cold reset for the activation sequence, but the card interface will not return an ATR, which will initiate deactivation sequence.

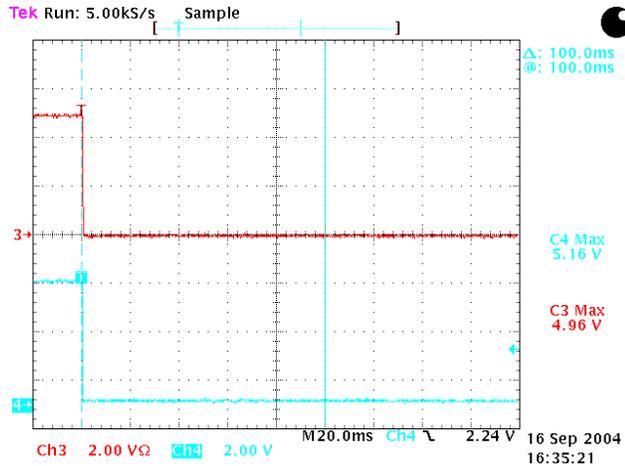
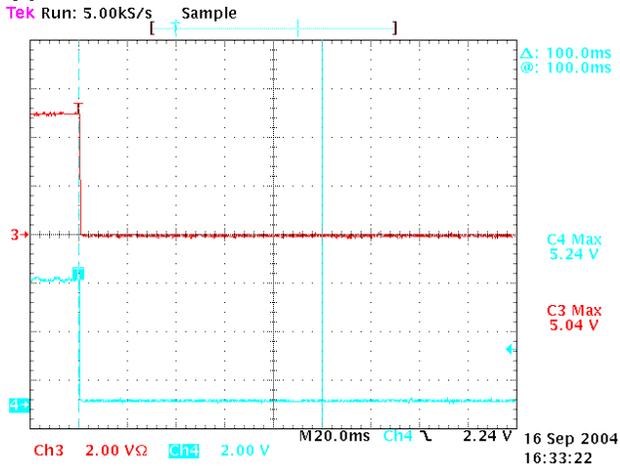
- The time from $V_{RST} \leq 0.4V$ until $V_{CC} \leq 0.4V$ is measured. This time must be $\leq 100ms$. Measurement T1
- V_{RST} is monitored from $V_{RST} \leq 0.4V$ until $V_{CC} \leq 4.6V$. This voltage shall not exceed $0V \leq V_{RST} \leq 0.4V$. Measurement T2
- V_{CLK} , V_{RST} and $V_{I/O}$ are monitored from $V_{CC} \leq 4.6V$ until $V_{CC} \leq 0.4V$. These voltages shall not exceed $0V \leq V_{CLK} \leq 0.4V$, $0V \leq V_{RST} \leq 0.4V$ and $0V \leq V_{I/O} \leq (V_{CC} + 0.25V)$. Measurement T3
- V_{CC} , V_{CLK} , V_{RST} and $V_{I/O}$ are monitored from $V_{CC} \leq 0.4V$ for 100mS. These voltages shall not exceed $0V \leq V_{CC} \leq 0.4V$, $0V \leq V_{CLK} \leq 0.4V$, $0V \leq V_{RST} \leq 0.4V$ and $0V \leq V_{I/O} \leq 0.4V$. Measurement T4

Black – I/O
 Green – CLK
 Blue – RST
 Red - Vcc

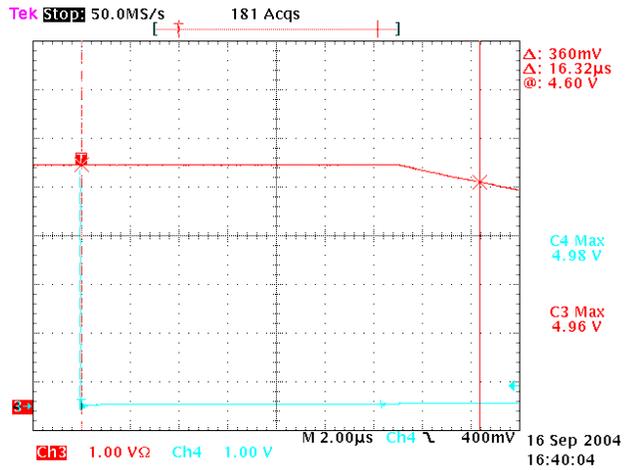
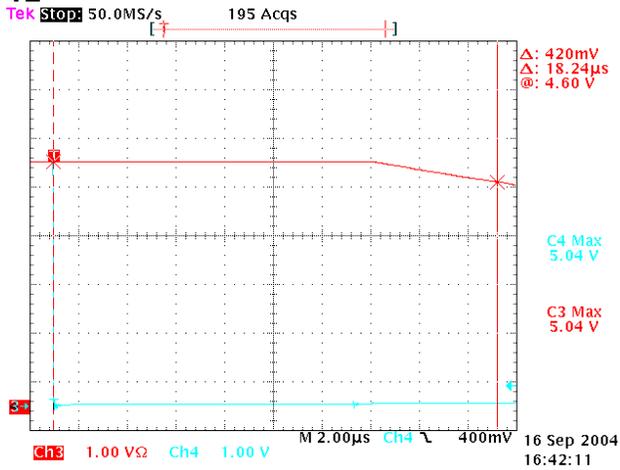
2mA

54mA

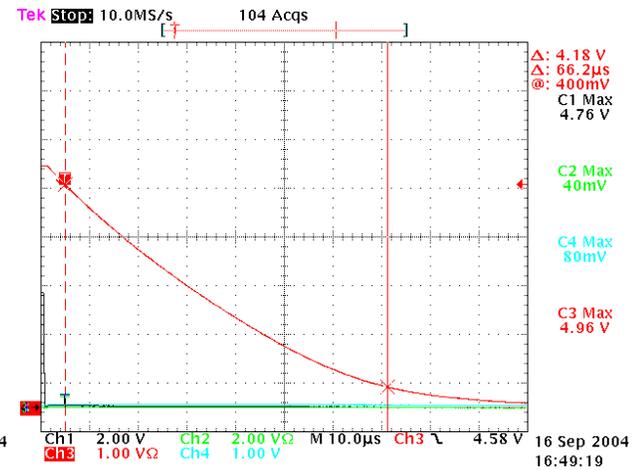
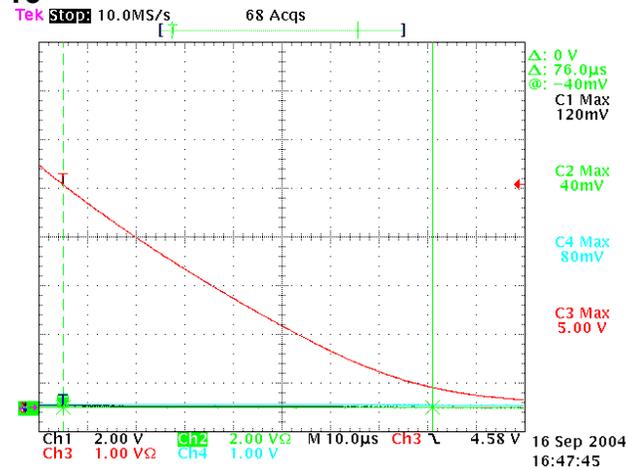
T1



T2



T3



T4

