Data Sheet

ADSD3500

Time-of-Flight Depth Image Signal Processor

FEATURES

- Depth processor for Analog Devices, Inc., Time-of-Flight imagers
- Full-depth processing at 640 x 512 resolution, up to 90 frames per second (FPS)
- Partial depth processing at 1024 x 1024 resolution, up to 30 FPS
- On-chip static random access memory (SRAM) for frame buffering and manipulation
- Arm Cortex-M33 processor for data flow control
- 4-lane MIPI CSI-2 receiver interface, 2.5 Gbps per lane
- 2-lane MIPI CSI-2 transmitter interface, 2.5 Gbps per lane
- I^2C Controller and Target (1 MHz), I^3C Target (12.5 MHz)
- QSPI Controller (50MHz) and Target (30 MHz)
- 22 GPIO for external connectivity
- Crystal oscillator (24 MHz) or external clock (24 MHz, 19.2 MHz)
- 1.8 V I/O supply, 0.8 V core supply
- 3.47 mm x 3.47 mm WLCSP with 9 x 9 ball array

APPLICATIONS

- Augmented reality (AR) systems
- Robotics
- Building automation
- Machine vision systems

GENERAL DESCRIPTION

The ADSD3500 is a Time-of-Flight (ToF) Depth Image Signal Processor (ISP) for Analog Devices' ToF products such as the ADTF3175 and ADSD3030. The Depth ISP processes the raw phase frames from the ToF imager, generating the final radial depth, active brightness (AB), and confidence frames. The ADSD3500 supports full computation of depth, active brightness and confidence data for 640 x 512 resolution and partial depth computation (pre-phase unwrap) for 1024 x 1024 resolution. Data and processing flow is controlled using the integrated ARM® Cortex®-M33. Computation is performed using dedicated hardware and memory, enabling a low-power ToF depth ISP solution. The ADSD3500 also controls the boot-up of the image sensor module, loading of calibration data, and triggering of frames.

The image data receiver (RX) and transmitter (TX) ports use standard Mobile Industry Processor Interface (MIPI) Camera Serial Link 2 (CSI-2) interfaces. Processor programming and operation are controlled through a 4-wire quad serial peripheral interface (QSPI), Inter-Integrated Circuit (I^2C), and Improved Inter-Integrated Circuit (I^3C) serial interfaces.

The ADSD3500 is available in a 3.47 mm x 3.47 mm Wafer-level chip scale packaging (WLCSP) and is specified over an operating temperature range of -25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

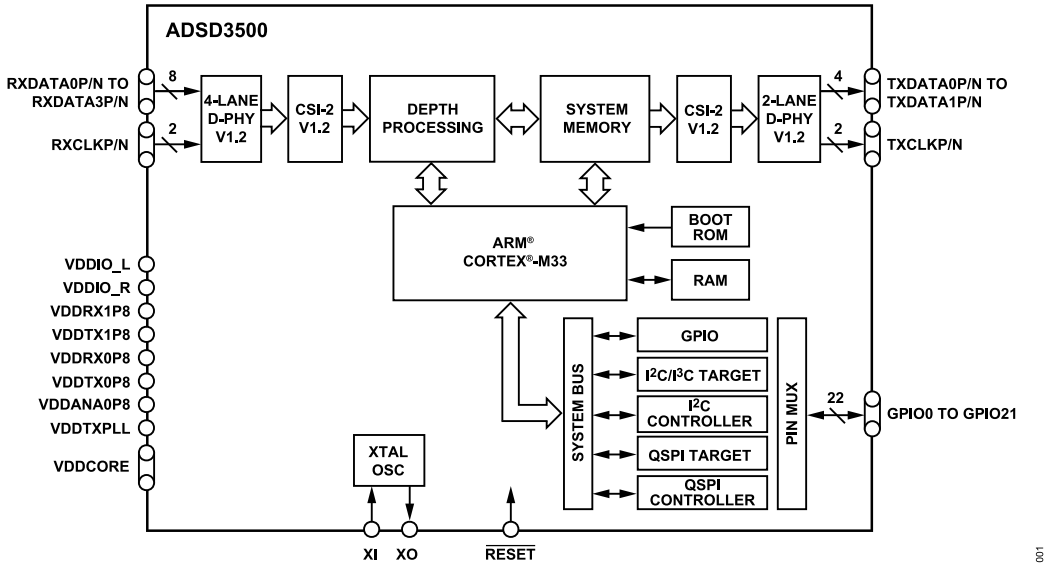

Figure 1. Functional Block Diagram

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