UG0897
User Guide
PolarFire and PolarFire SoC FPGA Power Estimator

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 5.0

The following is a summary of the changes made in revision 5.0 of this document.

- Replaced the following figures.
  - Figure 1, page 2
  - Figure 2, page 5
  - Figure 11, page 13
  - Figure 13, page 14

1.2 Revision 4.0

The following is a summary of the changes made in revision 4.0 of this document.

- Updated information about PolarFire SoC devices and PolarFire range, see Table 3, page 15.
- Updated MSS and MDDR, page 29
- Replaced the following figures.
  - Figure 1, page 2
  - Figure 2, page 5
  - Figure 11, page 13
  - Figure 13, page 14 through Figure 18, page 32.

1.3 Revision 3.0

The following is a summary of the changes made in revision 3.0 of this document.

- Figure 1, page 2
- System Requirements, page 3
- Figure 2, page 5
- Powering FPGA, page 14
- Table 3, page 15
- Figure 18, page 32

1.4 Revision 2.0

The following is a summary of the changes made in revision 2.0 of this document.

- Power Estimator Worksheets, page 5
- MPE Toolbar, page 5
- Configuring Basic Settings, page 15
- MSS and MDDR, page 29
- Figure 1, page 2
- Figure 2, page 5

1.5 Revision 1.0

Revision 1.0 was the first publication of this document.

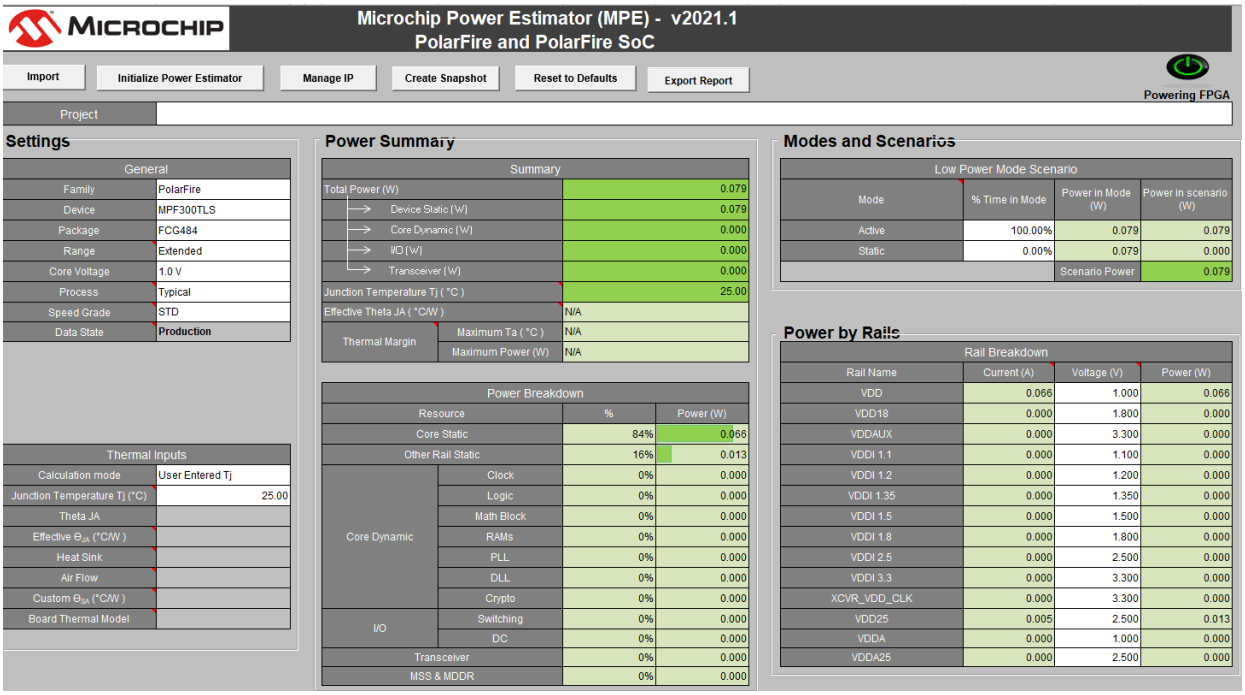
2 Introduction

Early power estimation helps designers define the design architecture within the power budget by applying suitable power saving strategies. It also helps board designers make informed decisions about the power supplies and heat sink to be used for the application. PolarFire® SoC Power Estimator (MPE) is a spreadsheet-based tool that enables designers to estimate the power consumption of PolarFire and PolarFire SoC FPGAs from design concept to design implementation. It provides thermal analysis, as well as information about the contribution of various factors in the total power consumption of PolarFire and PolarFire SoC FPGAs. Operating frequencies, device resources, clock resources, toggle rates, and other parameters are first entered into the Power Estimator tool. These parameters are then combined with pre-determined power models based on simulation and characterized device data to estimate the power consumption. The following are the key features of the Power Estimator:

- Simple GUI elements integrated into a worksheet for quick power estimation
- Power estimation during active and standby modes
- Power estimation using scenarios
- Separate worksheets with power estimation for specific device features
- Calculation of junction temperature based on user-specified thermal inputs
- Ability to create snapshots for future reference and data backup
- Graphical view for better user analysis
- API support to automate the estimator to use it in batch mode

The accuracy of power estimation depends on the settings and data entered in the tool, so it is important to enter realistic data. Also, the Power Estimator results are an early estimation of power consumption rather than measured data. Actual power consumption depends on the actual RTL design, place-and-route, and operating conditions. It is recommended to use Power Estimator for early-stage power estimation and use the SmartPower tool from Libero® SoC for accurate and detailed power estimation for designs after place-and-route. For more information about SmartPower, see *SmartPower for Libero SoC PolarFire Software*.

Figure 1 • **Power Estimator PolarFire and PolarFire SoC**



3 Getting Started with Power Estimator

This section describes the system requirements for using Power Estimator, the process to download Power Estimator, and input requirements to maximize the accuracy of the Power Estimator results.

3.1 System Requirements

The following are the minimum software requirements for using the Power Estimator:

- Microsoft Excel 2003, 2007, 2010, or 2013
- A Windows operating system that supports the above versions of Microsoft Excel

Note: The Power Estimator does not support the Linux operating system. OpenOffice spreadsheets or similar Google Sheets are not supported.

3.2 Downloading Power Estimator and Enabling Macros

Power Estimator for PolarFire SoC can be downloaded using the following link:

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=1244586

The Power Estimator workbook has several built-in macros. By default, the macro security level in Microsoft Excel is set to *high*, which automatically disables macros. To allow macro execution (required for the Power Estimator to function properly), open the Power Estimator workbook and perform the following steps.

In Microsoft Excel 2010 and 2013:

1. Click **File** > **Options**.
2. Click **Trust Center** in the left pane, and then click **Trust Center Settings**.
3. Click **Macro Settings** in the left pane, and select **Enable all macros**.
4. Click **OK.**

In Microsoft Excel 2007:

1. Click the Office button, and click **Excel Options**.
2. Click **Trust Center** in the left pane, and then click **Trust Center Settings**.
3. Click **Macro Settings** in the left pane, and select **Enable all macros**.
4. Click **OK.**

In Microsoft Excel 2003:

1. Click **Tools** > **Macro** > **Security**.
2. Click **Security Level**, and select **Medium**.
3. Click **OK.**

After performing these steps, close the Power Estimator workbook and reopen it. In the security notification that appears at the top, click **Enable this content** or **Enable Macros** (as applicable) to start using the workbook.

3.3 Input Requirements

The power consumption of an FPGA depends largely on the number of logic elements in the FPGA fabric. The following details must be as close as possible to the actual design for reasonably accurate power estimation:

- Device, package, and operating conditions
- Number of flip-flops, LUTs, LSRAM blocks, µSRAM blocks, math blocks, and I/Os
- High-Speed Serial (HSS) interface and Double Data Rate (DDR) interface details
- System clock and clock domain information
- Logic and I/O toggle rates
- Enable and write rates of the RAM

4 Using the Power Estimator Workbook

This section describes how to provide inputs for power estimation and view the power estimation results for the FPGA as a whole, as well as for individual features of the FPGA. It also provides a recommended flow for using the Power Estimator.

4.1 Power Estimator User Interface

The Power Estimator workbook has a Summary worksheet, which provides an at-a-glance view of the power estimation, and feature-specific worksheets that provide more detailed information about specific design resources. All the cells in the workbook are color coded to indicate their edit ability and the type of data they contain. The toolbar available in the Summary worksheet of the Power Estimator has simple GUI buttons to import and reset data, initialize power estimation, capture snapshots of Power Estimator data, and manage design IP.

4.1.1 Color Coding

In order to input the data required for power estimation and interpret the results of the Power Estimator, it is important to understand the color codes used in the Power Estimator workbook. The workbook has several worksheets, and the cells in each worksheet are color coded to simplify data entry and review. The following table shows the color codes used in the workbook.

Table 1 • **Power Estimator Color Codes**

Cell Color	Description
White	Editable field where data can be entered. Editable fields in the Settings section are mandatory.
Gray	Non-editable, description field.
Light Gray	Field not applicable because of selections made in other, related fields.
Green	Read-only, computed, summary value.
Light green	Read-only, computed, individual value.
Red	Input error. Details of the error can be found in the Errors section of the Summary worksheet.

4.1.2 Power Estimator Worksheets

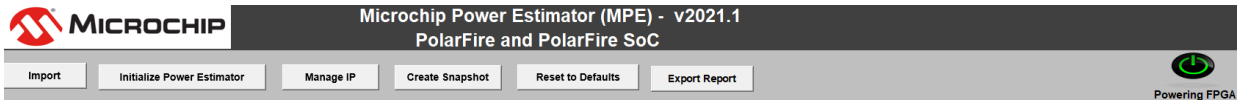
The following worksheets are available in the Power Estimator workbook:

- **Summary:** This is the first worksheet in the workbook. It allows you to input the device settings, modes and scenarios, and power rail details. It displays total power, as well as power breakdown by rails and resources. It also displays any errors that may exist in the data entered in any of the worksheets.
- **Graphs**: This worksheet displays a graphical representation of static current and on-chip power. It allows the user to easily analyze power using graphs
- **Snapshot:** This worksheet displays power consumption data captured at various points in time for future reference. A maximum of 10 snapshots can be saved. For more information, see Create Snapshot, **page 12**.
- **Current Breakdown:** This worksheet displays current support provided by: Functional Static Current (A), Inrush Current (A), Programming Current (A), and Zeroization Current (A).
- **Feature-specific worksheets:** These worksheets contain power and utilization data for specific device features such as clocks, logic, LSRAM, µSRAM, transceivers, I/Os, PLLs and DLLs, and security blocks.
- **User:** This is a blank worksheet where any calculations can be performed and notes entered.
- **Release:** This worksheet contains release notes for all the versions of the Power Estimator, starting with the most current release.

4.1.3 MPE Toolbar

The MPE toolbar at the top of the Summary worksheet provides options for quick import and entry of resource and IP data and allows you to optionally enter a project name.

Figure 2 • **MPE Toolbar**

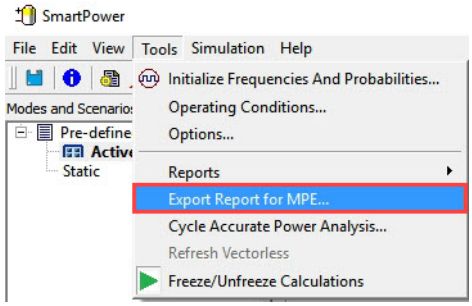


The following sections describe each of the MPE toolbar buttons.

4.1.3.1 Import

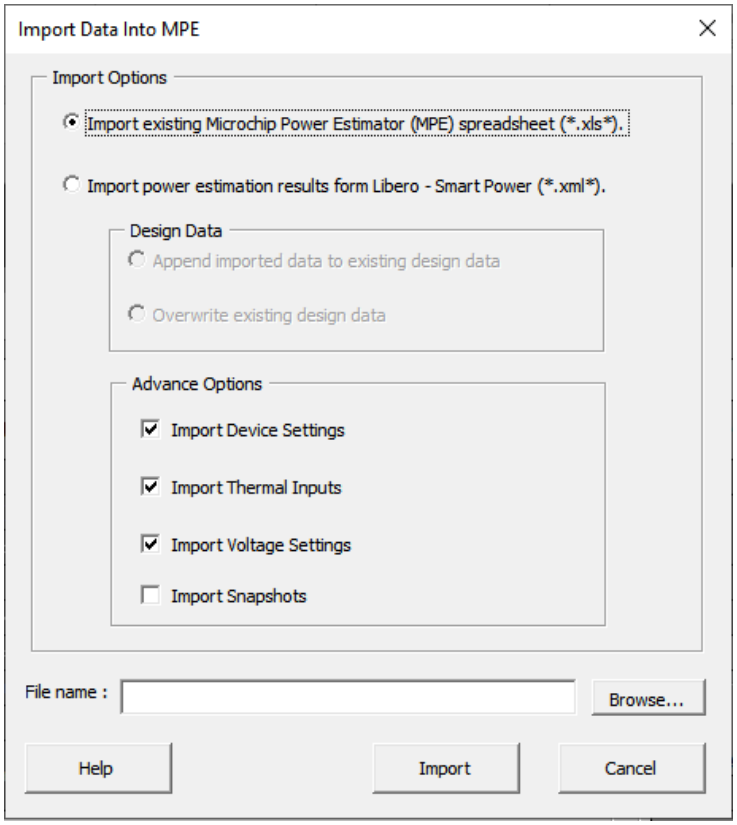
The Import button opens the Importing Data Into MPE wizard, which allows you to select an existing Power Estimator worksheet or a worksheet exported from Libero – SmartPower and import data from it. Click **Export Report for MPE...** to export the Power Estimator worksheet from SmartPower as shown in the following figure.

Figure 3 • **Exporting Power Estimator Worksheet from SmartPower**



You can either choose to import all data or import specific data using the check box available under Advance Options, as shown in the following figure.

Figure 4 • **Import Data Into MPE Wizard**



4.1.3.2 Initialize Power Estimator

The Initialize Power Estimator button opens the Initialize Power Estimator wizard where basic design data such as system clock frequency, number of design resources, I/O technology, and toggle rate can be entered for quick and easy power estimation. For more information, see Initializing Power Estimation, page 18.

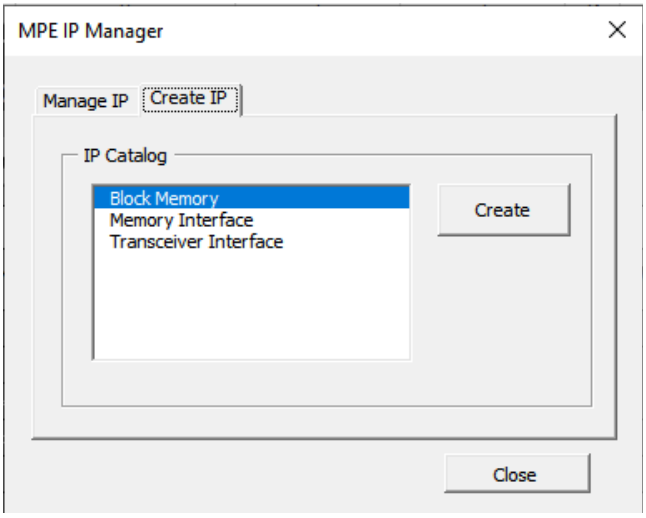
4.1.3.3 Manage IP

The Manage IP button opens the MPE IP Manager wizard, which allows you to add and delete any IP used in the design to the Power Estimator input data. Based on the details entered, values are automatically populated in the various feature-specific tabs, and the Power Estimator results are updated to include the resources consumed by the IP. The IP Manager wizard consists of the following two tabs:

- **Create IP:** creates memory and transceiver interface IP
- **Manage IP:** deletes previously created IP

The following figure shows the MPE IP Manager wizard.

Figure 5 • **MPE IP Manager Wizard**



Using the Create IP tab, you can create three types of IP: memory interface, transceiver interface, and block memory configuration (as shown in the preceding figure). The following figures show the MPE Memory Interface Configuration, MPE Transceiver Interface Configuration, and MPE block memory configuration windows that open when you select **Memory Interface**, **Transceiver Interface**, and **Block Memory** configuration respectively, in the IP catalog and click **Create**.

Figure 6 • **MPE Memory Interface Configuration Wizard**

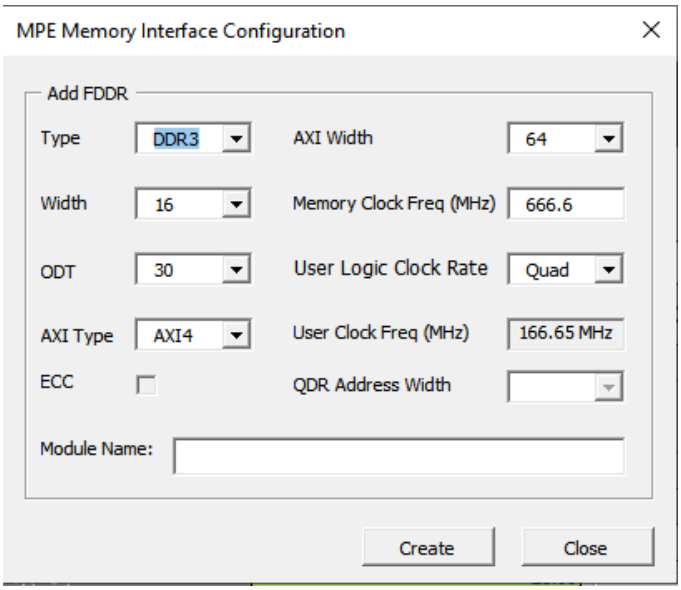


Figure 7 • **MPE Transceiver Interface Configuration Wizard**

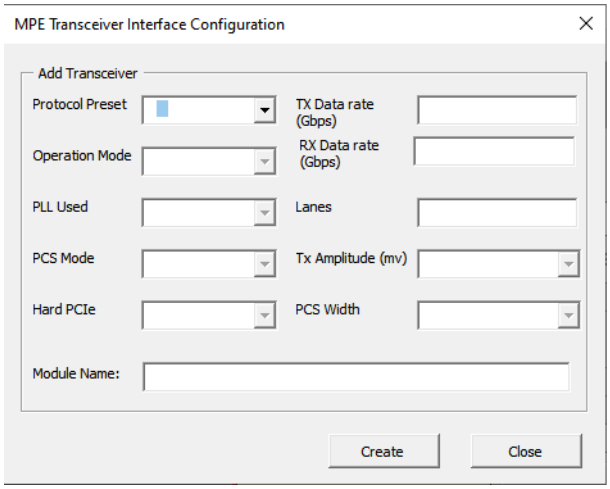


Figure 8 • **MPE Block Memory Configuration—LSRAM**

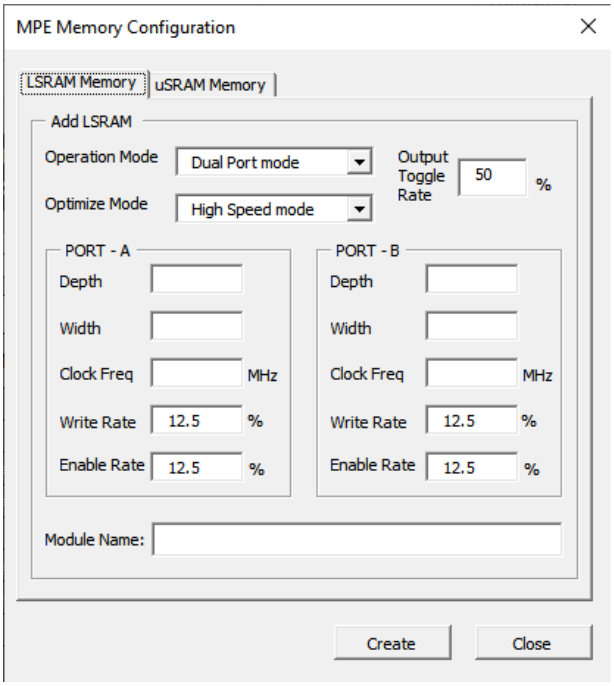
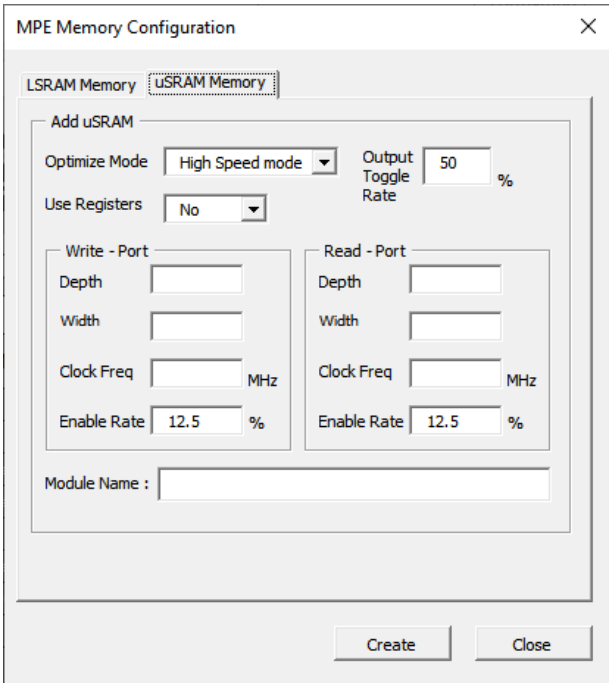


Figure 9 • **MPE Block Memory Configuration—µSRAM**



The following table lists the parameters required for creating an IP using the MPE IP Manager.

Table 2 • **Parameters Required for Creating IP**

IP	Parameter	Description
Memory Interface	Type	DDR memory type. Available options are DDR3, LPDDR3, QDR, and DDR4.
	Width	Memory interface width. Available options are 8, 16, 32, and 64 bits for DDR3 and DDR4; 16 and 32 bits for LPDDR3; 9, 18, and 36 bits for QDR.
	ODT	Input on-die termination (ODT) impedance in ohms.
	AXI Type	AXI interface type. Available options are AXI3 and AXI4.
	ECC	Enable Correction Code (ECC) status. Select or deselect the checkbox to indicate whether ECC is enabled.
	AXI Width	AXI interface width. Automatically selected based on the memory width.
	Memory Clock Freq (MHz)	Memory clock frequency.
	User Logic Clock Rate	User logic clock rate.The Quad option is automatically selected.
	User Clock Freq (MHz)	User clock frequency. Automatically populated based on other memory parameters.
	Module Name	Name of the memory interface module.
	QDR Address Width	Address width of QDR memory. Available options are 18, 19, 20, and 21.
	Module Name	Name of the MPE Memory interface module.

Table 2 • **Parameters Required for Creating IP *(continued)***

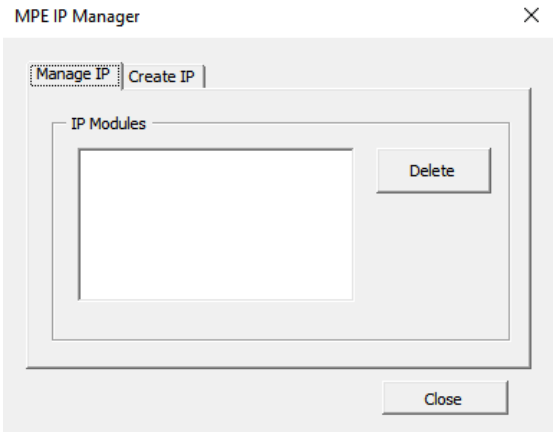
IP	Parameter	Description
Transceiver Interface	Protocol Preset	Protocol to interface the fabric with the transceiver. Based on the selection, other fields such as PLL used, data rate, CTLE drive, PCS mode, PCS width, and hard PCIe are automatically populated (they can be manually changed by selecting from the available options, if necessary). Available options are: – PCIe Gen1 – PCIe Gen2 – 10GBase-KR – SGMII
	Operation Mode	Hardware configuration mode used for the transceiver block. Available options are duplex, transmitter, and receiver.
	PLL Used	PLL that provides the clock for the transceiver block.
	PCS Mode	PCS interface mode that connects the transceiver PMA to the FPGA fabric, and provides data, control, and status signaling to the fabric IP. Available options are: – PMA – 8b/10b – PIPE – 64b/66b – 64b/67b
	Hard PCIe	Hard PCIe usage status. Choose **Yes** if hard PCIe is used for the transceiver block. Choose **No** if soft PCIe is used. Applies to PCIe Gen1 and Gen2 protocols only.
	TX Data rate (Gbps)	Rate of operation of the transceiver. Supported range is 0.5 Gbps to 12.7 Gbps.
	RX Data rate (Gbps)	Rate of operation of the receiver. Supported range is 0.5 Gbps to 12.7 Gbps.
	Lanes	Number of transceiver lanes in the transceiver block.
	Tx Amplitude (mv)	Transmit (TX) driver's differential swing amplitude.
	PCS Width	PCS width. Automatically selected based on the PCS mode (protocol preset). If the protocol supports multiple widths, the desired width can be manually selected.
	Module Name	Name of the transceiver interface module.

Table 2 • **Parameters Required for Creating IP *(continued)***

IP	Parameter	Description
Block memory configuration: LSRAM	Operation Mode	Select the operating mode of LSRAM—Dual Port mode or Two Port mode.
	Optimize Mode	Select the optimize mode of LSRAM—Low power or High speed.
	Output Toggle Rate	Enter the average percentage of time the clock enable is active regardless of the activity on RAM data and address inputs.
	Depth	Enter the depth of LSRAM required for A and B ports of the block memory.
	Width	Enter the width of LSRAM required for A and B ports of the block memory.
	Clock Freq	Enter the clock frequency for A and B ports of the block memory.
	Write Rate	Enter the percentage of time for A and B ports, which are used for write operations. It implies that the time not used for write operations is used for read operations.
	Enable Rate	Enter the average percentage of time for ports A and B are enabled.
	Module Name	Name of the block memory
Block memory configuration: USRAM	Optimize Mode	Select the optimize mode of USRAM—Low power or High speed.
	Output Toggle Rate	Enter the average percentage of time the clock enable is active regardless of the activity on RAM data and address inputs.
	Use Registers	Choose **Yes** if you want to implement µSRAMS as registers. Else choose **No**.
	Depth	Enter the depth of µSRAM required for write and read ports.
	Width	Enter the width of µSRAM required for write and read ports.
	Clock Freq	Enter the clock frequency for write and read ports.
	Enable Rate	Enter the percentage of time, the write and read ports are enabled.
	Module Name	Name of the block memory.

After the IP is created, the IP module is listed on the Manage IP tab, as shown in the following figure.

Figure 10 • **MPE IP Manager IP Modules List**

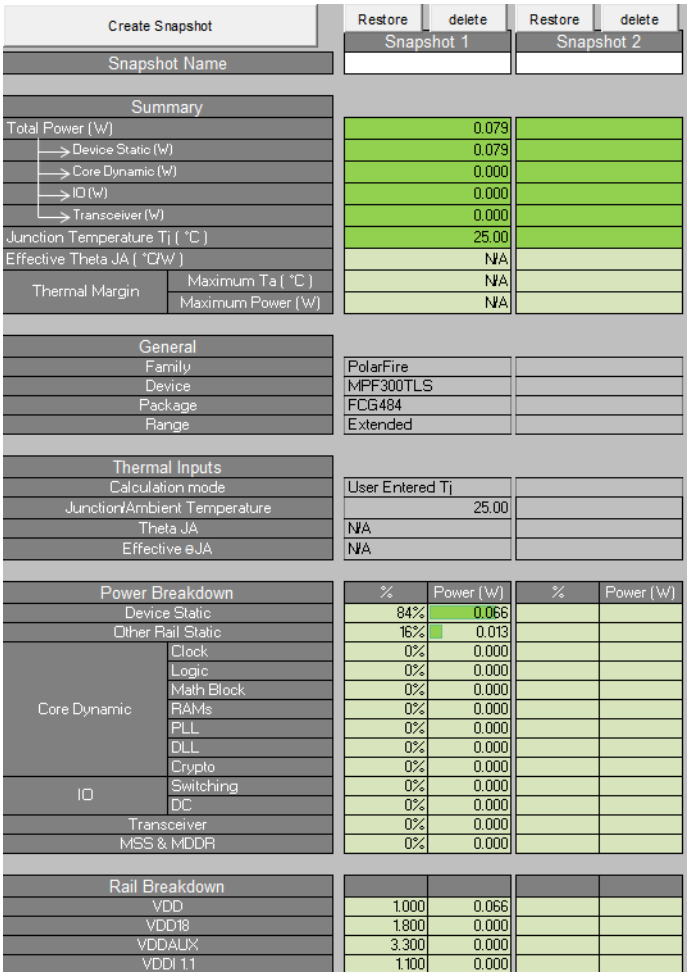


To delete an IP, select the IP, and click **Delete**.

4.1.3.4 Create Snapshot

The Create Snapshot button captures a snapshot of the current power estimation data and saves it for future reference. The saved data appears in the Snapshot worksheet as shown in the following figure. A maximum of 10 snapshots can be saved in the Power Estimator. If this number is exceeded, a message is displayed asking you to delete a worksheet before saving another snapshot.

Figure 11 • **Snapshot Worksheet**



Create Snapshot	Restore	delete	Restore	delete
Snapshot Name	Snapshot 1		Snapshot 2	
Summary				
Total Power (W)	0.079			
→ Device Static (W)	0.079			
→ Core Dynamic (W)	0.000			
→ IO (W)	0.000			
→ Transceiver (W)	0.000			
Junction Temperature Tj (°C)	25.00			
Effective Theta JA (°C/W)	N/A			
Thermal Margin – Maximum Ta (°C)	N/A			
Thermal Margin – Maximum Power (W)	N/A			
General				
Family	PolarFire			
Device	MPF300TLS			
Package	FCG484			
Range	Extended			
Thermal Inputs				
Calculation mode	User Entered Tj			
Junction/Ambient Temperature	25.00			
Theta JA	N/A			
Effective eJA	N/A			
Power Breakdown	%	Power (W)	%	Power (W)
Device Static	84%	0.066		
Other Rail Static	16%	0.013		
Core Dynamic – Clock	0%	0.000		
Core Dynamic – Logic	0%	0.000		
Core Dynamic – Math Block	0%	0.000		
Core Dynamic – RAMs	0%	0.000		
Core Dynamic – PLL	0%	0.000		
Core Dynamic – DLL	0%	0.000		
Core Dynamic – Crypto	0%	0.000		
IO – Switching	0%	0.000		
IO – DC	0%	0.000		
Transceiver	0%	0.000		
MSS & MDDR	0%	0.000		
Rail Breakdown				
VDD	1.000	0.066		
VDD18	1.800	0.000		
VDDAUX	3.300	0.000		
VDDI 1.1	1.100	0.000		

To delete a snapshot that is no longer required, click the Delete button corresponding to the snapshot you want to delete. To restore the current Power Estimator data to that associated with a specific snapshot, click the Restore button corresponding to the snapshot.

4.1.3.5 Reset to Defaults

The Reset to Defaults button opens a window with the following options to reset the data in the Power Estimator workbook to default values:

- **Reset Data:** Resets the data in feature-specific worksheets only.
- **Reset all settings:** Resets the data in the Summary worksheet and the feature-specific worksheets.
- **Reset all settings and snapshots:** Resets all the data in the workbook including the Summary and Snapshot worksheets.

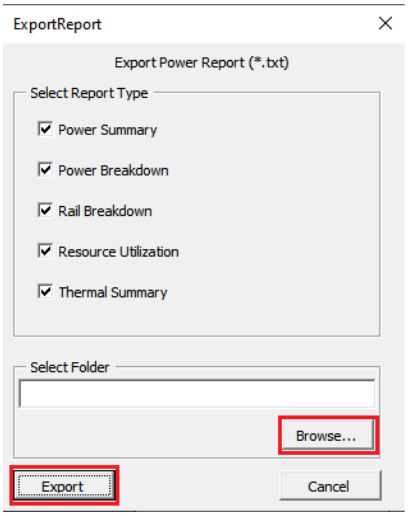
Note: You can also reset existing data (from feature-specific worksheets only) using the Initialize Power Estimator wizard. For more information, see Initializing Power Estimation, page 18.

4.1.3.6 Export Report

The Export Report button opens a window with the following options to export the power estimator data in a text file. Select the report type, click **Browse...** and navigate to the location to save the project, and then click **Export**.

- Power Summary
- Power Breakdown
- Rail Breakdown
- Resource Utilization
- Thermal Summary

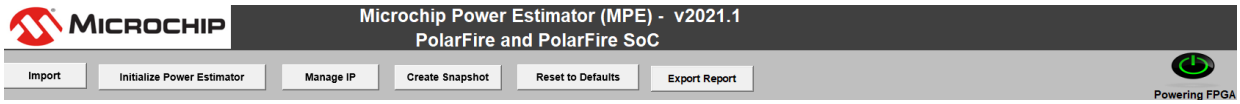
Figure 12 • **Export Report**



4.1.3.7 Powering FPGA

When you click **Powering FPGA** icon as highlighted in the following figure, you will be directed to the *Powering FPGAs* page. This page provides information about building flexible and powerful FPGA-based systems and optimize system power performance using power management solutions.

Figure 13 • **Powering FPGA**



4.2 Recommended Flow

The following is the sequence of steps recommended for estimating power using the Power Estimator:

1. **Settings:** Select the basic settings, that is, the device, package, temperature grade, operating conditions, and thermal inputs. For more information, see Configuring Basic Settings, page 15.
2. **Modes and scenarios (optional):** Enter the percentage of the device operational time in various modes, for example, 50% in active mode. For more information, see Selecting Modes and Scenarios, page 17.
3. **Initialization:** Click the Initialize Power Estimator button in the MPE toolbar, and enter design-specific data to initialize power estimation. For more information, see Initializing Power Estimation, page 18.
4. **Power Estimation Results:** View the values populated in the Summary worksheet and the feature-specific worksheets. For more information, see Viewing and Analyzing Power Estimator Results, page 31.

Note: If the design uses multiple modules, after selecting parameters in the Initiate Power Estimation wizard, enter the details of additional modules in the appropriate feature-specific worksheets for accurate power estimation. For more information, see Entering Feature-Specific Data, page 21.

4.3 Providing Inputs for Power Estimation

This section describes how to provide general and thermal inputs, select modes and scenarios, and initialize power estimation.

4.3.1 Configuring Basic Settings

The first step for estimating power is to enter the design settings in the Summary worksheet of the Power Estimator workbook. The settings are classified into general settings and thermal inputs. The following table describes each of the settings.

Table 3 • **General Settings and Thermal Inputs**

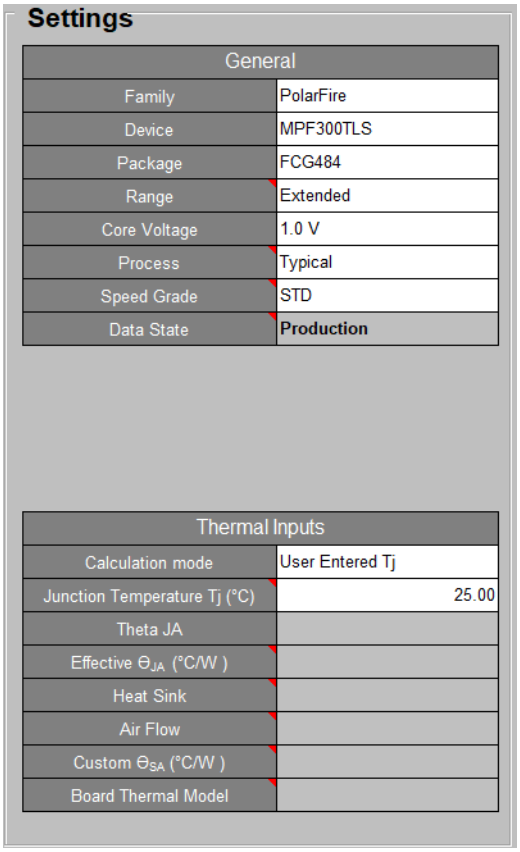
Setting	Description
General Settings	
Family	Device family. PolarFire and PolarFire SoC. This is automatically selected as PolarFire.
Device	For PolarFire SoC family, the device part number options available are: MPFS025T, MPFS025TL, MPFS025TS, MPFS025TLS, MPFS095T, MPFS095TL, MPFS095TS, MPFS095TLS, MPFS160T, MPFS160TL, MPFS160TS, MPFS160TLS, MPFS250T, MPFS250TS, MPFS460T, MPFS460TS, MPFS460TL, and MPFS460TLS. For PolarFire family, the device part number options available are: MPF100T, MPF100TS, MPF100TL, MPF100TLS. MPF200T, MPF200TS, MPF200TL, MPF200TLS, MPF300T, MPF300TS, MPF300TL, MPF300TLS, MPF300XT, MPF500T, MPF500TS, MPF500TL, MPF500TLS, RTPF500T, RTPF500TS, RTPF500TL, and RTPF500TLS.
Package	Device package. Available options vary per device.
Range	Product grade. Select **Industrial** for industrial applications (-40° C to 100° C temperature range) and **Extended** for other applications (0° C to 100° C temperature range). MIL Range is also supported. MPF200TS (FCS325), MPF300TS (FC484), MPF300TS (FCV484), MPF300TS (FCS536), MPF500TS (FC784), and MPF500TS (FC1152) TGrade2 range is supported by PolarFire (-40° C to 125° C temperature range).
Core Voltage	Core voltage used for the design. PolarFire and PolarFire SoC devices support 1.0 V and 1.05 V core voltage.
Process	Manufacturing process variations for the design. Available options are: **Typical:** uses the average power dissipation factor of the resources used in the design. **Maximum:** uses the highest power dissipation factor from the resources used in the design.
Speed Grade	Speed grade used in the design. Available options are: STD and -1. The speed grade has a significant impact on the quiescent current for some devices. Specifying a speed grade helps estimate quiescent current more accurately.
Data State	Readiness level of the data entered as inputs. Available options are: **Advance:** Initial, estimated data based on simulation, other products, and speed grades. Cannot be used for production. **Preliminary:** Data based on simulation and/or initial characterization. Information is likely to be correct, but changes are possible. **Production:** Data considered to be final. In this data state, we recommend using SmartPower for Libero SoC instead of Power Estimator.
Thermal Inputs	

Table 3 • **General Settings and Thermal Inputs *(continued)***

Setting	Description
Calculation mode	The method of calculation of junction temperature. Available options are: **User Entered Tj:** allows the user to specify the junction temperature. **Estimated Tj:** calculates junction temperature based on user-specified thermal inputs that are enabled when this option is selected.
Junction Temperature Tj (°C)	User-specified junction temperature of the device. Applicable only if User Entered Tj is selected as the calculation mode.
Ambient Temperature Ta (°C)	Temperature of the air surrounding the device. Applicable only if Estimated Tj is selected as the calculation mode. Calculates junction temperature based on power dissipation and either thermal resistance or effective θJA, depending on the option selected for Theta JA.
Theta JA	Applicable only if Estimated Tj is selected as the calculation mode. Available options are: **Custom Theta JA:** allows a custom effective Theta Ja to be entered. **Estimated Theta JA** (for future release)**:** enables the Heat Sink, Air Flow, Custom θ SA (°C/W), and Board Thermal Model fields and estimates the effective Theta JA based on the values entered.
Effective θJA (°C/W)	Effective thermal resistance calculated based on user-specified device, package, air flow, heat sink, and board model inputs, and pre-determined characterization and simulation data. Applicable only if Estimated Tj is selected as the calculation mode. In conditions not covered by the available options or where extensive thermal remodeling is done, a custom value can be entered by selecting Custom Theta JA in the Theta JA field.
Heat Sink	Heat sink selection from standard profiles based on device package and air flow. To enter a custom value, select the Custom option.
Air Flow (for future release)	Ambient air flow in meters per second (m/s), which, when increased, reduces the junction temperature, and when reduced, increases the junction temperature. Applicable only if both Estimated TJ and Estimated Theta JA are selected. Available options are Still Air (meaning no air flow), 1.0 m/s, and 2.5 m/s.
Custom θSA (°C/W) (for future release)	User-specified heat sink-to-ambient thermal resistance. Applicable only if both Estimated TJ and Estimated Theta JA are selected. To enter a custom value, select the Custom option in the Heat Sink field.
Board Thermal Model (for future release)	The thermal model of the board. Applicable only if both Estimated TJ and Estimated Theta JA are selected. Available options are: **None:** assumes that no heat is dissipated through the board. **JEDEC (2s2p):** assumes that the board has characteristics of the JEDEC 2s2p test board specified in the JESD51-9 standard.

The following figure shows the General Settings and Thermal Inputs sections of the Power Estimator.

Figure 14 • **General Settings and Thermal Inputs**



4.3.2 Selecting Modes and Scenarios

The Power Estimator allows you to optionally specify the percentage of time the device spends in active and static modes, and uses this information to calculate the power consumption in the specified scenario.

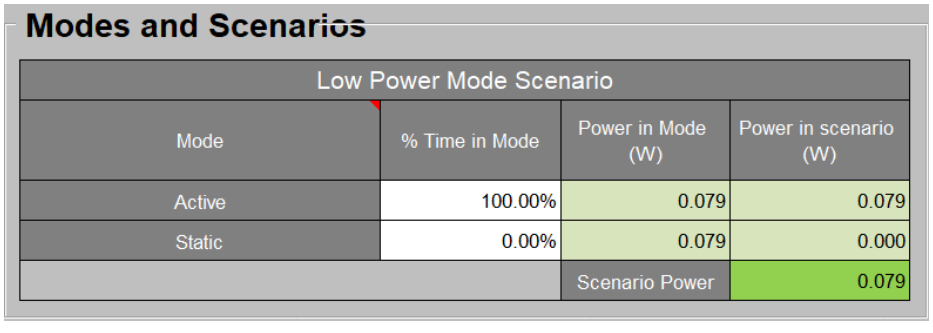
Based on the values entered in the % Time in Mode column, the following values are calculated for each mode:

- **Power in Mode (W):** Shows the power consumed in the mode assuming 100% of the time was spent in the same mode.
- **Power in Scenario (W):** Shows the power consumed in the mode taking into account the percentage of time specified for that mode.

Note: If the percentage across modes exceeds 100, an error is displayed.

The following figure shows the Modes and Scenarios section of the Power Estimator.

Figure 15 • **Modes and Scenarios**



4.3.3 Entering Rail Voltages

Depending on the device, package, and design resources used, the Power Estimator automatically populates the voltages for applicable power supplies in the Power by Rail section of the Summary worksheet. You can manually change the voltage values (within acceptable ranges) to calculate power supply at different voltages. Based on the voltage entered for each supply, the current requirement (Current (A)) and the estimated power consumption (Power (W)) of the supply are automatically calculated, as shown in the following figure.

Figure 16 • **Power by Rail Section**

Power by Rails

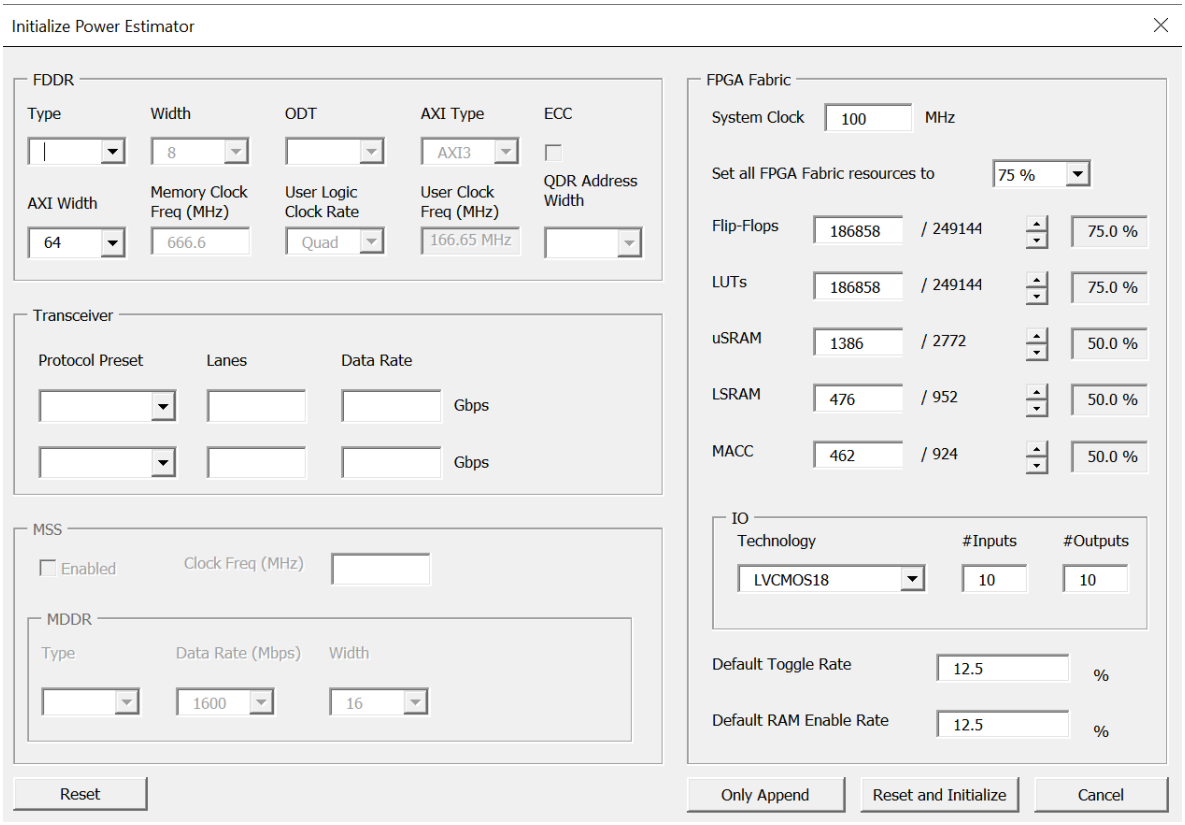
Rail Breakdown			
Rail Name	Current (A)	Voltage (V)	Power (W)
VDD	0.066	1.000	0.066
VDD18	0.000	1.800	0.000
VDDAUX	0.000	3.300	0.000
VDDI 1.1	0.000	1.100	0.000
VDDI 1.2	0.000	1.200	0.000
VDDI 1.35	0.000	1.350	0.000
VDDI 1.5	0.000	1.500	0.000
VDDI 1.8	0.000	1.800	0.000
VDDI 2.5	0.000	2.500	0.000
VDDI 3.3	0.000	3.300	0.000
XCVR_VDD_CLK	0.000	3.300	0.000
VDD25	0.005	2.500	0.013
VDDA	0.000	1.000	0.000
VDDA25	0.000	2.500	0.000

4.3.4 Initializing Power Estimation

After entering the settings, click the Initialize Power Estimator button on the MPE toolbar, and enter applicable design-specific values in the Initialize Power Estimator wizard. Based on the inputs provided in the wizard, design data is automatically populated in the feature-specific worksheets (such as Clock, Logic, and LSRAM) of the Power Estimator workbook. Entries thus populated can be edited from the feature-specific worksheets to provide more accurate inputs for power estimation, including module names and additional rows of data that were not entered when initiating power estimation. For more information, see Entering Feature-Specific Data, page 21.

The following figure shows the Initialize Power Estimator wizard.

Figure 17 • **Initialize Power Estimator Wizard**



Note: The MSS section is only available, if the product family is selected as PolarFire SoC from the General Settings.

The following table lists the parameters available in the Initialize Power Estimator wizard.

Table 4 • **Initialize Power Estimator Wizard Fields**

Parameter	Sub-Parameter	Action
FDDR	Type	Choose the DDR memory type. Available options are DDR3 and DDR4.
	Width	Choose the memory interface width.
	ODT	Specify the input on-die termination impedance in ohms.
	AXI Type	Choose the AXI interface type. Available options are AXI3 and AXI4.
	ECC	Check to enable correction code. Available only for 32- and 64-bit memory interface width.
	AXI Width	Choose the AXI interface width.
	Memory Clock Freq (MHz)	Enter the memory clock frequency.
	User Logic Clock Rate	The user logic clock rate type is automatically selected as **Quad**.
	User Clock Freq (MHz)	The user clock frequency is automatically populated based on other memory parameters.
	QDR Address Width	Address width of QDR memory. Available options are 18, 19, 20, and 21.
Transceiver	Protocol Preset	Choose a protocol to interface the fabric with the transceiver. Based on the selection, other fields such as PLL used, data rate, CTLE drive, PCS mode, PCS width, and hard PCIe are automatically populated (they can be manually changed by selecting from the available options, if necessary). Available options are: – PCIe Gen1 – PCIe Gen2 – 10GBase-KR – SGMII
	Lanes	Enter the number of transceiver lanes in the block.
	Data Rate	Enter the rate of operation of the transceiver. Supported range is 0.5 Gbps to 12.7 Gbps.

Table 4 • **Initialize Power Estimator Wizard Fields *(continued)***

Parameter	Sub-Parameter	Action
FPGA Fabric	System Clock	Enter the fabric clock frequency. Default value: 100 MHz Valid range: 0 to 400 MHz
	Set all FPGA Fabric resources to	Use this list to choose a single design utilization percentage for all fabric resources. Available values are 25%, 50%, 75%, and 100%. If necessary, the utilization of individual resources can be edited using the up and down arrows provided for each resource.
	Flip-Flops	Enter the number of flip-flops used in the design, or choose the percentage of overall design resources used by flip-flips.
	LUTs	Enter the number of LUTs used in the design, or choose the percentage of overall design resources used by LUTs.
	µSRAM	Enter the number of µSRAM blocks used in the design, or choose the percentage of overall design resources used by µSRAM blocks.
	LSRAM	Enter the number of LSRAM blocks used in the design, or choose the percentage of overall design resources used by LSRAM blocks.
	MACC	Enter the number of math blocks used in the design, or choose the percentage of overall design resources used by math blocks.
IO	Technology	Select the I/O standard used in the design from the list of available standards.
	#Inputs	Enter the number of inputs in the design.
	#Outputs	Enter the number of outputs in the design.
Default Toggle Rate		Enter a default toggle rate for the design resources.
Default RAM Enable Rate		Enter a default RAM enable rate for µSRAM and LSRAM.

After entering the data, to append the data to existing data in the various worksheets of the Power Estimator workbook, click **Only Append**. To clear the existing resource data and replace it with fresh data entered in the wizard, click **Reset and Initialize**.

4.3.5 Entering Feature-Specific Data

The Initiate Power Estimator wizard is designed to collect basic design data required for power estimation. To add module names and additional rows of data that are not supported by the Initialize Power Estimator wizard, use the worksheet specific to each device feature. The following sections provide information about each feature-specific worksheet in the Power Estimator workbook.

4.3.5.1 Clocks

Details of clocks used in the design are entered in the Clock worksheet. PolarFire and PolarFire SoC devices support various clock networks such as global clock networks, bank clock networks, input/output regional clock networks (ICLK), and local regional clock networks (LCLK). Each row in the Clock worksheet is associated with a separate clock domain. Based on the values entered, the power consumption of each clock domain is populated in the Power (W) column.

The following table lists the parameters required for each clock domain in the Clock worksheet.

Table 5 • **Clock Worksheet Parameters**

Parameter	Action
Name	Enter the name of the clock domain.
Clock Frequency (MHz)	Enter the clock domain frequency. Valid ranges are: For global clocks, ICLK, and LCLK: 0 to 550 MHz. For bank clocks: 0 to 1250 MHz.
Clock Type	Choose the clock type: Global, Regional (ICLK), Regional (LCLK), or Bank Clock.
Fanout	Enter the number of registers and other synchronous elements (LSRAM, µSRAM, math blocks, and I/Os) clocked in the design. Not applicable to bank clocks.
Clock Buffer Enable Rate	Enter the average percentage of time the entire clock tree is active for the clock domain. A 100% clock buffer enable rate means that the clock tree is toggled at the clock frequency.

For more information about the clocking resources in PolarFire SoC FPGAs, see *UG0913: PolarFire SoC FPGA Clocking Resources User Guide*.

4.3.5.2 Logic

Each row in the Logic worksheet represents a separate logic module. Based on the values entered, the power consumption of the logic in each module is populated in the Power (W) column.

The following table lists the parameters required for each module in the Logic worksheet.

Table 6 • **Logic Worksheet Parameters**

Parameter	Action
Name	Enter the name of the logic module.
Clock Frequency (MHz)	Enter the clock domain frequency. Valid ranges are: For global clocks, ICLK, and LCLK: 0 to 550 MHz. For bank clocks, 0 to 1250 MHz.
Number of DFF	Enter the number of D-flip-flops (sequential modules) used in the module.
Number of 4LUT	Enter the number of 4-input LUTs used in the module.
Design Complexity	Enter the average fanout of nets driven by the registers and LUTs in the module.
Toggle Rate	Enter the toggle rate for the registers and LUTs in the module.

For more information about PolarFire SoC FPGA fabric logic, see *UG0912: PolarFire SoC FPGA Fabric User Guide*.

4.3.5.3 LSRAM

Each row in the LSRAM worksheet represents a separate logic module. Based on the values entered, the power consumption of LSRAM blocks in each module is populated in the Power (W) column.

The following table lists the parameters required for each module in the LSRAM worksheet.

Table 7 • **LSRAM Worksheet Parameters**

Parameter	Action
Name	Enter the name of the module containing the LSRAM block(s).
Number of LSRAM Blocks	Enter the number of LSRAM blocks used in the module.
Width	Enter the data width of each RAM port. Available options are 1, 2, 5, 10, 20, 32, and 40. For mixed-width RAMs, use a larger port width for a conservative estimate.
Clock Frequency (MHz)	Enter the clock frequency for ports A and B of the module in the column corresponding to each port. The maximum frequency supported is 450 MHz.
Write Rate	Enter the percentage of time ports; A and B are used for write operations in the column corresponding to each port. It is implied that the time that is not used for write operations is used for read operations.
Read Rate (1 - Write Rate)	Enter the percentage of time; ports A and B are used for read operations in the column corresponding to each port.
Write Mode	Different write modes—simple write, read before write, and write feed through.
Enable Rate	Enter the average percentage of time ports A and B are enabled in the column corresponding to each port.
Pipeline Enable	Register pipeline can be enabled or disabled.
ECC Enable	ECC can be enabled or disabled.
Output Toggle Rate	Enter the average percentage of time the clock enable is active regardless of the activity on RAM data and address inputs.

For more information about LSRAM support, see *UG0912: PolarFire SoC FPGA Fabric User Guide*.

4.3.5.4 µSRAM

Each row in the µSRAM worksheet represents a separate logic module. Based on the values entered, the power consumption of µSRAM blocks in each module is populated in the Power (W) column.

The following table lists the parameters required for each module in the µSRAM worksheet.

Table 8 • **µSRAM Worksheet Parameters**

Parameter	Action
Name	Enter the name of the module containing the µSRAM block(s).
Number of µSRAM Blocks	Enter the number of µSRAM blocks used in the module.
Width	Enter the data width of each RAM port. The number can be any positive integer up to 12. For mixed-width RAMs, use a larger port width for a conservative estimate.
Use Registers	Select **Yes** or **No**, respectively, to enable and disable the use of registers.
Write Clock Frequency (MHz)	Enter the clock frequency of the write port of the µSRAM blocks in the module.
Read Port Clock Domain Frequency (MHz)	Enter the clock frequency of the read port of the µSRAM blocks in the module.
Enable Rate	Enter the percentage of time the write and read ports are enabled in the column corresponding to each port.
Output Toggle Rate	Enter the average percentage of time the clock enable is active regardless of the activity on RAM data and address inputs.

For more information about µSRAM support, see *UG0912: PolarFire SoC FPGA Fabric User Guide*.

4.3.5.5 Math Blocks

Details of math blocks used in the design are entered in the Math Block worksheet. Each row in this worksheet represents a separate logic module. Based on the values entered, the power consumption of math blocks in each module is populated in the Power (W) column.

The following table lists the parameters required for each module in the Math Block worksheet.

Table 9 • **Math Block Worksheet Parameters**

Parameter	Action
Name	Enter the name of the module containing the math block(s).
Clock Frequency (MHz)	Enter the clock domain frequency. Maximum frequency supported is 450 MHz.
Number of Math Blocks	Enter the number of math blocks used in the module.
Output Toggle Rate	Enter the average percentage of time the clock enable is active regardless of the activity on RAM data and address inputs.
Mode	Provide the mode of operation for the math block. The following modes are supported: – Normal-Multiplier – Normal-Multiplier-Accumulator – SIMD – DOTP
Pre Adder	Can be enabled or disabled.
Pipelined Inputs	Input data pipelining can be enabled or disabled.
Pipelined Outputs	Output data pipelining can be enabled or disabled.

For more information about math blocks, see *UG0912: PolarFire SoC FPGA Fabric User Guide*.

4.3.5.6 I/Os

Details of I/O blocks used in the design are entered in the IO worksheet. Each row in the IO worksheet represents a separate I/O bus or module. Based on the values entered for each module, power consumption of the VDD, VDD18, VDDAUX, and VDDI supplies, along with the total power consumption across supplies, is automatically populated.

The following table lists the parameters required for each module in the IO worksheet.

Table 10 • **IO Worksheet Parameters**

Parameter	Action
Name	Enter the name of the I/O bus or module.
Bank Type	Choose the bank type: HSIO, GPIO, or XCVR_REFCLK.
I/O standard	Choose the I/O standard from the list of available standards.
Mixed Mode VDDI	Mixed mode VDDI is only applicable for inputs.
Input Pins[1]	Enter the number of input pins or input differential pairs used in the module.
Output Pins[1]	Enter the number of output pins or output differential pairs used in the module.
Bidir Pins[1]	Enter the number of bidirectional pins or bidirectional differential pairs used in the module.
VCM	Can be enabled or disabled for xxxxxxxx
Schmitt Trigger	Can be enabled or disabled for inputs pin or bidirectional pin.
ODT	Select the input on-die termination (ODT) impedance in ohms. Available options are 60, 120, and NO_ODT.
Output Drive (mA) / Drive Impedance (Ohm)	This setting is used for outputs or bidirectional IOs.
Slew Calibration	This setting is used for outputs and bidirectional IOs.
Output Load (pF)	Enter the capacitance of the board and the external components.
IOG Mode	If I/O gearing is not used, choose **Unused**. If it is used, choose from the list of available modes.
Clock (MHz)	Enter the clock domain frequency. Maximum frequency supported is 800 MHz.
Data Rate	Select the data rate for the I/Os in the module. For I/Os used as clocks, choose **Clock**. For others, choose **SDR** (single data rate) or **DDR** (double data rate).
Toggle Rate	Enter the toggle rate of the I/Os in the module.
Output Enable	Enter the percentage of time outputs are enabled in the module. For bidirectional I/Os, the input path is assumed to be active when outputs are disabled.

1. Differential pairs must be considered as a single pin.

For more information about I/O support, see *UG0916: PolarFire SoC FPGA IO User Guide*.

4.3.5.7 Transceivers

Details of transceiver blocks used in the design are entered in the Transceiver worksheet. Because the PLLs in PolarFire and PolarFire SoC FPGAs can drive up to four lanes, each row in the worksheet may represent either a single-lane or a multi-lane transceiver block. The number of lanes used must be specified for each block.

The following table lists the parameters required for each transceiver block in the Transceiver worksheet.

Table 11 • **Transceiver Worksheet Parameters**

Parameter	Action
Name	Enter the name of the transceiver block.
Protocol Preset	Choose a protocol to interface the fabric with the transceiver. Based on the selection, other fields such as PLL used, data rate, CTLE drive, PCS mode, PCS width, and hard PCIe are automatically populated (they can be manually changed by selecting from the available options, if necessary). Available options are: – PCIe Gen1 – PCIe Gen2 – 10GBase-KR – SGMII
Number of Lanes	Enter the number of transceiver lanes in the block.
Operational Mode	Choose the hardware configuration mode used for the transceiver block: Duplex, Independent Tx/Rx, Tx Only, or Rx.
Data Rate (Gbps)	Specify the rate of operation of the transceiver. Supported range is 0.5 Gbps to 12.7 Gbps. **Note:** Data Rate option is different for Tx and Rx.
PLL Used	Choose the PLL that provides the clock for the transceiver block. Q#_TXPLL0 and Q#_TXPLL1 can be used by a pair of adjacent transmit lanes with the adjacent transceiver quad lane blocks either above, below, or both above and below the PLL. Q#_TXPLL_SSC is used within the quad only.
DFE Enable	Choose **Yes** if Differential Feedback Equalization (DFE), used in conjunction with CTLE to equalize channel response, is enabled for the transceiver block. Choose **No** if DFE is not enabled.
Eye Monitor Enable	Choose **Yes** if eye monitor (an on-device circuitry to visualize post-equalization signal quality in the receive (RX) path) is enabled for the transceiver block. Choose **No** if eye monitor is not enabled.
CTLE Drive	Specify the number of CTLE drives. CTLE equalizes low-pass channel response and compensates high frequency losses in the channel, improving the quality of received signals. Available mapping factors are 0, 1, 2, and 3.
TX Amplitude (mV)	Enter the transmit (TX) driver's differential swing amplitude.
Mode	Choose the PCS interface mode that connects the transceiver PMA to the FPGA fabric and provides data, control, and status signaling to the fabric IP. Available options are: – PMA – 8b/10b – PIPE – 64b/66b – 64b/67b
Width	Choose the FPGA fabric interface width. Available options vary based on the protocol selected.
Hard PCIe	Choose **Yes** if hard PCIe is used for the transceiver block. Choose **No** if soft PCIe is used. Applies to PCIe Gen1 and Gen2 protocols only.

For more information about transceiver support in PolarFire and PolarFire SoC FPGAs, see *UG0915: PolarFire SoC FPGA Transceiver User Guide*.

4.3.5.8 PLLs and DLLs

PolarFire and PolarFire SoC devices have two PLLs and two DLLs in each corner of the FPGA fabric to provide flexible clocking schemes for the logic implemented in the fabric. Details of the PLLs used in the fabric are entered in the PLL Power section and those of the DLLs are entered in the DLL Power section of the PLL and DLL worksheet. The following table lists the parameters required for each PLL or DLL in this worksheet.

Table 12 • **PLL & DLL Worksheet Parameters**

Parameter	Action
Name	Enter the name of the PLL or DLL module.
Reference Clock Frequency (MHz)	Enter the reference clock frequency for the PLL or DLL module.
Output0 Frequency (MHz)	Enter the frequency of output 0.
Output1 Frequency (MHz)[1]	Enter the frequency of output 1.
Output2 Frequency (MHz)[1]	Enter the frequency of output 2.
Output3 Frequency (MHz)[1]	Enter the frequency of output 3.
Mode[1]	Choose the PLL mode as low power or low jitter. **Note:** Supported mode options are: Min VCO for Low Power and Max VCO for Low Jitter.

1. This parameter is applicable to PLLs only, and, therefore, does not appear in the DLL Power section.

For more information about PLLs and DLLs in PolarFire SoC FPGAs, see *UG0913: PolarFire SoC FPGA Clocking Resources User Guide*.

4.3.5.9 MSS and MDDR

PolarFire SoC FPGAs are ideal for running full-fledged Operating Systems (Linux) using the 5x core MSS, which includes four 64-bit RISC-V application cores and a 64-bit RISC-V monitor core.

The MSS feature applies only to the PolarFire SoC and not PolarFire.The following table lists the parameters required for RISC-V, MDDR, AXI MSS/Fabric Interfaces, and IO Interfaces in this worksheet.

Table 13 • **MSS & DDR Worksheet Parameters**

Parameter	Action
MSS Configuration	Disabled Enabled
RISC-V (Quad U54)	
Clock Frequency (MHz)	Enter the clock domain frequency. Valid ranges are: Up to 625 MHz.
Number of Cores Used	Enter number of cores (up to 4).
L2 Cache Size Used Configuration	512 KB 1 MB 1.5 MB 2 MB
MDDR	
MDDR Type	DDR4 LPDDR4 DDR3
Data Rate (Mbps)	1600 for DDR4 1333 for DDR3
Width	Choose the MDDR width (x 16 and x 32) + ECC
Read Mode Utilization	Can enter up to 100%.
Write Mode Utilization	Can enter up to 100%.
Activity during read/write	Can enter up to 100%.
AXI MSS / Fabric Interfaces	
FIC0 Configuration	Master/Slave Disabled
FIC1 Configuration	Master/Slave Disabled
FIC2 Configuration	Master/Slave Disabled
FIC3 Configuration	Master/Slave Disabled
FIC0 Clock Frequency (MHz)	Enter the clock domain frequency. Valid ranges are: For global clocks, ICLK, and LCLK: 0 to 550 MHz. For bank clocks, 0 to 1250 MHz.
FIC1 Clock Frequency (MHz)	Enter the clock domain frequency. Valid ranges are: For global clocks, ICLK, and LCLK: 0 to 550 MHz. For bank clocks, 0 to 1250 MHz.
FIC2 Clock Frequency (MHz)	Enter the clock domain frequency. Valid ranges are: For global clocks, ICLK, and LCLK: 0 to 550 MHz. For bank clocks, 0 to 1250 MHz.

Table 13 • **MSS & DDR Worksheet Parameters *(continued)***

Parameter	Action
FIC3 Clock Frequency (MHz)	Enter the clock domain frequency. Valid ranges are: For global clocks, ICLK, and LCLK: 0 to 550 MHz. For bank clocks, 0 to 1250 MHz.
IO Interfaces	
GEM_0 Configuration	GMII / MII SGMII
GEM_1 Configuration	GMII / MII SGMII
User Crypto	
UserCrypto Block Configuration	Enabled Disabled
UserCrypto Block Clock Frequency (MHz)	Enter the clock domain frequency. Valid ranges are: Up to 625 MHz.

For more information about MSS and DDR in PolarFire SoC FPGAs, see *UG0880: PolarFire SoC MSS User Guide*.

4.3.5.10 Security

PolarFire and PolarFire SoC FPGAs support data security using an Athena F5200 TeraFire Crypto Processor. Details of this cryptoprocessor are entered in the **User Crypto** worksheet.

The following table lists the parameters required in the **User Crypto** worksheet.

Table 14 • **User Crypto Worksheet Parameters**

Parameter	Action
Clock Frequency (MHz)	Enter the clock domain frequency. Maximum value is 250 MHz.
Toggle Rate	Enter the toggle rate of the user crypto block.

For more information about the security features of PolarFire SoC FPGAs, see *UG0918: PolarFire SoC FPGA Security User Guide*.

4.4 Viewing and Analyzing Power Estimator Results

This section explains how to view and analyze the results of Power Estimator to optimize power for PolarFire and PolarFire SoC FPGAs.

4.4.1 Viewing Power Estimation Data

Based on the data provided in the Initialize Power Estimator wizard and the feature-specific worksheets, power consumption is estimated and the results displayed in all the tabs. The following table lists the various power estimation views generated in the Power Estimator.

Table 15 • **Power Estimator Views**

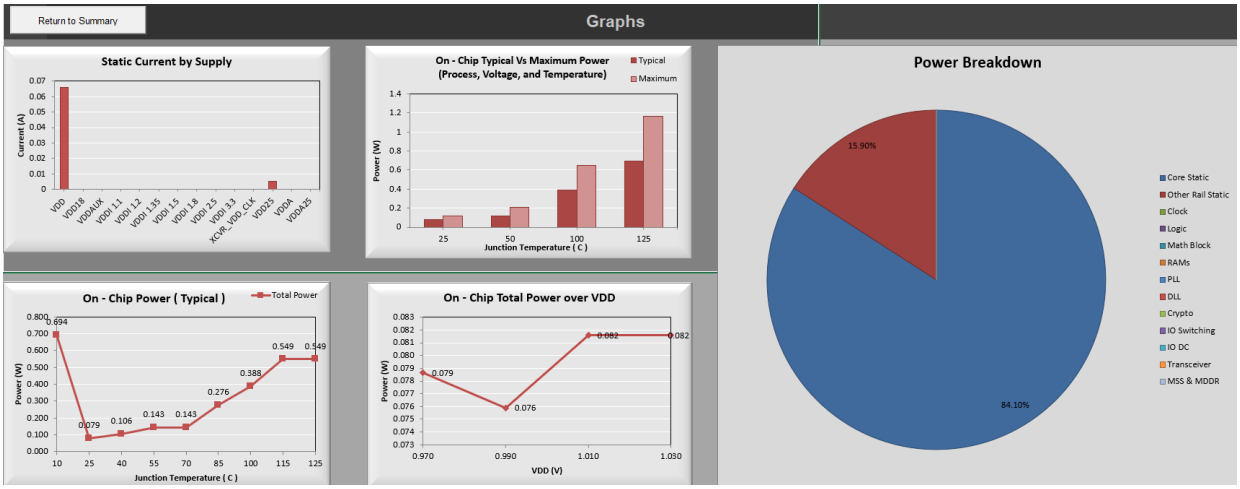
View	Description	Worksheet and Section
Power by type	Provides device static and core dynamic power details.	Summary worksheet – Power Summary section
Power by resource	Provides a consolidated view of power used by each device feature, such as clock, logic, and I/Os.	Summary worksheet – Power Breakdown section
Power based on modes and scenarios	Provides power consumption based on the percentage of time spent in various operational modes.	Summary worksheet – Modes and Scenarios section
Power by rail	Provides power breakdown for each voltage rail.	Summary worksheet – Power by Rail section
Resource utilization	Provides the utilization rate for each device feature.	Summary worksheet – Resource Utilization section Feature-specific worksheet – Utilization section
Power by hard block	Provides the power breakdown for transceiver hard blocks.	Transceiver worksheet – Power (W) by Hard Block section

4.4.1.1 Graphs

Graphs feature allows user to easily analyze power using graphs. A Graph section is added next to the Summary section in the MPE. It displays five different graph types:

- **Power Breakdown**: displays a pie chart of the power per component type.
- **Static Current by Supply**: displays a bar graph of the current for each power rail.
- **On-chip Typical vs Maximum Power**: displays a bar graph with typical and maximum power for supported Junction temperatures.
- **On-chip Power (Typical)**: displays a line graph of the total power across temperature for the selected process corner.
- **On-chip Total Power over VDD**: displays a line graph showing of the total power across the range of supported VDD values.

Figure 18 • **Graphs Worksheet**



4.4.2 Analyzing Power Estimation Data

Proper analysis of the Power Estimator results can help balance your power and performance goals. Actions that can be taken based on the results vary based on the application's requirements and cost considerations. The following are the examples of design changes that can be made based on the Power Estimator results:

- Thermal inputs significantly affect the total power. If the total power exceeds the power margin, reduce the ambient temperature by installing a suitable heat sink, ensuring proper air flow, and using other cooling devices. You can check the total power at different ambient temperatures and heat sink/air flow settings using the Power Estimator.
- Choose a device suitable for the design based on the power margin and resource utilization. For example:
  - If the power exceeds marginal value and there are unused logic elements (that is, the resource utilization is significantly less than 100%), change the device to one that uses less logic elements.
  - If the resource utilization exceeds 100%, it means the device selected does not support the number of resources used in the design. In this case, choose a device with more logic elements to meet the design requirements.
- Choose the appropriate speed grade for the design based on your power and performance goals. A higher speed grade improves performance but leads to higher static power. To prevent unnecessary power costs, avoid using a speed grade higher than necessary for optimal performance of the application.

5 Appendix 1: Using Power Estimator in Batch Mode

The following functions allows user to make changes to the estimator environment, create snapshot, set device info, get resource utilization, record text report, and so on.

1. To set a device, use function setDevice (parameter) and pass the device name.
   ```
   Function setDevice (device As String)
   ```
2. To set a package, use function setPackage (parameter) and pass the package name.
   ```
   Function setPackage (package As String)
   ```
3. To set a Temperature grade, use function setTemperatureRange (parameter) and pass the temperature grade name.
   ```
   Function setTemperatureRange (tRange As String)
   ```
4. To set a core voltage, use function setCoreVoltage (parameter) and pass the core voltage.
   ```
   Function setCoreVoltage (cVoltage As String)
   ```
5. To set a process, use function setProcess (parameter) and pass the process name.
   ```
   Function setProcess (process As String)
   ```
6. To set a speed grade, use function setSpeedGrade (parameter) and pass the speed grade name.
   ```
   Function setSpeedGrade (sGrade As String)
   ```
7. To set junction temperature, use function setJunctionTemperature (parameter) and pass the temperature value.
   ```
   Function setJunctionTemperature(jTemp As String)
   ```
8. To get resource utilization value, use getResourceUtilization (parameter) and pass the resource name as string.
   ```
   Function getResourceUtilization(Resource As String)
   ```
9. To get mode power value, use getModePower (parameter) and pass the mode name as string.
   ```
   Function getModePower (mode As String)
   ```
10. To set device info with device, package, temperature grade, and speed grade, use setDeviceInfo (parameter) and pass the values.
    ```
    Function setDeviceInfo (device As String, package As String, tGrade As String, sGrade As String)
    ```
11. To export the power report in a text file, use exportPowerReport (parameter) and pass the required reports as parameters.
    ```
    Function exportPowerReport (Power_Summary:=True, Power_Breakdown:=True, Rail_Breakdown:=True, Resource_Utilization:=True, Thermal_Summary:=True, File_Location:=".")
    ```
12. To instantiate the DDR in the IP, use setDDR (parameters) and pass the values to instantiate.
    ```
    Function setDDR (ddr_type As String, ddr_width As Integer, ddr_clkfreq As Double, ddr_odt As String, ddr_axitype As String, ddr_axiwidth As Integer, ddr_logicclkrate As String, ddr_ecc As String, ddr_module_name As String)
    ```
13. To instantiate the Transceiver in the IP, use setTransceiver (parameters) and pass the values to instantiate.
    ```
    Function setTransceiver (module_name As String, protocol_preset As String, xcvr_lanes_tb As Integer, operation_mode As String, xcvr_data_rate_tb As Double, pll_used As String, tx_amplitude As String, pcs_mode As String, pcs_width As Integer, hard_pcie As String
    ```
14. To instantiate the LSRAM in the IP, use setLSRAM (parameters) and pass the values to instantiate.
    ```
    Function setLSRAM (usram_module_name As String, usram_writeP_depth As Integer, usram_writeP_width As Integer, usram_writeP_clkfreq As Double, usram_writeP_enablerate As String, usram_readP_depth As Integer, usram_readP_width As Integer, usram_readP_clkfreq As Double, usram_read-
    ```

```
P_enablerate As String, usram_optimizemode_cb As String, usram_togglerate
As String, usram_useregisters_cb As String)
```

15. To instantiate the uSRAM in the IP, use setUSRAM (parameters) and pass the values to instantiate.
```
Function setUSRAM (usram_module_name As String, usram_writeP_depth As
Integer, usram_writeP_width As Integer, usram_writeP_clkfreq As Double,
usram_writeP_enablerate As String, usram_readP_depth As Integer,
usram_readP_width As Integer, usram_readP_clkfreq As Double, usram_read-
P_enablerate As String, usram_optimizemode_cb As String, usram_togglerate
As String, usram_useregisters_cb As String)
```
16. To instantiate Power Estimator settings in the IP, use InitPowerEstimator(parameters) and pass the values to instantiate.
```
Function InitPowerEstimator (fpga_sys_clk As String, cb_init_fabric As
String, fpga_reg_txt As String, fpga_comb_txt As String, fpga_uram_txt As
String, fpga_lsram_txt As String, fpga_math_txt As String, io_tech As
String, inputs_tb As String, outputs_tb As String, default_tr_txt As
String, default_er_txt As String, ok_append As String, ok_clear As String,
reset_button As String)
```
17. To import MPE settings from previous saved report, use import (parameters).
```
Function import (estimator_rb As String, smartpower_rb As String, imp_ap-
pend_data As String, imp_overwrite_data As String, Imp_device_settings As
String, Imp_thermal_inputs As String, Imp_voltage_settings As String,
Imp_snapshots As String, file_path As String)
```
18. To take a snapshot, use createSnapshot (parameters) and pass the values "True" or "False"
```
Function createSnapshot (snapshot As String)
```
19. To delete an IP, use deleteIP (parameters) and pass the IP to be deleted.
```
Function deleteIP (manage_ip_name As String)
```
20. To reset IP, use resetToDefault (parameters) and pass the resetting modes.
```
Function resetToDefault (reset_data As String, reset_all_settings As
String, reset_all_settings_snapshots As String)
```

Note: The user inputs should be correct combination to avoid errors. If wrong values are entered, a DRC (Design Rule Check(s)) should be performed. The current version of the power estimator does not have a common DRC system.

Python Script example to use the APIs:

```
import win32com.client

xl = win32com.client.Dispatch("Excel.Application")

xl.Workbooks.Open(Filename = "D:\PolarFire_Power_Estimator.xlsm", ReadOnly =
1)

xl.Application.Run("setDeviceInfo", "MPF300XT", "FCG484", "Extended", "STD")
```

6 Appendix 2: Additional Documentation

This document assumes that the reader has a good understanding of the PolarFire and PolarFire SoC devices, is experienced in digital and analog board design, and knowledgeable in the electrical characteristics of systems. Background information on the key theories and concepts of FPGA design is available in *High Speed Digital Design: A Handbook of Black Magic*[1] and other industry literature. The following documents provide additional information about the PolarFire FPGA architecture and help use Power Estimator effectively:

- *PolarFire SoC Advance Product Overview*
- *UG0880: PolarFire SoC MSS User Guide*
- *UG0881: PolarFire SoC FPGA Booting And Configuration User Guide*
- *UG0888: PolarFire SoC Trace and Debug User Guide*
- *UG0886: PolarFire SoC FPGA Peripherals User Guide*
- *UG0902: PolarFire SoC FPGA Packaging and Pin Descriptions User Guide*
- *UG0901: PolarFire SoC Board Design Guidelines User Guide*
- *UG0890: PolarFire SoC FPGA Power-Up and Resets User Guide*
- *PolarFire SoC Packaging Pin Assignment Table (PPAT)*
- *PolarFire SoC FPGA Advance Datasheet*
- *UG0905: PolarFire SoC FPGA System Services User Guide*
- *UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide*
- *UG0904: PolarFire SoC FPGA Gigabit Ethernet MAC User Guide*
- *UG0912: PolarFire SoC FPGA Fabric User Guide*
- *UG0916: PolarFire SoC FPGA IO User Guide*
- *UG0915: PolarFire SoC FPGA Transceiver User Guide*
- *UG0913: PolarFire SoC FPGA Clocking Resources User Guide*
- *UG0914: PolarFire SoC FPGA Programming User Guide*
- *UG0918: PolarFire SoC FPGA Security User Guide*

1.Johnson, Howard, and Martin Graham, High Speed Digital Design: A Handbook of Black Magic. Prentice Hall PTR, 1993. ISBN-10 0133957241 or ISBN-13: 978-0133957242