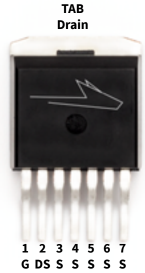
C3M0032120J1

Silicon Carbide Power C3M^{TM} MOSFET Technology
N-Channel Enhancement Mode

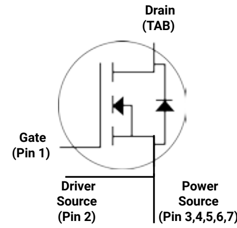
Features

- 3rd generation Silicon Carbide (SiC) MOSFET technology
- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant



Halogen-Free

RoHS compliant



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Part Number	Package	Marking
C3M0032120J1	TO 263-7L XL	C3M0032120J1

Applications

- Solar inverters
- EV motor drive
- High voltage DC/DC converters
- Switched mode power supplies
- Load switch

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	V	$T_C = 25°C$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19	V	Transient	
Operational Gate-Source Voltage	$V_{GS\ op}$		-4/15		V	Static	Note 1
DC Continuous Drain Current	I_D			68	A	$V_{GS} = 15$ V, $T_C = 25$ °C, $T_J \leq 150$ °C	Fig. 19 Note 2
				44	A	$V_{GS} = 15$ V, $T_C = 100$ °C, $T_J \leq 150$ °C	
Pulsed Drain Current	I_{DM}			120	A	t_{Pmax} limited by T_{jmax} $V_{GS} = 15$V, $T_C = 25$ °C	Fig. 22
Power Dissipation	P_D			277	W	$T_C = 25$ ˚C, $T_J = 150$ °C	Fig. 20
Operating Junction Temperature	T_J			-40 to +175	°C		
Case and Storage Temperature	T_C, T_{stg}			-40 to 150	°C		
Solder Temperature	T_L			260	°C	According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

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Electrical Characteristics (T_C = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200	—	—	V	V_{GS} = 0 V, I_D = 100 µA	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.7	3.6	V	V_{DS} = V_{GS}, I_D = 11.5 mA, T_J = 25°C	Fig. 11
		—	2.2	—		V_{DS} = V_{GS}, I_D = 11.5 mA, T_J = 150°C	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	50	µA	V_{DS} = 1200 V, V_{GS} = 0 V	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance	$R_{DS(on)}$	23	32	43	mΩ	V_{GS} = 15 V, I_D = 41.4 A, T_J = 25°C	Fig. 4, 5, 6
		—	55	—		V_{GS} = 15 V, I_D = 41.4 A, T_J = 150°C	
Transconductance	g_{fs}	—	25	—	S	V_{DS} = 20 V, I_{DS} = 41.4 A, T_J = 25°C	Fig. 7
			24			V_{DS} = 20 V, I_{DS} = 41.4 A, T_J = 175°C	
Input Capacitance	C_{iss}	—	3424	—	pF	V_{GS} = 0 V, V_{DS} = 1000 V ƒ = 100 khz V_{AC} = 25 mV	Fig. 17, 18
Output Capacitance	C_{oss}	—	133	—			
Reverse Transfer Capacitance	C_{rss}	—	11	—			
Output Capacitance Stored Energy	E_{oss}	—	72	—	µJ		Fig. 16
Turn-On Switching Energy (Body Diode FWD)	E_{on}	—	360	—	µJ	V_{DS} = 800 V, V_{GS} = -4 V/15 V, I_D = 41.4 A, $R_{G(ext)}$ = 2.5 Ω, L= 99 µH	Fig. 26
Turn-Off Switching Energy (Body Diode FWD)	E_{off}	—	90	—			
Turn-On Delay Time	$t_{d(on)}$	—	15	—	ns	V_{DD} = 800 V, V_{GS} = -4 V/15 V I_D = 41.4 A, $R_{G(ext)}$ = 2.5 Ω, L= 99 µH Timing relative to V_{DS} Inductive load	Fig. 27
Rise Time	t_r	—	16	—			
Turn-Off Delay Time	$t_{d(off)}$	—	25	—			
Fall Time	t_f	—	7	—			
Internal Gate Resistance	$R_{G(int)}$	—	1.6	—	Ω	ƒ = 1 MHz, V_{AC} = 25 mV	
Gate to Source Charge	Q_{gs}	—	40	—	nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_D = 41.4 A Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—	28	—			
Total Gate Charge	Q_g	—	111	—			

Reverse Diode Characteristics (T_C = 25°C unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage	V_{SD}	5.0	—	V	V_{GS} = -4 V, I_{SD} = 20 A, T_J = 25°C	Fig. 8, 9, 10
Diode Forward Voltage		4.5	—			
Continuous Diode Forward Current	I_S	—	49	A	V_{GS} = -4 V, T_J = 150°C, I_{SD} = 20 A,	Note 1
Diode Pulse Current	$I_{S, pulse}$	—	120		V_{GS} = -4 V, pulse width t_P limited by $T_{j\,max}$	Note 1
Reverse Recovery Time	t_{rr}	13	—	ns	V_{GS} = -4 V, I_{SD} = 41.4 A, V_R = 800 V, di_F/dt = 7450 A/µs, T_J = 150°C	Note 1
Reverse Recovery Charge	Q_{rr}	323	—	nC		
Peak Reverse Recovery Current	I_{RRM}	45	—	A		
Reverse Recovery Time	t_{rr}	18	—	ns	V_{GS} = -4 V, I_{SD} = 41.4 A, V_R = 800 V, di_F/dt = 2200 A/µs, T_J = 150°C	Note 1
Reverse Recovery Charge	Q_{rr}	164	—	nC		
Peak Reverse Recovery Current	I_{RRM}	16	—	A		

Thermal Characteristics

Parameter	Symbol	Typ	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.45	°C/W	Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	40		

Typical Performance

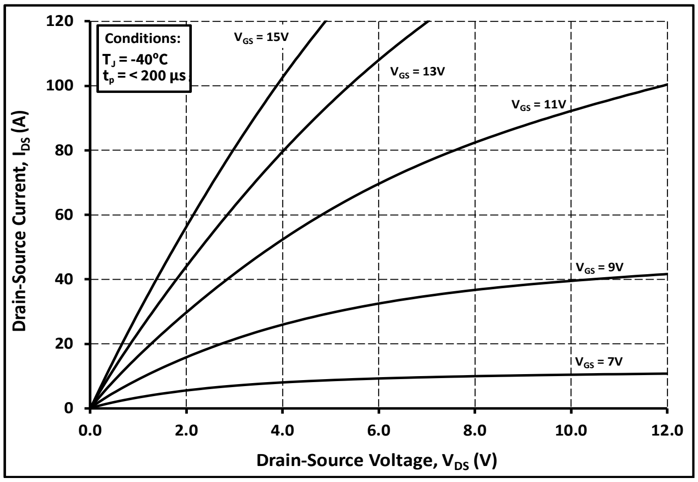


Figure 1. Output Characteristics T_J = -40°C

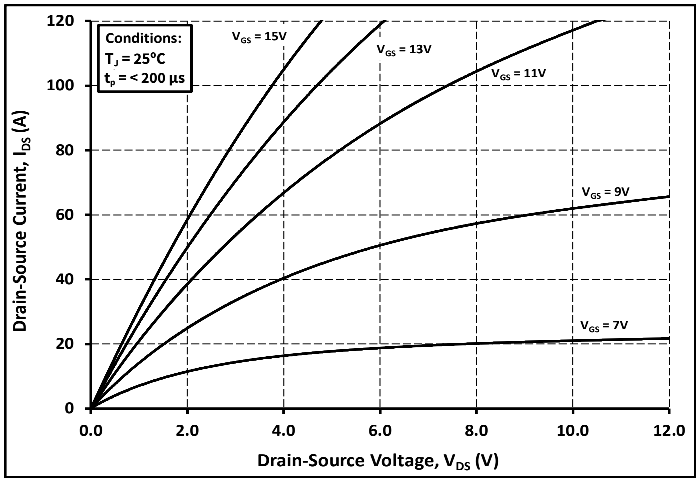


Figure 2. Output Characteristics T_J = 25°C

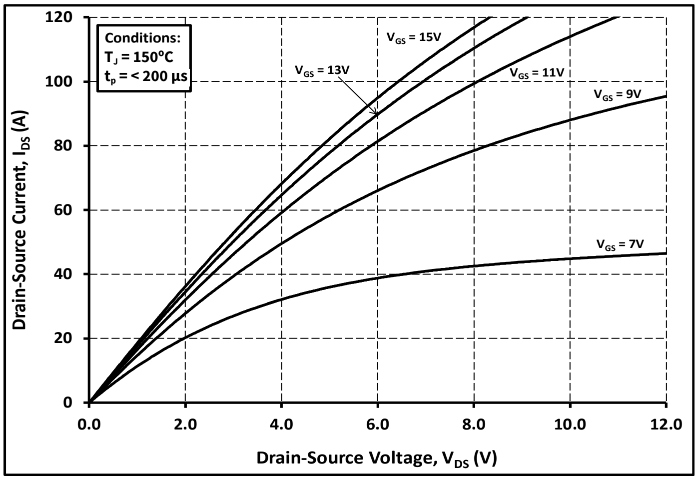


Figure 3. Output Characteristics T_J = 150°C

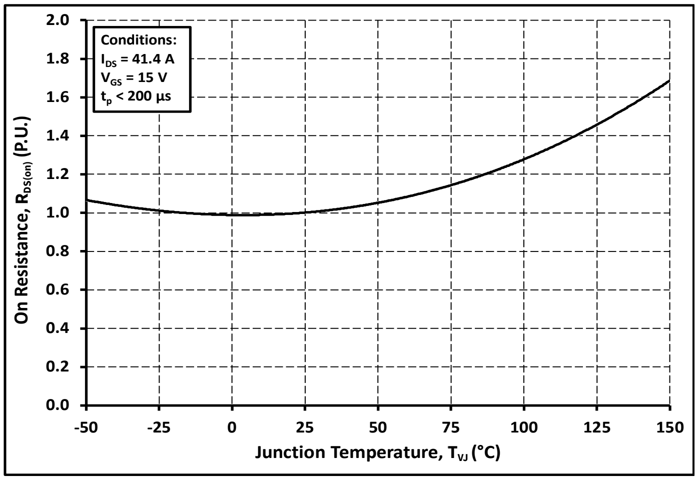


Figure 4. Normalized On-Resistance vs Temperature

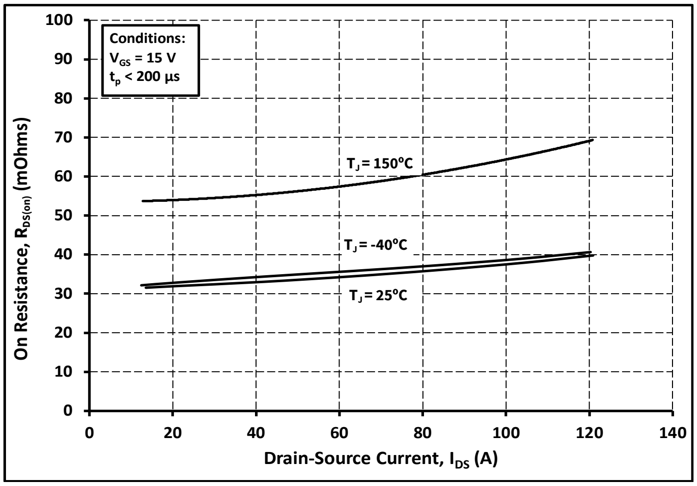


Figure 5. On-Resistance vs Drain Current
For Various Temperatures

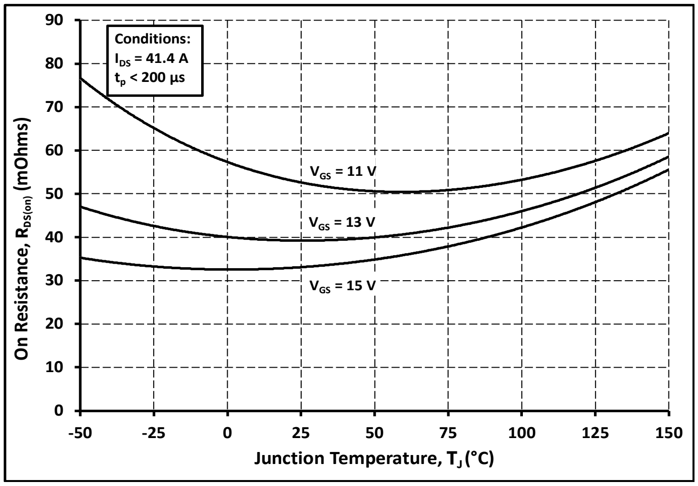


Figure 6. On-Resistance vs Temperature
For Various Gate Voltage

Typical Performance

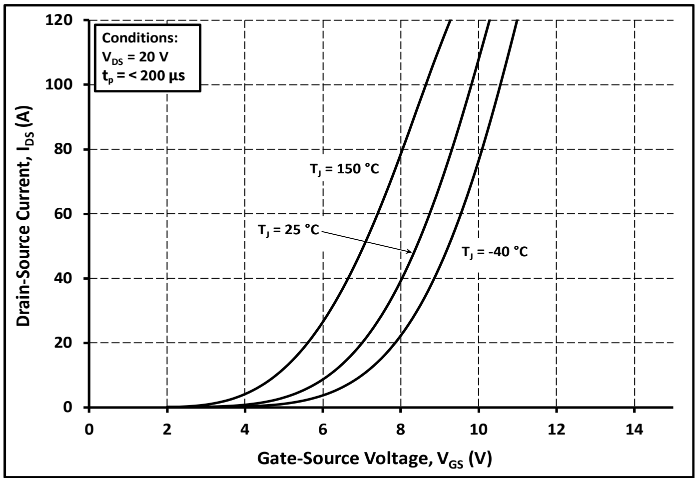


Figure 7. Transfer Characteristic for Various Junction Temperatures

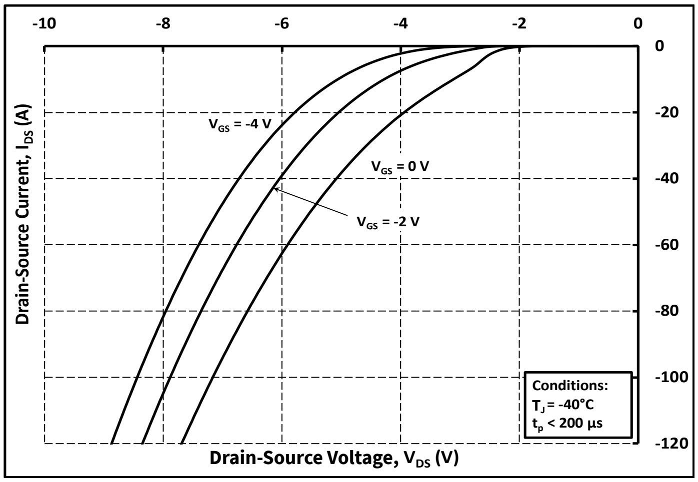


Figure 8. Body Diode Characteristic at -40°C

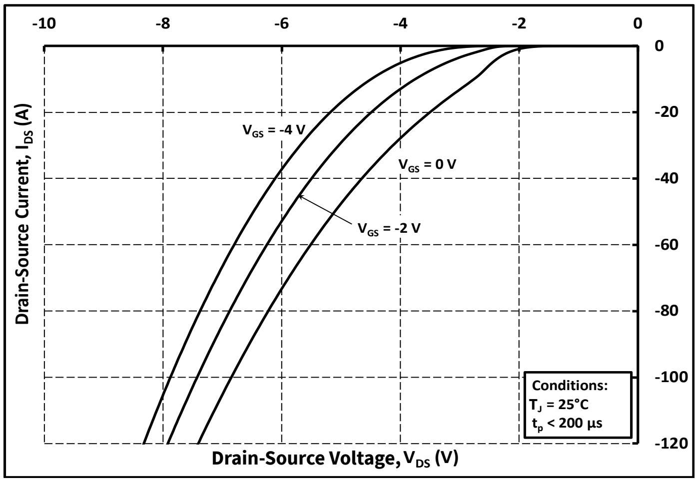


Figure 9. Body Diode Characteristic at 25°C

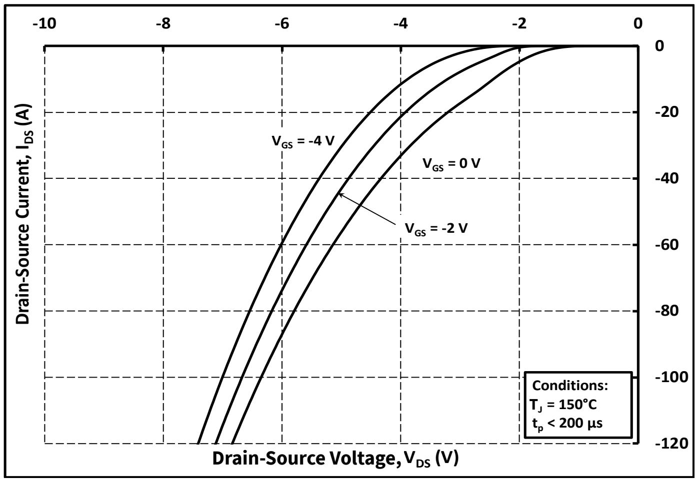


Figure 10. Body Diode Characteristic at 150°C

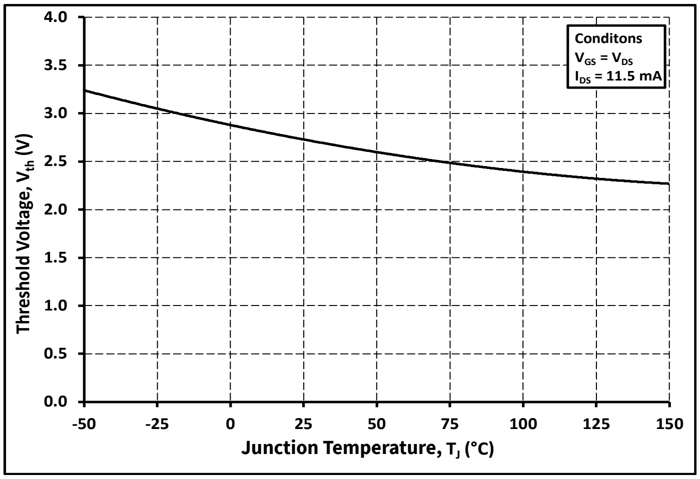


Figure 11. Threshold Voltage vs Temperature

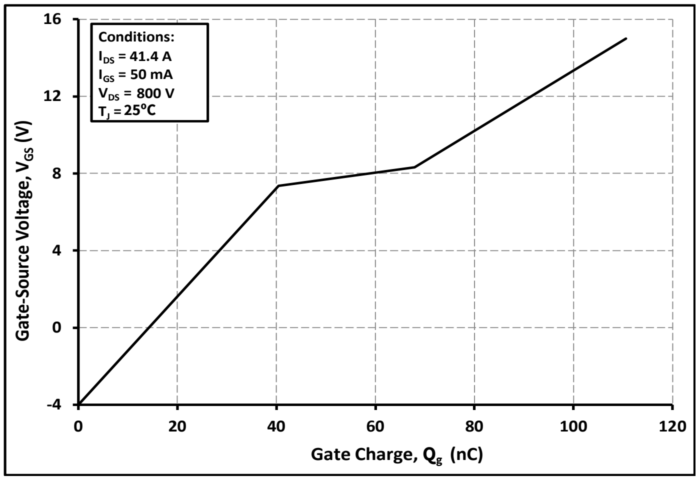


Figure 12. Gate Charge Characteristics

Typical Performance

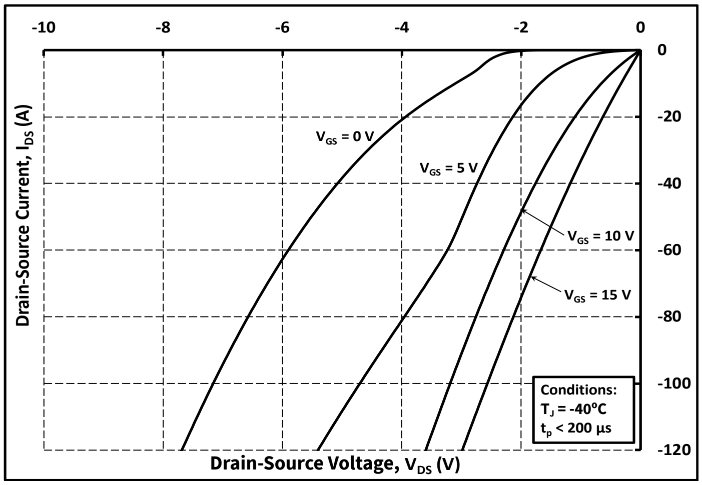


Figure 13. 3rd Quadrant Characteristic at -40°C

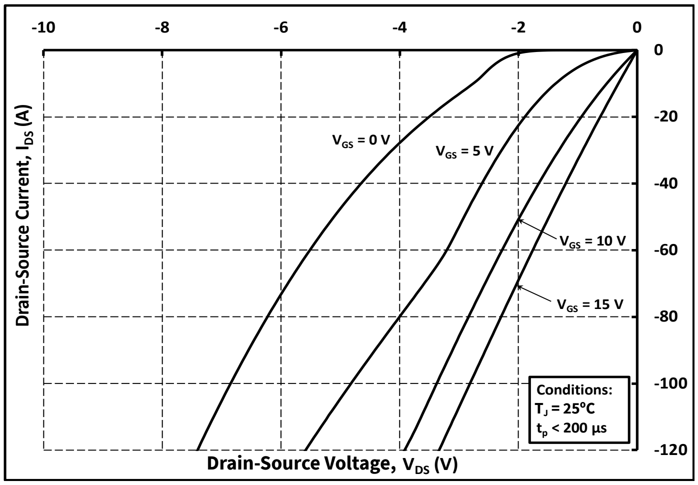


Figure 14. 3rd Quadrant Characteristic at 25°C

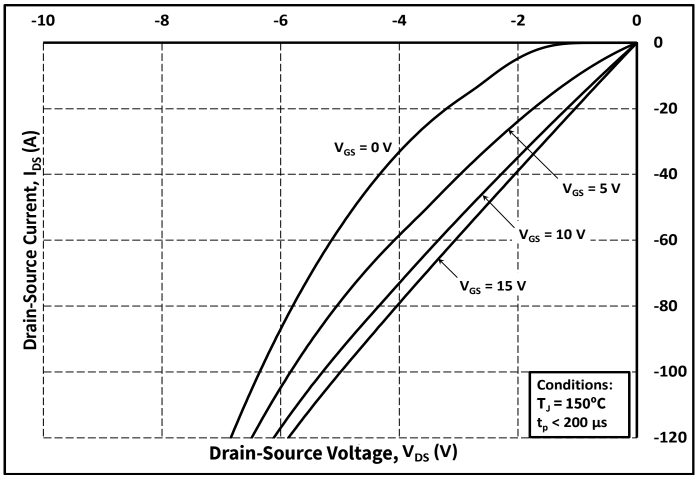


Figure 15. 3rd Quadrant Characteristic at 150°C

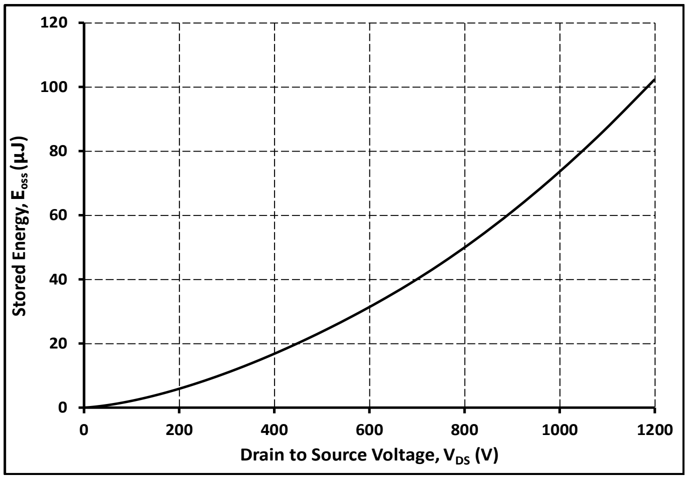


Figure 16. Output Capacitor Stored Energy

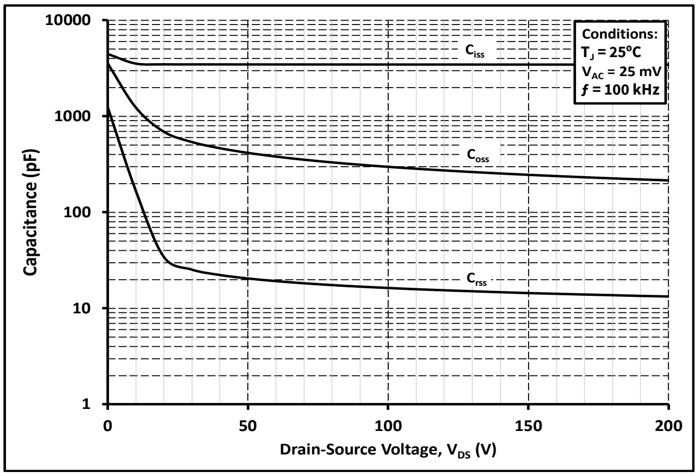


Figure 17. Capacitances vs Drain-Source Voltage (0 - 200 V)

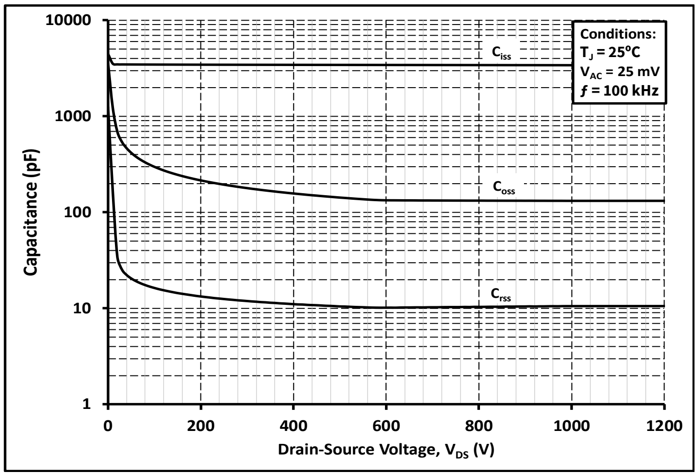


Figure 18. Capacitances vs Drain-Source Voltage (0 - 1200 V)

Typical Performance

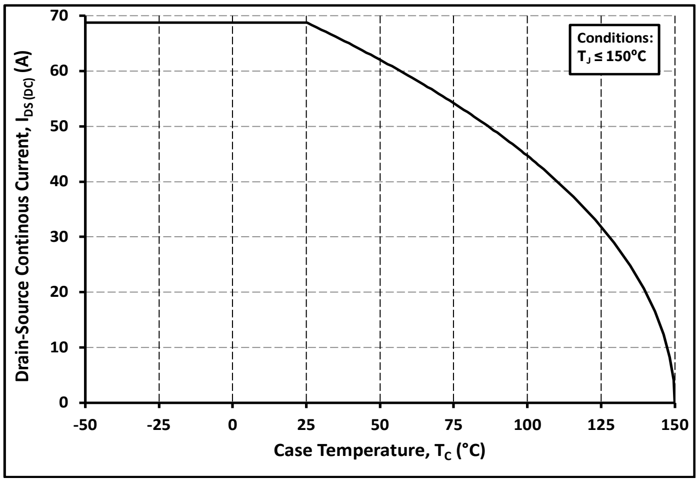


Figure 19. Continuous Drain Current Derating vs Case Temperature

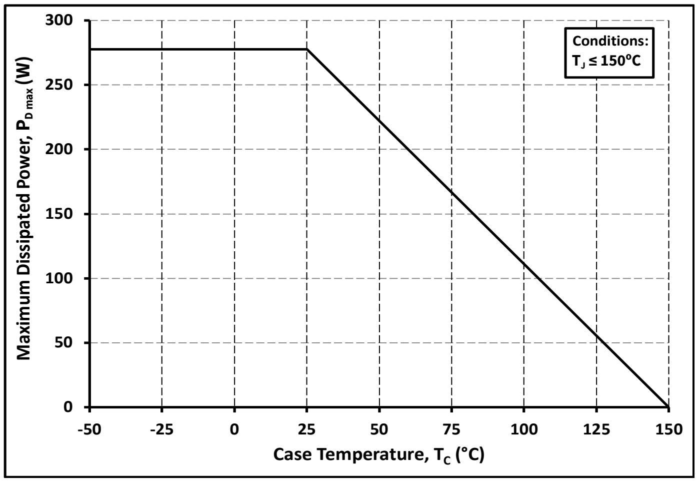


Figure 20. Maximum Power Dissipation Derating vs Case Temperature

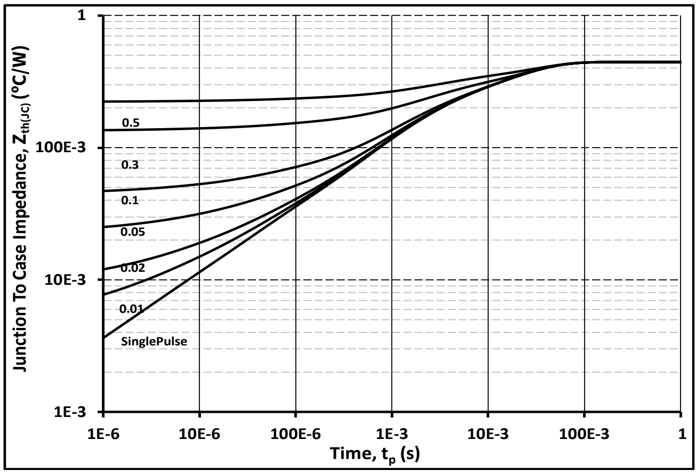


Figure 21. Transient Thermal Impedance (Junction - Case)

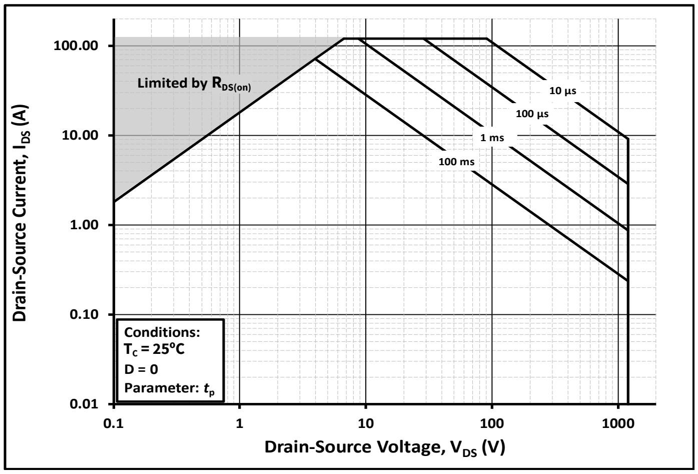


Figure 22. Safe Operating Area

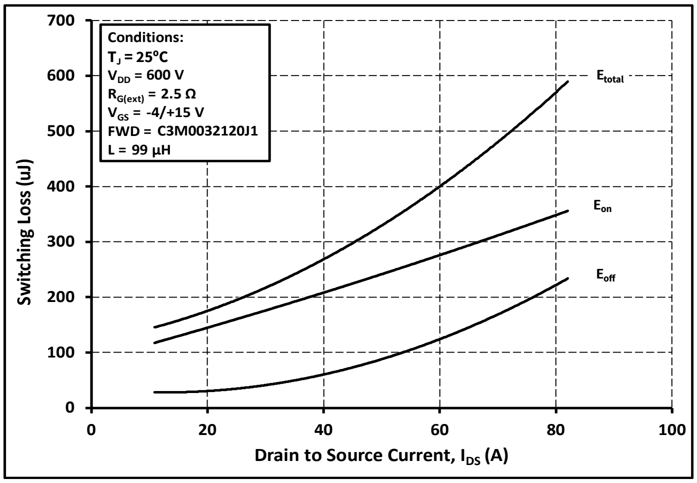


Figure 23. Clamped Inductive Switching Energy vs Drain Current (V_{DD} = 600 V)

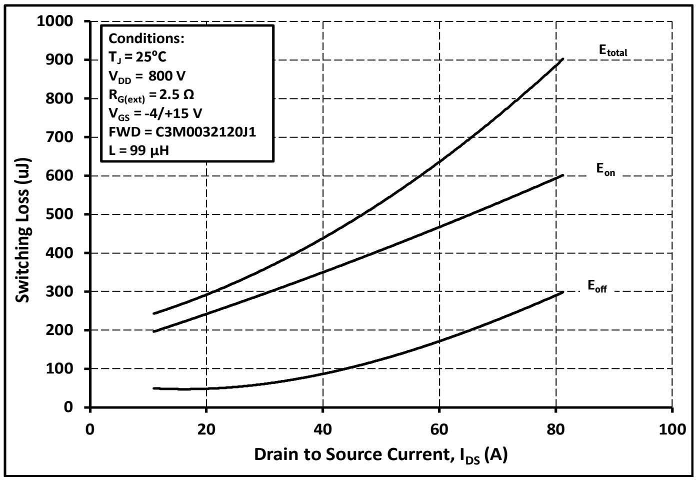


Figure 24. Clamped Inductive Switching Energy vs Drain Current (V_{DD} = 800 V)

Typical Performance

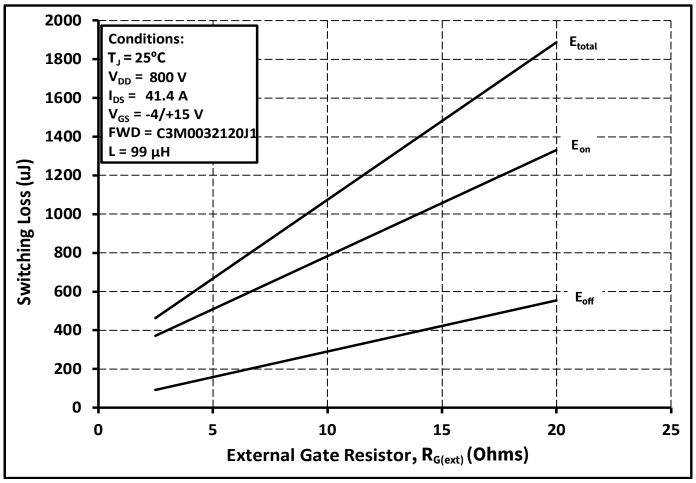


Figure 25. Clamped Inductive Switching Energy vs $R_{G(ext)}$

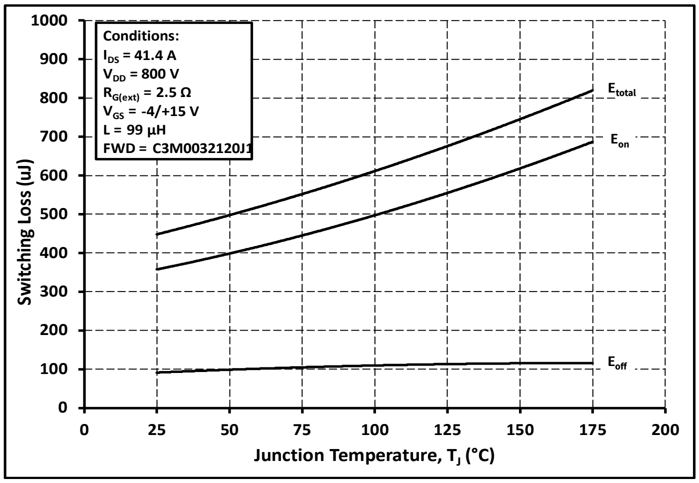


Figure 26. Clamped Inductive Switching Energy vs Temperature

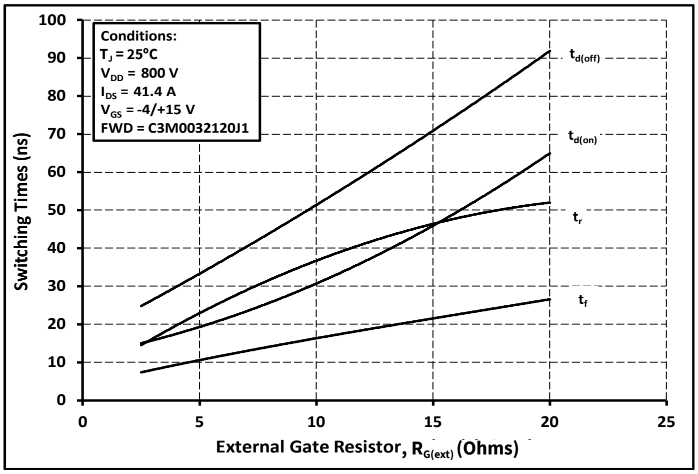


Figure 27. Switching Times vs. $R_{G(ext)}$

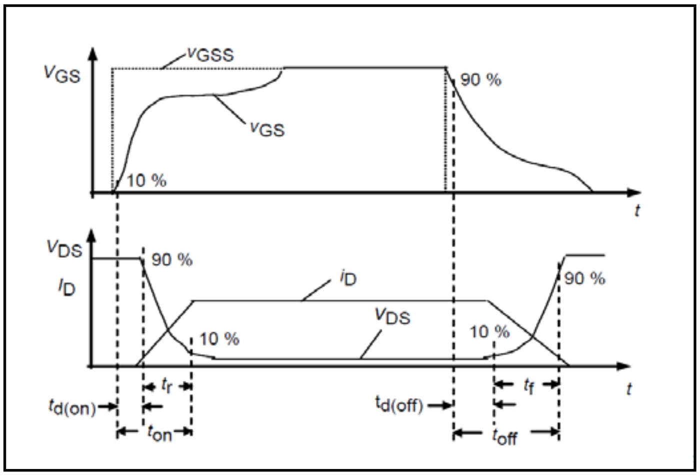


Figure 28. Switching Times Definition

Test Circuit Schematic

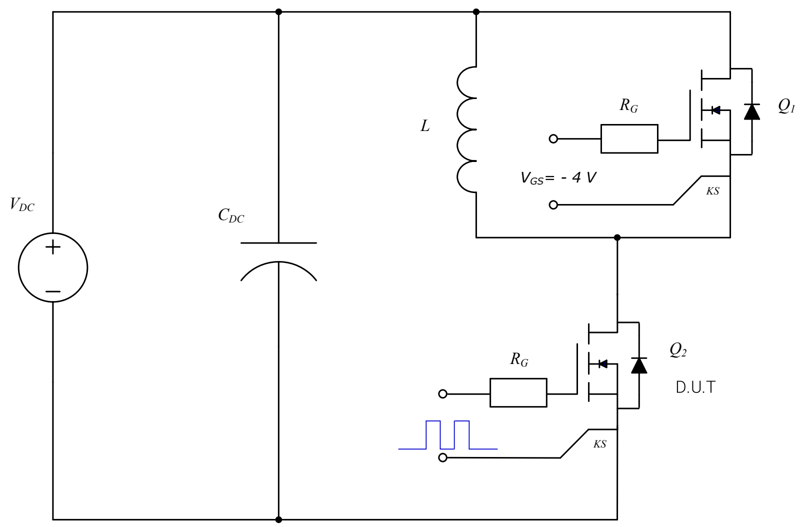
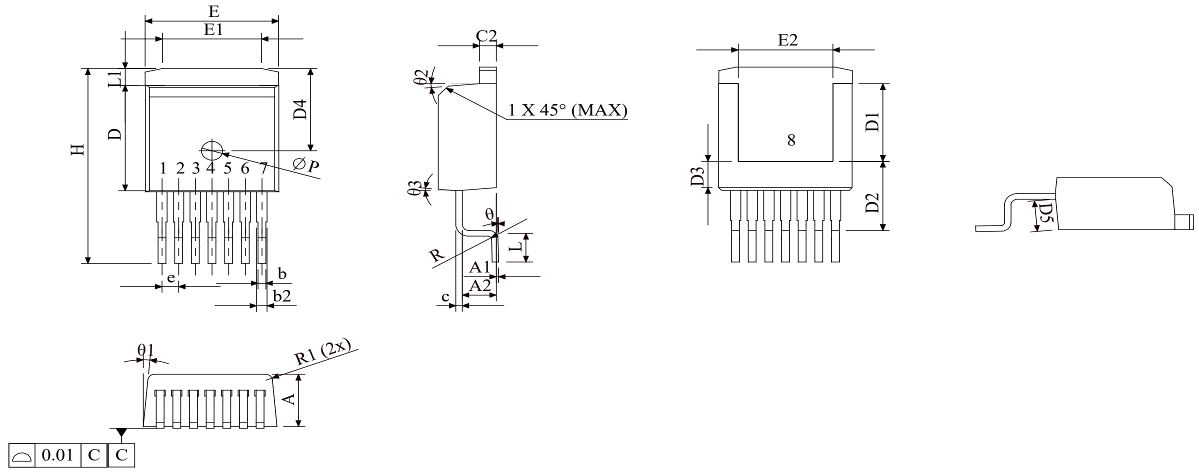


Figure 29. Clamped Inductive Switching Waveform Test Circuit

Note:
Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

Package Dimensions – Package TO-263-7L XL



SYMBOL	MIN (mm)	MAX (mm)
A	4.30	4.57
A1	0.00	0.25
A2	2.595 REF	
b	0.50	0.70
b2	0.60	1.00
c	0.281	0.481
C2	1.17	1.37
D	9.025	9.125
D1	6.50	6.70
D2	5.39 REF	
D3	2.148	---
D4	7.000 REF	
D5	2.555	---
A2	2.595 REF	
E	10.13	10.23
E1	6.50	8.60
E2	6.778	7.665
e	1.27 TYP	
H	15.043	17.313
L	2.324	2.700
L1	0.968	1.868
R	0.506 REF	
R1	0.500 REF	
P	1.60 REF	
θ	0°	8°
θ1	4.5°	5.5°
θ2	4°	6°
θ3	4°	6°

1	GATE
2	KELVIN
3	SOURCE
4	SOURCE
5	SOURCE
6	SOURCE
7	SOURCE
8	DRAIN

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

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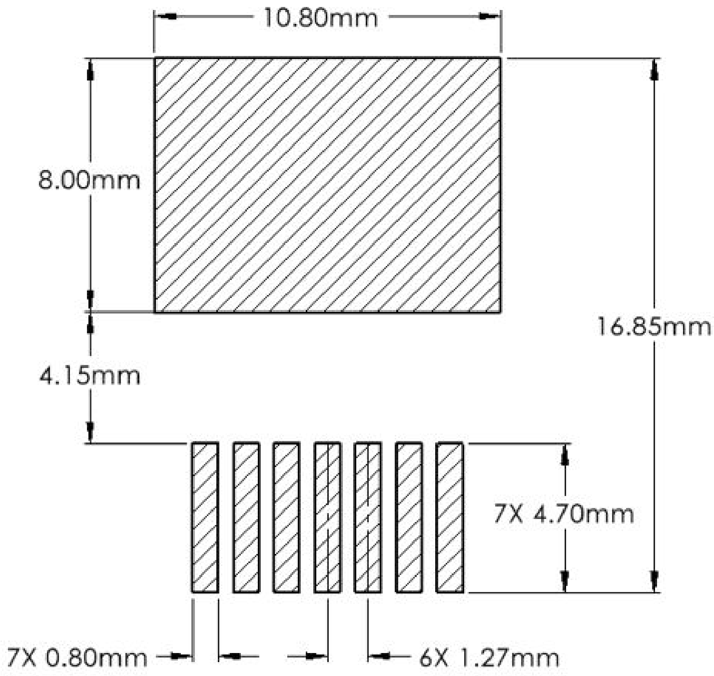
TITLE: PACKAGE OUTLINE DRAWING: TO 263-7L J1

REVISION NO. 01 A4

Date: 04/13/22 SCALE:1:1 SHEET 1 OF 1

Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
2	December-2020	N/A
3	December-2023	Updated Wolfspeed branding, package drawing, package image, solder pad layout, added Rev history, Table 1 layout revised

Related Links

- SPICE Models
- SiC MOSFET Isolated Gate Driver reference design
- SiC MOSFET Evaluation Board

Notes & Disclaimer

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This product has not been designed or tested for use in, and is not intended for use in, applications in which failure of the product would reasonably be expected to cause death, personal injury, or property damage, including but not limited to equipment implanted into the human body, life-support machines, cardiac defibrillators, and similar emergency medical equipment, aircraft navigation, communication, and control systems, aircraft power and propulsion systems, air traffic control systems, and equipment used in the planning, construction, maintenance, or operation of nuclear facilities.

The Silicon Carbide MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Documentation sections of www.wolfspeed.com.

REACh Compliance

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

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