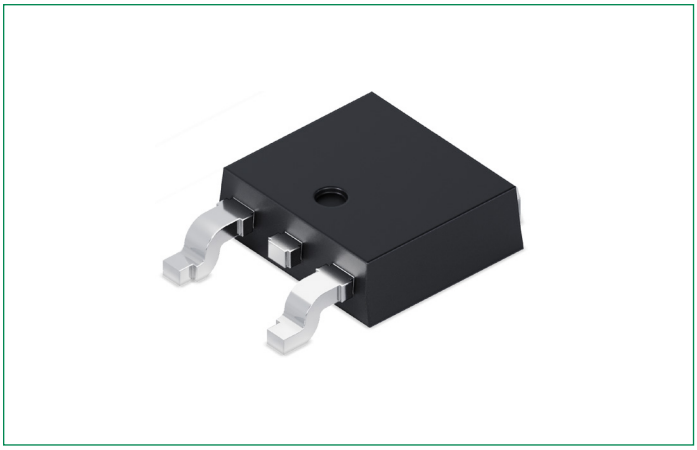
IXTY2P50PA

–500 V, –2 A PolarP™ MOSFET

P-Channel Enhancement Mode

RoHS HF



Features & Benefits:

- AEC Q101 Qualified
- Avalanche Rated
- Rugged PolarP™ Process
- Low Package Inductance
- Easy to Mount
- Space Savings

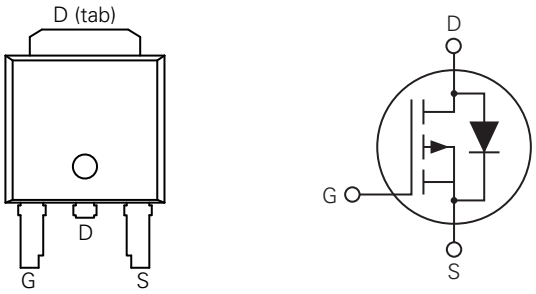
Applications:

- High-side Switches
- Push Pull Amplifiers
- DC Choppers
- Automatic Test Equipment
- Current Regulators

Product Summary

Characteristics	Value	Unit
V_{DSS}	–500	V
$R_{DS(on),max}$	4.2	Ω
I_{D25}	–2	A

Pinout Diagram (TO-252)



G: Gate; **D:** Drain; **S:** Source; **tab:** Drain

Revised: XZ 07/12/2023

Maximum Ratings

Symbol	Characteristics	Conditions	Value	Units
V_{DSS}	Drain-Source Voltage	T_J = 25 °C to 150 °C	–500	V
V_{GSS}	Gate-Source Voltage	Continuous	±20	V
V_{GSM}		Transient	±30	
I_{D25}	Drain Current	T_C = 25 °C	–2	A
I_{DM}		T_C = 25 °C, Pulse width limited by T_{JM}	–6	
I_A	Avalanche Current	T_C = 25 °C	–2	A
E_{AS}	Avalanche Energy	T_C = 25 °C	150	mJ
dV/dt	Reverse Diode dV/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150$ °C	10	V/ns
P_D	Power Dissipation	T_C = 25 °C	58	W
T_J	Operating Junction Temperature	–	–55 to +150	°C
T_{JM}	Maximum Junction Temperature	–	150	
T_{stg}	Storage Temperature	–	–55 to +150	
T_{sold}	Soldering Temperature	Plastic Body for 10 s	260	°C
W	Weight	–	0.35	g

Thermal Characteristics

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$R_{th, JC}$	Thermal Resistance, Junction-to-Case	–	–	2.15	°C/W

Electrical Characteristics – Static (T_J = 25 °C unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = –250 µA, V_{GS} = 0 V	–500	–	–	V
$V_{GS(th)}$	Gate Threshold Voltage	I_D = –50 µA, V_{GS} = V_{DS}	–2.5	–	–4.5	V
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±20 V	–	–	±50	nA
I_{DSS}	Drain-Source Current	V_{DS} = V_{DSS}, V_{GS} = 0 V	–	–	–1	µA
		V_{DS} = V_{DSS}, V_{GS} = 0 V, T_J = 125 °C	–	–	–5	
$R_{DS(on)}$	Drain-Source On-Resistance[1]	V_{GS} = –10 V, I_D = 0.5 x I_{D25}	–	–	4.2	Ω

Note 1: Pulse test, t ≤ 300 µs, duty cycle, d ≤ 2%

Electrical Characteristics – Dynamic (T_J = 25 °C unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
g_{fs}	Transconductance[1]	V_{DS} = –10 V, I_D = 0.5 x I_{D25}	1.4	2.4	–	S
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –25 V, f = 1MHz	–	600	–	pF
C_{oss}	Output Capacitance		–	70	–	
C_{rss}	Reverse Transfer Capacitance		–	12	–	
$Q_{g(on)}$	Total Gate Charge	V_{GS} = –10 V, V_{DS} = 0.5 x V_{DSS}, I_D = 0.5 x I_{D25}	–	11.9	–	nC
Q_{gs}	Gate-Source Charge		–	4.0	–	
Q_{gd}	Gate-Drain Charge		–	4.3	–	
$t_{d(on)}$	Turn-on Delay Time	**Resistive Switching** V_{GS} = –10 V, V_{DS} = 0.5 x V_{DSS}, I_D = 0.5 x I_{D25}, $R_{G(ext)}$ = 50 Ω	–	26	–	ns
t_r	Rise Time		–	62	–	
$t_{d(off)}$	Turn-off Delay Time		–	54	–	
t_f	Fall Time		–	66	–	

Note 1: Pulse test, t ≤ 300 µs, duty cycle, d ≤ 2%

Source-Drain Diode Characteristics (T_J = 25 °C unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
I_S	Continuous Diode Forward Current	V_{GS} = 0 V	–	–	-2	A
I_{SM}	Diode Pulse Current	Repetitive, Pusle width limited by T_{JM}	–	–	-8	A
V_{SD}	Diode Forward Voltage[1]	I_F = –2 A, V_{GS} = 0 V	–	–	-2.8	V
t_{rr}	Reverse Recovery Time	I_F = –1 A, –di/dt = –100 A/µs, V_r = –100 V, V_{GS} = 0 V	–	300	–	ns
Q_{rm}	Reverse Recovery Charge		–	3.9	–	µC
I_{rm}	Reverse Recovery Current		–	-26	–	A

Note 1: Pulse test, t ≤ 300 µs, duty cycle, d ≤ 2%

Characteristic Curves

Fig. 1. Output Characteristics @ T_J = 25 ºC

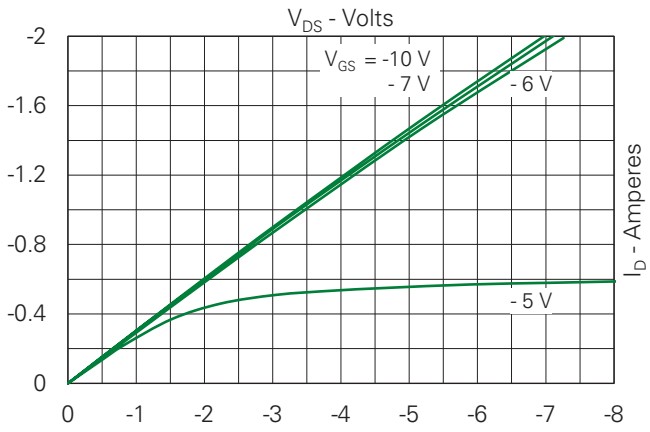


Fig. 2. Extended Output Characteristics @ T_J = 25 ºC

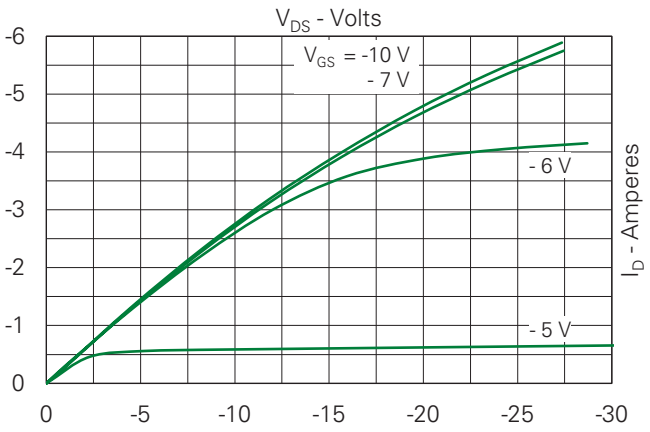


Fig. 3. Output Characteristics @ T_J = 125 ºC

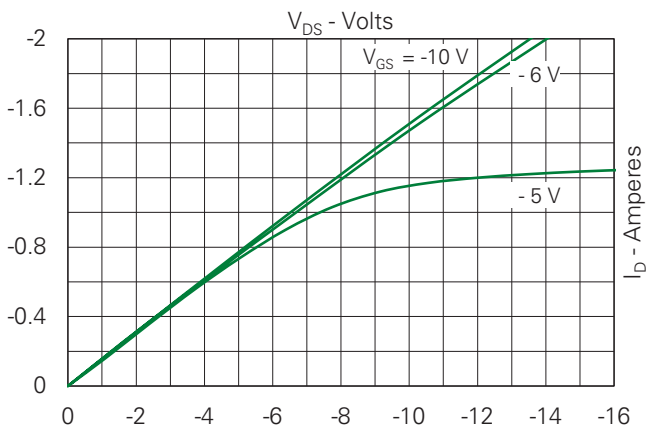


Fig. 4. $R_{DS(on)}$ Normalized to I_D = -1 A Value vs. Junction Temperature

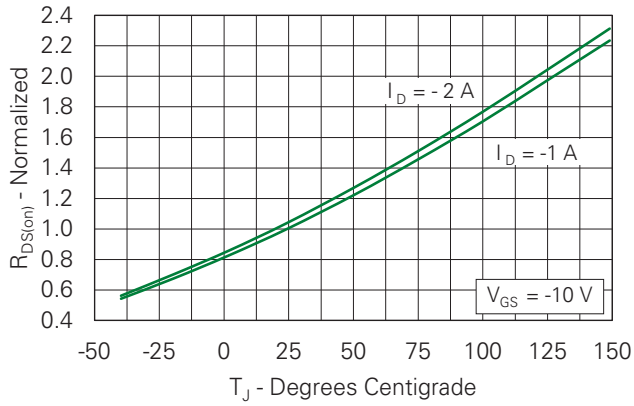


Fig. 5. $R_{DS(on)}$ Normalized to I_D = -1 A Value vs. Drain Current

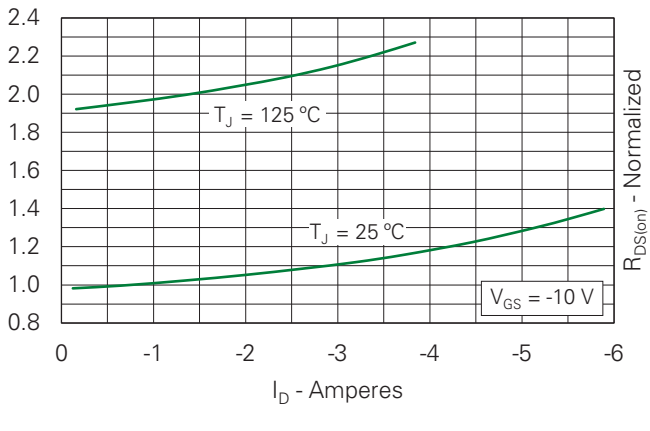


Fig. 6. Maximum Drain Current vs. Case Temperature

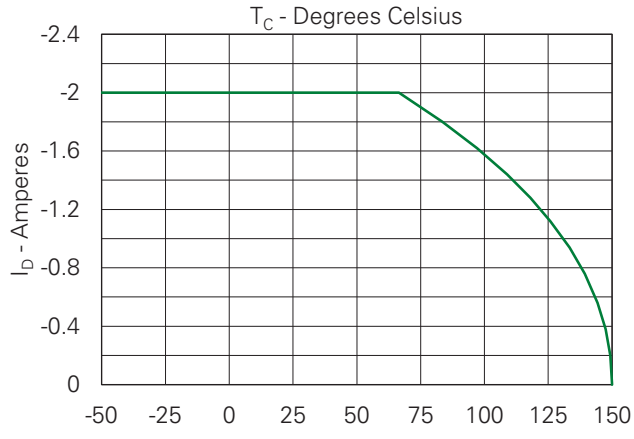


Fig. 7. Input Admittance

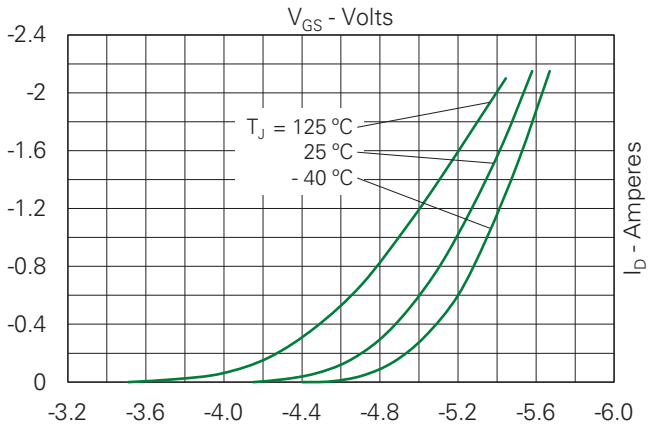


Fig. 8. Transconductance

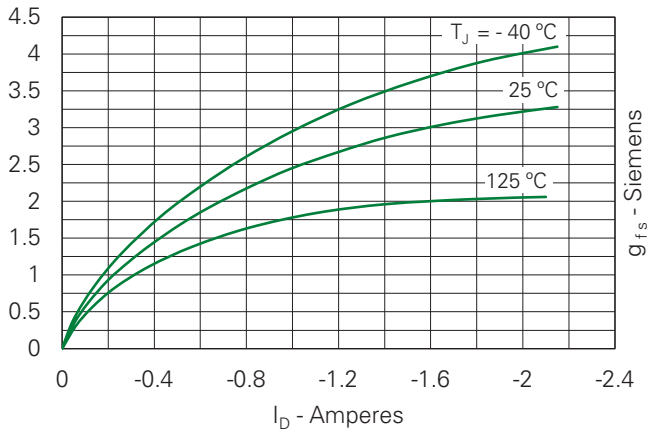


Fig. 9. Forward Voltage Drop of Intrinsic Diode

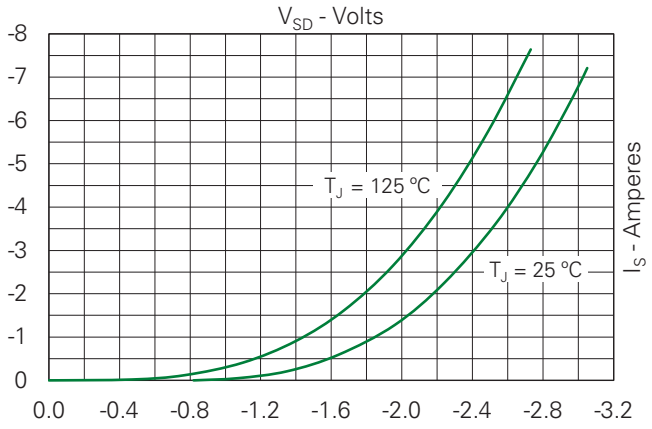


Fig. 10. Gate Charge

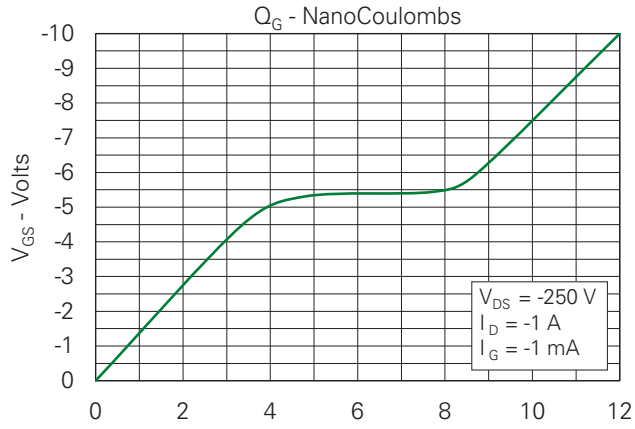


Fig. 11. Capacitance

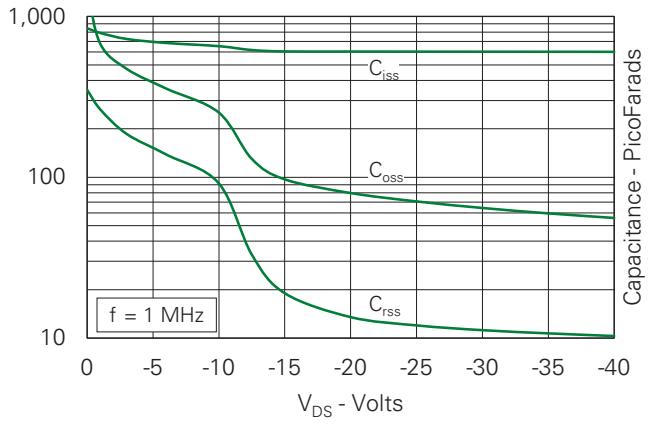


Fig. 12. Forward-Bias Safe Operating Area

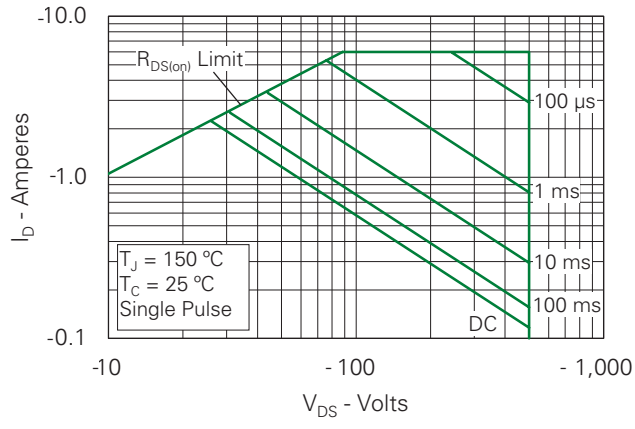
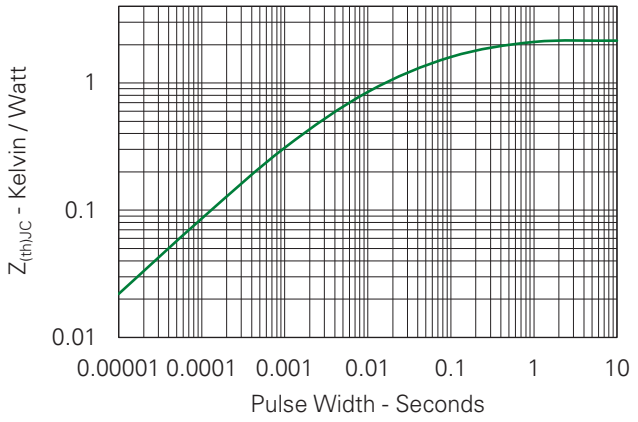
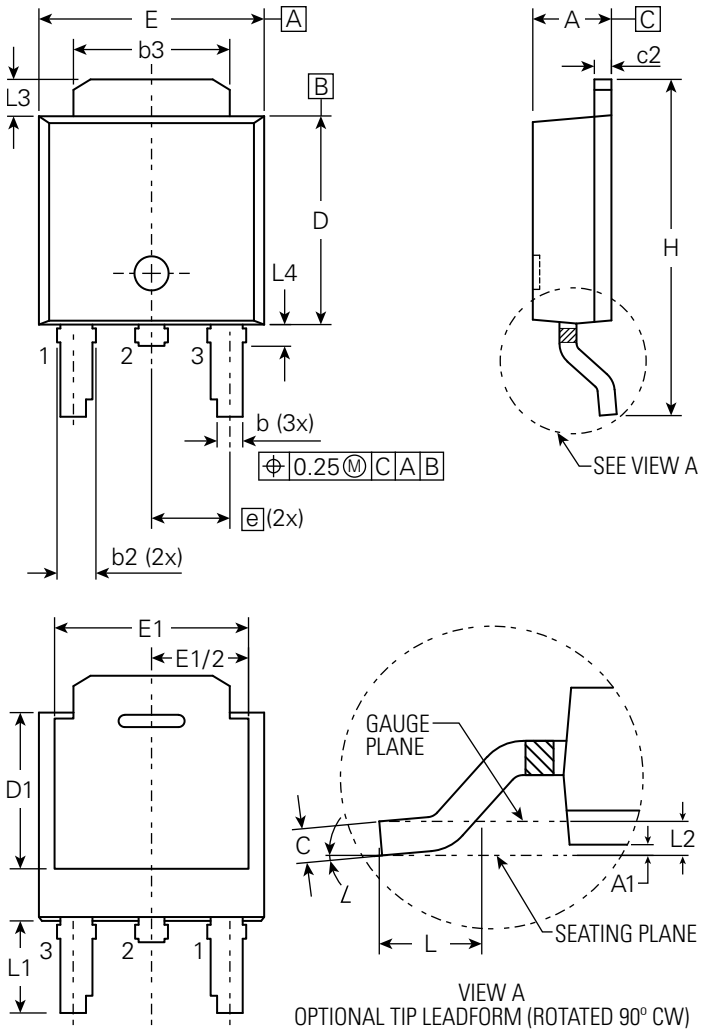


Fig. 13. Maximum Transient Thermal Impedance



Part Outline Drawing (TO-252)



Symbol	Inches			Millimeters		
	Min.	Typical	Max.	Min.	Typical	Max
A	0.086	0.090	0.094	2.18	2.28	2.38
A1	–	–	0.005	–	–	0.13
b	0.025	0.030	0.035	0.63	0.76	0.89
b2	0.028	0.037	0.045	0.72	0.93	1.14
b3	0.180	0.198	0.215	4.57	5.02	5.46
c	0.018	0.021	0.024	0.46	0.54	0.61
c2	0.018	0.021	0.024	0.46	0.54	0.61
D	0.235	0.240	0.245	5.97	6.10	6.22
D1	0.215	0.222	0.230	5.45	5.65	5.85
E	0.250	0.257	0.265	6.35	6.54	6.73
E1	0.202	0.210	0.218	5.14	5.34	5.54
e	–	0.090	–	–	2.29	–
H	0.370	0.390	0.410	9.40	9.91	10.41
L	0.055	0.063	0.070	1.40	1.59	1.78
L1	–	0.114	–	–	2.90	–
L2	–	0.020	–	–	0.51	–
L3	0.035	0.043	0.050	0.89	1.08	1.27
L4	–	0.020	0.040	–	0.51	1.01
∠	–	–	10 deg.	–	–	10 deg.