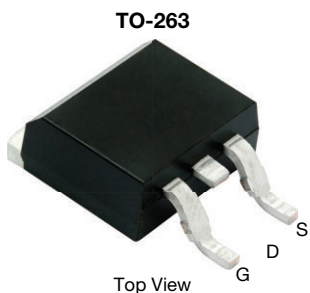


Automotive N-Channel 200 V (D-S) 175 °C MOSFET

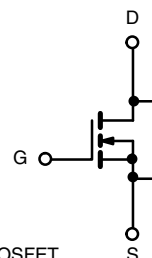


FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



PRODUCT SUMMARY

V _{DS} (V)	200
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.0153
I _D (A)	95
Configuration	Single
Package	TO-263

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	200	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current	I _D	T _C = 25 °C 95	A
		T _C = 125 °C 55	
Continuous source current (diode conduction) ^a	I _S	120	
Pulsed drain current ^b	I _{DM}	170	
Single pulse avalanche current	I _{AS}	64	
Single pulse avalanche energy	E _{AS}	205	mJ
Maximum power dissipation ^b	P _D	T _C = 25 °C 375	W
		T _C = 125 °C 125	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R _{thJA}	40	°C/W
Junction-to-case (drain)	R _{thJC}	0.4	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		200	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.5	3.0	3.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 200 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 200 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 200 V, T _J = 175 °C	-	-	600	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	40	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A	-	0.0127	0.0153	Ω
		V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	-	-	0.0310	
		V _{GS} = 10 V	I _D = 20 A, T _J = 175 °C	-	-	0.0404	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 20 A		-	54	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	3200	4200	pF
Output capacitance	C _{oss}			-	1300	1750	
Reverse transfer capacitance	C _{rss}			-	80	110	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 100 V, I _D = 9 A	-	55	85	nC
Gate-source charge ^c	Q _{gs}			-	14	-	
Gate-drain charge ^c	Q _{gd}			-	16.5	-	
Gate Resistance	R _g	f = 1 MHz		1.35	2.74	4.20	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 100 V, R _L = 11.1 Ω I _D ≅ 9 A, V _{GEN} = 10 V, R _g = 1 Ω		-	17	30	ns
Rise time ^c	t _r			-	8	15	
Turn-off delay time ^c	t _{d(off)}			-	39	60	
Fall time ^c	t _f			-	16	30	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}			-	-	170	A
Forward voltage	V _{SD}	I _F = 20 A, V _{GS} = 0 V		-	0.82	1.5	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs		-	129	260	ns
Body diode reverse recovery charge	Q _{rr}			-	685	1400	nC
Reverse recovery fall time	t _a			-	106	-	ns
Reverse recovery rise time	t _b			-	26	-	
Body diode peak reverse recovery current	I _{RM(REC)}			-	-11	-	A

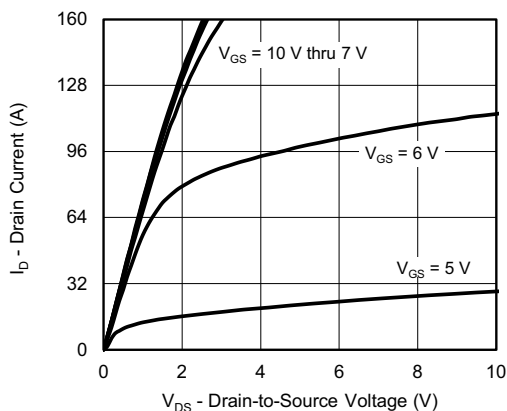
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

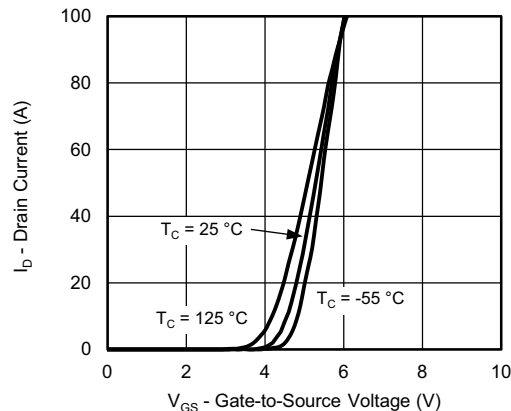
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



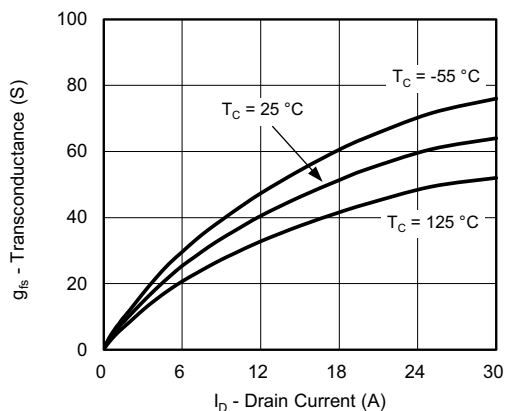
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



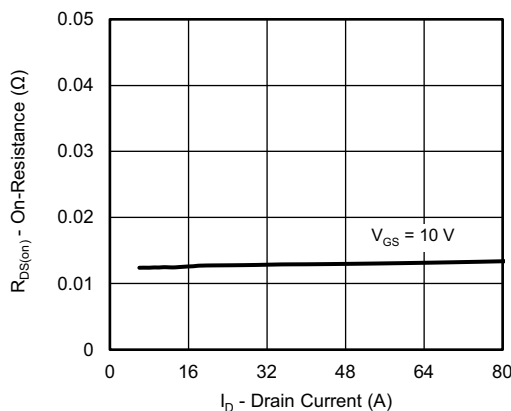
Output Characteristics



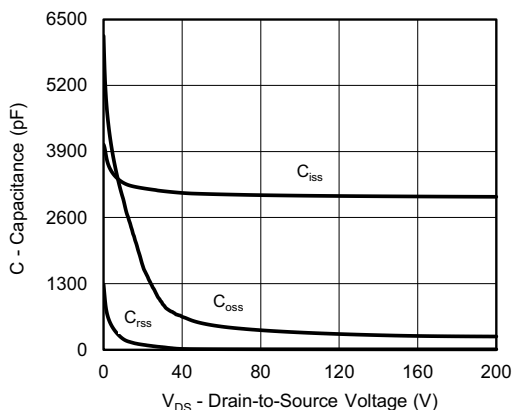
Transfer Characteristics



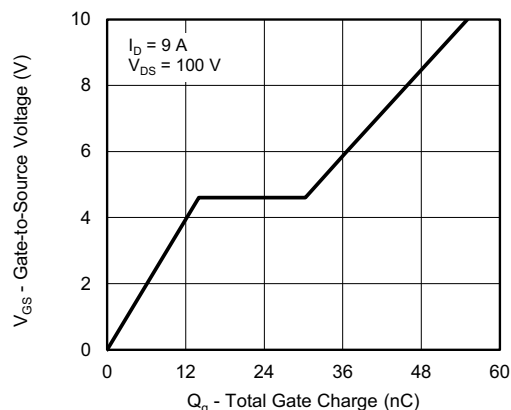
Transconductance



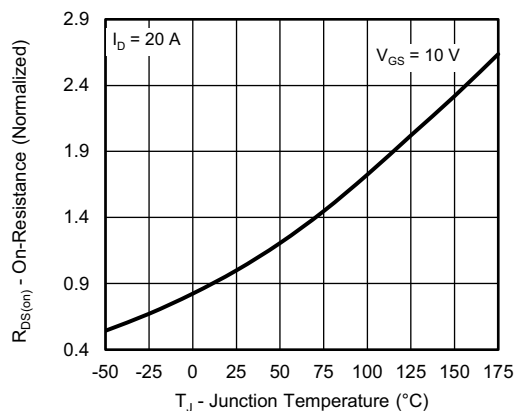
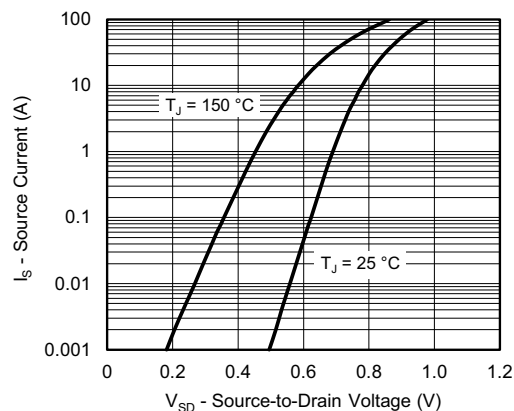
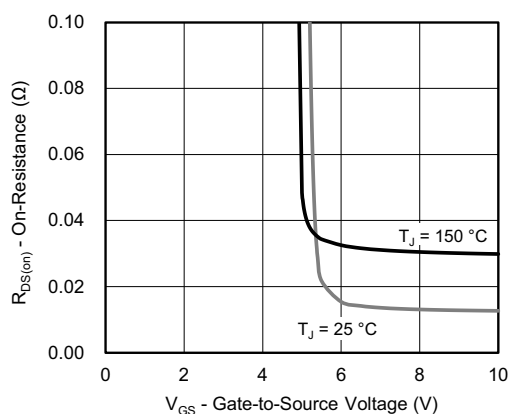
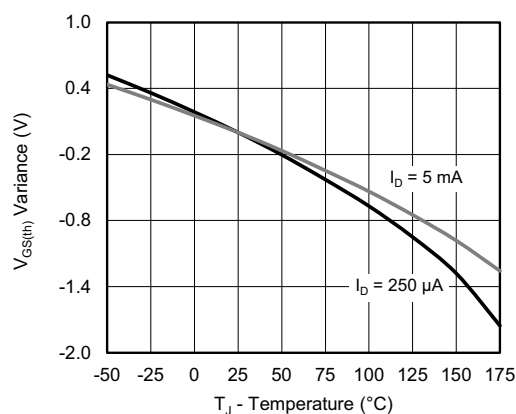
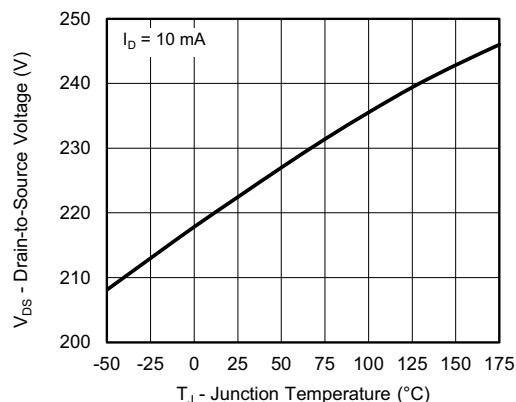
On-Resistance vs. Drain Current



Capacitance

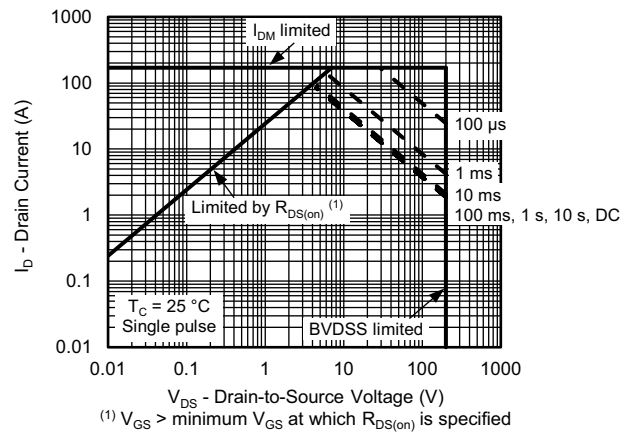


Gate Charge

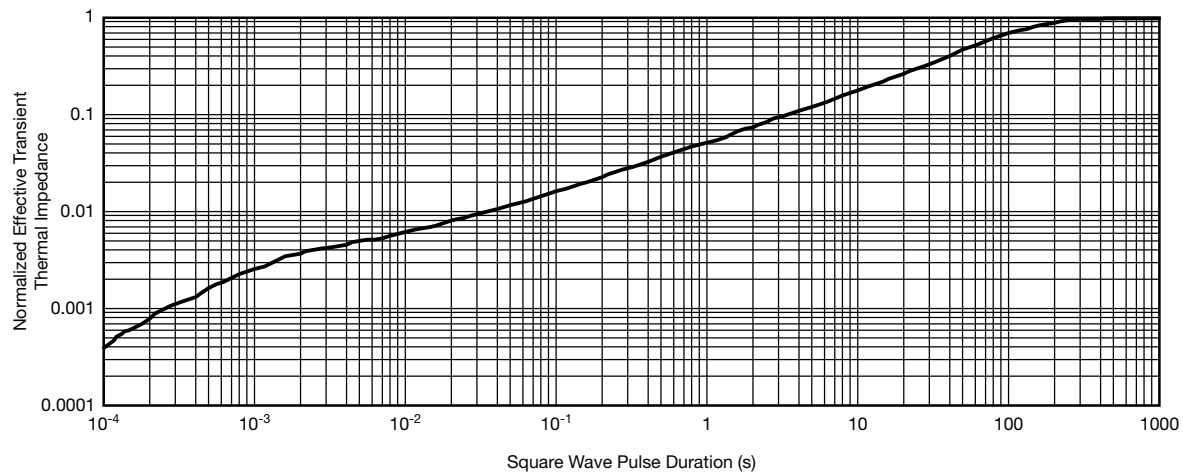
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



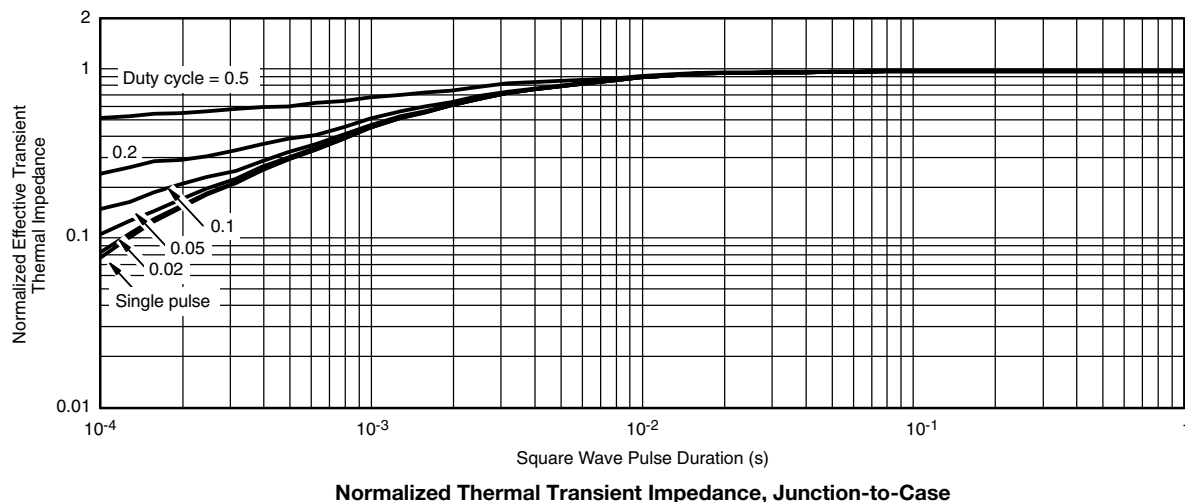
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction to Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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TO-263 (D²PAK): 3-LEAD



DETAIL A (ROTATED 90°)



SECTION A-A

Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

ECN: T13-0707-Rev. K, 30-Sep-13
DWG: 5843

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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