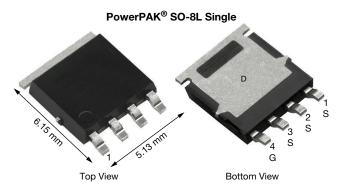
## SQJ860EP

www.vishay.com

**Vishay Siliconix** 

# Automotive N-Channel 40 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY	
V <sub>DS</sub> (V)	40
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.0060
$R_{DS(on)} (\Omega)$ at $V_{GS} = 4.5 V$	0.0073
I <sub>D</sub> (A)	60
Configuration	Single

### **FEATURES**

- TrenchFET<sup>®</sup> power MOSFET
- AEC-Q101 qualified
- 100 %  $R_q$  and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

N-Channel MOSFET

D

s



RoHS COMPLIANT HALOGEN FREE

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJ860EP-T1 (for detailed order number please see <u>www.vishay.com/doc?79771</u> )

ABSOLUTE MAXIMUM RATINGS (T	<sub>C</sub> = 25 °C, unles	s otherwise noted	)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	40	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
Continuous Drain Current	T <sub>C</sub> = 25 °C <sup>a</sup>	1	60		
Continuous Drain Current	T <sub>C</sub> = 125 °C	I <sub>D</sub>	36		
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	43	А	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	120		
Single Pulse Avalanche Current		I <sub>AS</sub>	32		
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	51	mJ	
Martin an Dan an Diastantina b	T <sub>C</sub> = 25 °C	D	48	14/	
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 125 °C	P <sub>D</sub>	16	W	
Operating Junction and Storage Temperature Ran	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C		
Soldering Recommendations (Peak Temperature)	d, e		260		

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	R <sub>thJA</sub>	70	°C/W
Junction-to-Case (Drain)		R <sub>thJC</sub>	3.1	0/10

#### Notes

a. Package limited.

- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0, I_D = 250 \ \mu A$		40	-	-	v
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	- V <sub>GS</sub> , I <sub>D</sub> = 250 μΑ	1.5	2.0	2.5	v
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, $V_{GS} = \pm 20$ V	-	-	± 100	nA
		$V_{GS} = 0 V$	= 0 V V <sub>DS</sub> = 40 V		-	1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	μA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	30	-	-	А
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A	-	0.0050	0.0060	
	-	V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 8 A	-	0.0061	0.0073	Ω
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A, T <sub>J</sub> = 125 °C	-	-	0.0099	
Dynamic <sup>b</sup>		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A, T <sub>J</sub> = 175 °C	-	-	0.0122	
Forward Transconductance <sup>b</sup>	<b>g</b> fs	V <sub>DS</sub>	= 15 V, I <sub>D</sub> = 10 A	-	78	-	S
Dynamic <sup>b</sup>					•		
Input Capacitance	C <sub>iss</sub>			-	2020	2700	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 25 V, f = 1 MHz	-	265	350	pF
Reverse Transfer Capacitance	C <sub>rss</sub>			-	110	150	
Total Gate Charge <sup>c</sup>	Qg			-	34	55	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 10 V$	$V_{DS} = 20 \text{ V}, I_D = 20 \text{ A}$	-	6	-	nC
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	7	-	
Gate Resistance	Rg	f = 1 MHz		1.3	2.7	4.5	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>				10	20	- ns
Rise Time <sup>c</sup>	t <sub>r</sub>	$\label{eq:VDD} \begin{array}{l} V_{\text{DD}} = 20 \ \text{V}, \ R_{\text{L}} = 2 \ \Omega \\ I_{\text{D}} \cong 10 \ \text{A}, \ V_{\text{GEN}} = 10 \ \text{V}, \ R_{\text{g}} = 1 \ \Omega \end{array}$		-	5	10	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	30	50	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	5	10	1
Source-Drain Diode Ratings and Charac	teristics <sup>b</sup>	·			•		
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	120	А
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> :	= 10 A, V <sub>GS</sub> = 0	-	0.8	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>			-	29	60	ns
Body diode reverse recovery charge	Q <sub>rr</sub>	1	A -1:/-14 100 A/	-	27	60	nC
Reverse recovery fall time	ta	I <sub>F</sub> = 5 /	A, di/dt = 100 A/µs	-	17	-	
Reverse recovery rise time	t <sub>b</sub>	1		-	11	-	ns
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-1.8	-4	А

#### Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

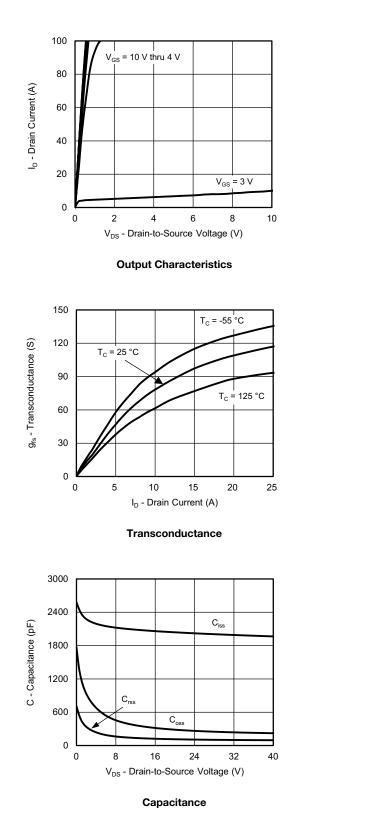
c. Independent of operating temperature.

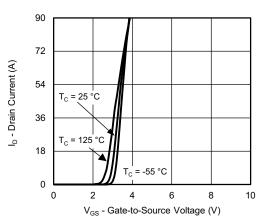
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

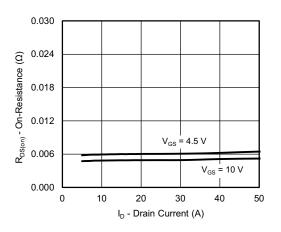


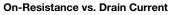
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

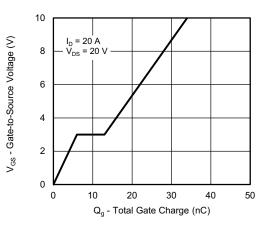




Transfer Characteristics







Gate Charge

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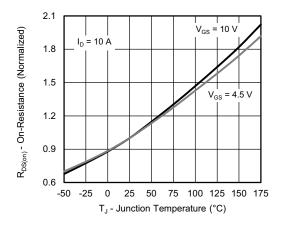
3

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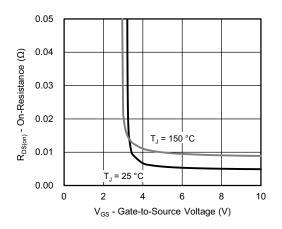
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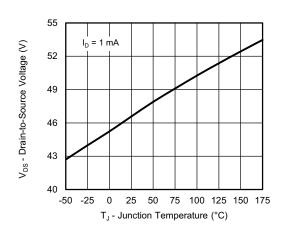
### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



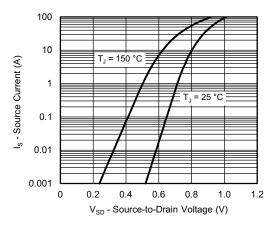
**On-Resistance vs. Junction Temperature** 



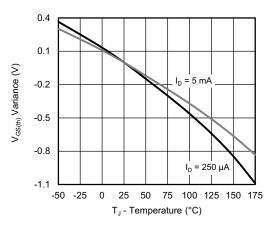
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



Source Drain Diode Forward Voltage

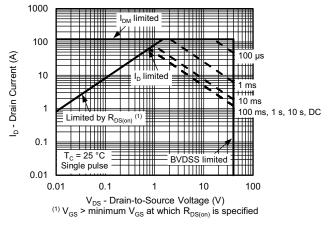


**Threshold Voltage** 

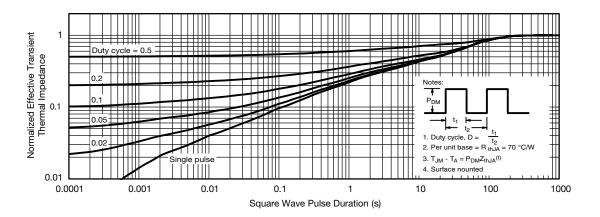
4

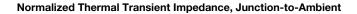


### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)









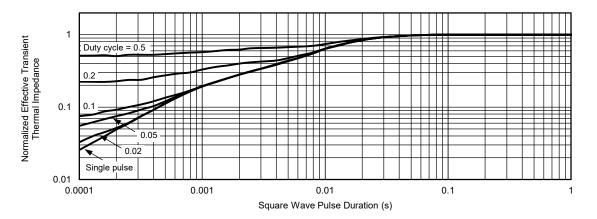


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## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

The characteristics shown in the two graphs

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- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

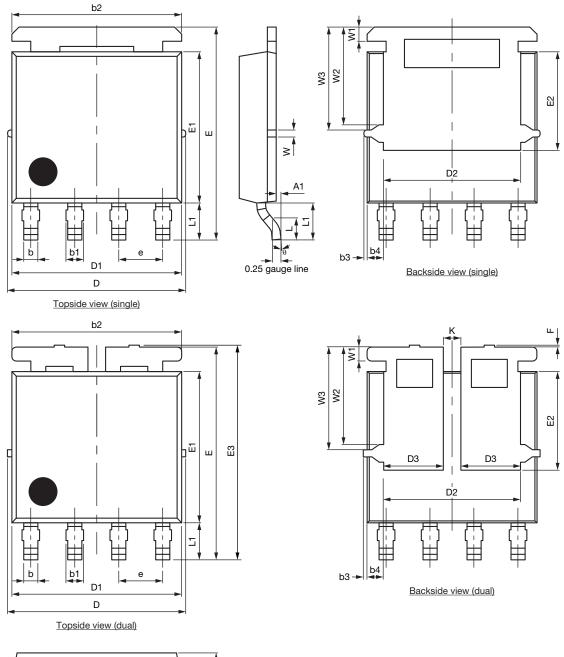
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

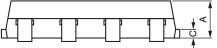
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75516.









# **Package Information**



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DIM		MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
А	1.00	1.07	1.14	0.039	0.042	0.045		
A1	0.00	-	0.127	0.00	-	0.005		
b	0.33	0.41	0.48	0.013	0.016	0.019		
b1	0.44	0.51	0.58	0.017	0.020	0.023		
b2	4.80	4.90	5.00	0.189	0.193	0.197		
b3		0.094			0.004			
b4		0.47			0.019			
С	0.20	0.25	0.30	0.008	0.010	0.012		
D	5.00	5.13	5.25	0.197	0.202	0.207		
D1	4.80	4.90	5.00	0.189	0.193	0.197		
D2	3.86	3.96	4.06	0.152	0.156	0.160		
D3	1.63	1.73	1.83	0.064	0.068	0.072		
е		1.27 BSC		0.050 BSC				
E	6.05	6.15	6.25	0.238	0.242	0.246		
E1	4.27	4.37	4.47	0.168	0.172	0.176		
E2	2.75	2.85	2.95	0.108	0.112	0.116		
E3	6.05	6.22	6.40	0.238	0.245	0.252		
F	-	-	0.15	-	-	0.006		
L	0.62	0.72	0.82	0.024	0.028	0.032		
L1	0.92	1.07	1.22	0.036	0.042	0.048		
К		0.51		0.020				
W		0.23			0.009			
W1	0.41		0.016					
W2		2.82		0.111				
W3		2.96		0.117				
θ	0°	-	10°	0°	-	10°		

Note

• Millimeters will govern



### RECOMMENDED MINIMUM PAD FOR PowerPAK<sup>®</sup> SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)

Revision: 07-Feb-12



Vishay

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