Vishay Siliconix

# N-Channel 20 V (D-S) MOSFET



PRODUCT SUMMARY	
V <sub>DS</sub> (V)	20
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.00135
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.00175
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 2.5 \text{ V}$	0.00460
Q <sub>g</sub> typ. (nC)	18.2
I <sub>D</sub> (A)	177 <sup>g</sup>
Configuration	Single

### **FEATURES**

- TrenchFET® Gen IV power MOSFET
- $\bullet$  Optimized  $Q_g,\ Q_{gd},\ and\ Q_{gd}/Q_{gs}$  ratio reduces switching related power loss

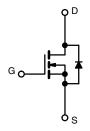
COMPLIANT HALOGEN **FREE** 

100 % R<sub>a</sub> and UIS tested

· Material categorization: for definitions of compliance please see www.vishav.com/doc?99912

### **APPLICATIONS**

- Synchronous rectification
- High power density DC/DC
- Synchronous buck converter
- · Load switching



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiR800ADP-T1-GE3

ABSOLUTE MAXIMUM RATING	<b>iS</b> (1 <sub>A</sub> = 25 °C, u	inless otherv	vise noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		$V_{DS}$	20	V	
Gate-source voltage		$V_{GS}$	+12 / -8	v	
	T <sub>C</sub> = 25 °C		177		
Continuous drain augrent (T. 150 °C)	T <sub>C</sub> = 70 °C	1 .	142		
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	l <sub>D</sub>	50.2 b, c		
	T <sub>A</sub> = 70 °C	1	40.2 <sup>b, c</sup>	^	
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	150	A	
Continuous source durin die de source t	T <sub>C</sub> = 25 °C		56.8		
Continuous source-drain diode current	T <sub>A</sub> = 25 °C	l <sub>S</sub>	4.5 <sup>b, c</sup>		
Single pulse avalanche current		I <sub>AS</sub>	20		
Single pulse avalanche energy  L = 0.1 mH		E <sub>AS</sub>	20	mJ	
	T <sub>C</sub> = 25 °C		62.5		
Maximum power dissipation	T <sub>C</sub> = 70 °C	1 5	40	w	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	5 b, c	VV	
	T <sub>A</sub> = 70 °C	7	3.2 <sup>b, c</sup>		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature) c			260		

THERMAL RESISTANCE RATING	GS				
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient b	t ≤ 10 s	R <sub>thJA</sub>	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	1.7	2	C/VV

### **Notes**

- a. Package limited
- Surface mounted on 1" x 1" FR4 board
- See solder profile (<a href="https://www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W
- $T_C = 25 \, ^{\circ}C$



# Vishay Siliconix

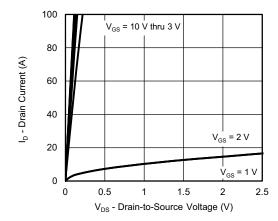
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static					•	L	
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 10 mA	-	18	-		
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-3.6	-	mv/°C	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.6	-	1.5	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = +12 / -8 \text{ V}$	-	-	100	nA	
Zana alian alla andra la consul		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	-	-	1	μA	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15		
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	Α	
	$\begin{array}{cccccccccccccccccccccccccccccccccccc$						
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	0.00145	0.00175	Ω	
Diam-source on-state resistance			-	0.00350	0.00460		
Forward transconductance <sup>a</sup>	9fs	$V_{DS} = 15 \text{ V}, I_D = 10 \text{ A}$	-	60	-	S	
Dynamic <sup>b</sup>			•		•	•	
Input capacitance	C <sub>iss</sub>		-	3415	-		
Output capacitance		$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	1290	-	рF	
Reverse transfer capacitance			-	72	-	ρı	
<del>-</del>	0	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	35.2	53		
Total gate charge	$Q_g$		-	18.2	27.5		
Gate-source charge	Q <sub>qs</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$	-	7.3	-	nC	
Gate-drain charge			-	3.6	-		
Gate resistance		f = 1 MHz	0.4	0.85	1.4	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	20	40		
Rise time		$V_{DD} = 10 \text{ V}, R_1 = 1 \Omega, I_D \cong 10 \text{ A},$	-	13	26		
Turn-off delay time	t <sub>d(off)</sub>	$V_{DD}$ = 10 V, $R_L$ = 1 $\Omega$ , $I_D \cong$ 10 A, $V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$		40	80	1	
Fall time	t <sub>f</sub>		-	10	20		
Turn-on delay time	t <sub>d(on)</sub>		-	12	24	ns	
Rise time	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_{I} = 1 \Omega, I_{D} \cong 10 \text{ A},$	-	5	10		
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	34	68		
Fall time	t <sub>f</sub>		-	6	10		
<b>Drain-Source Body Diode Characteristi</b>	cs				•	ı	
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	56.8		
Pulse diode forward current	I <sub>SM</sub>		-	-	150	Α	
Body diode voltage	V <sub>SD</sub>	$I_{S} = 5 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.73	1.1	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	32	64	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	21	42	nC	
Reverse recovery fall time	t <sub>a</sub>				-		
Reverse recovery rise time	t <sub>b</sub>		-	16	-	ns	

### Notes

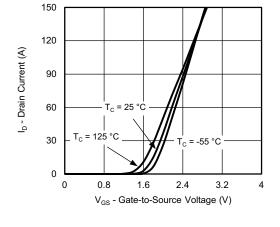
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

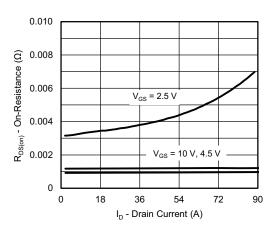




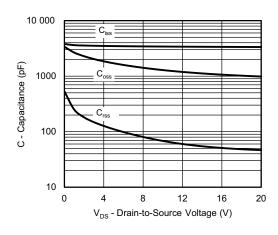
### **Output Characteristics**



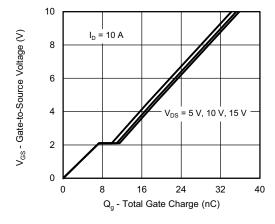
**Transfer Characteristics** 



On-Resistance vs. Drain Current and Gate Voltage

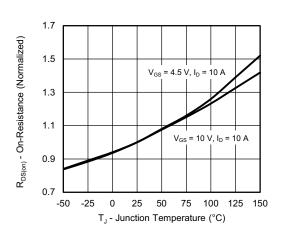


Capacitance

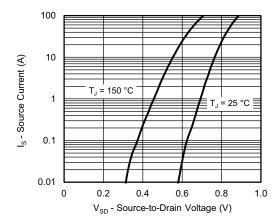


**Gate Charge** 

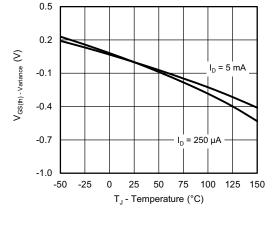
On-Resistance vs. Junction Temperature



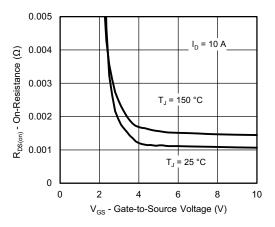




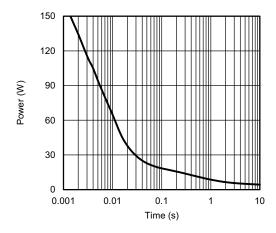
Source-Drain Diode Forward Voltage



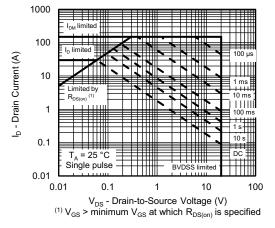
**Threshold Voltage** 



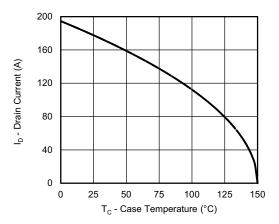
On-Resistance vs. Gate-to-Source Voltage



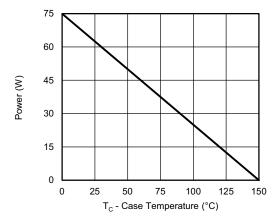
Single Pulse Power, Junction-to-Ambient

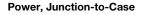


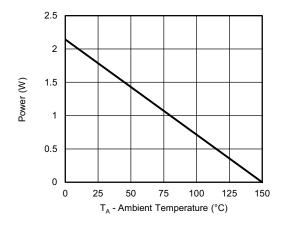
Safe Operating Area, Junction-to-Ambient



### Current Derating a



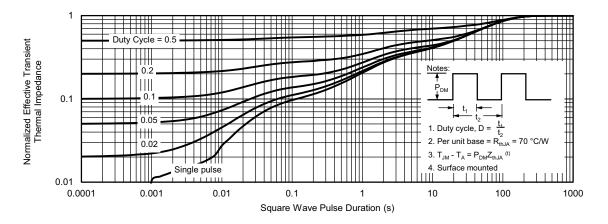




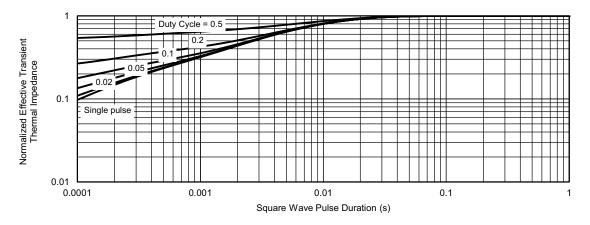
Power, Junction-to-Ambient

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





### Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?79335">www.vishay.com/ppg?79335</a>.



DWG: 5881

PowerPAK® SO-8, (Single/Dual)

# Notes 1. Inch will govern. 2 Dimensions exclusive of mold gate burrs.

3. Dimensions exclusive of mold flash and cutting burrs.

Backside View of Dual Pad

DIM.	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX	
Α	0.97	1.04	1.12	0.038	0.041	0.044	
A1		-	0.05	0	-	0.002	
b	0.33	0.41	0.51	0.013	0.016	0.020	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	5.05	5.15	5.26	0.199	0.203	0.20	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.56	3.76	3.91	0.140	0.148	0.15	
D3	1.32	1.50	1.68	0.052	0.059	0.06	
D4		0.57 typ. 0.0225 typ.					
D5		3.98 typ.		0.157 typ.			
Е	6.05	6.15	6.25	0.238	0.242	0.24	
E1	5.79	5.89	5.99	0.228	0.232	0.23	
E2	3.48	3.66	3.84	0.137	0.144	0.15	
E3	3.68	3.78	3.91	0.145	0.149	0.15	
E4		0.75 typ.			0.030 typ.		
е		1.27 BSC			0.050 BSC		
K		1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-	
Н	0.51	0.61	0.71	0.020	0.024	0.02	
L	0.51	0.61	0.71	0.020	0.024	0.02	
L1	0.06	0.13	0.20	0.002	0.005	0.00	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.01	
М	0.125 typ.			0.005 typ.			

Revison: 13-Feb-17 1 Document Number: 71655



### RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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