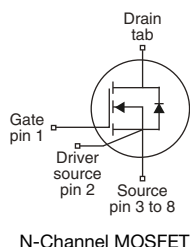
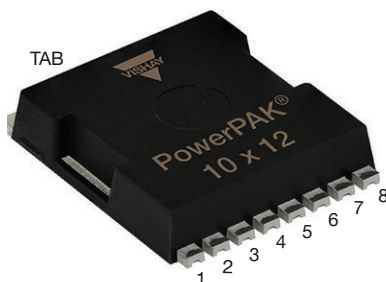


EF Series Power MOSFET With Fast Body Diode

PowerPAK® 10 x 12


FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low effective capacitance ($C_{o(er)}$)
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	0.061
Q_g max. (nC)	72	
Q_{gs} (nC)	20	
Q_{gd} (nC)	11	
Configuration	Single	

ORDERING INFORMATION

Package	PowerPAK 10 x 12
Lead (Pb)-free and halogen-free	SiHK075N60EF-T1GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	600	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current ($T_J = 150\text{ }^{\circ}\text{C}$)	V_{GS} at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	33	A
		$T_C = 100\text{ }^{\circ}\text{C}$		21	
Pulsed drain current ^a			I_{DM}	97	
Linear derating factor				1.54	W/ $^{\circ}\text{C}$
Single pulse avalanche energy ^b			E_{AS}	226	mJ
Maximum power dissipation			P_D	192	W
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	$^{\circ}\text{C}$
Drain-source voltage slope		$T_J = 125\text{ }^{\circ}\text{C}$	dv/dt	100	V/ns
Reverse diode dv/dt ^d				50	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4.0$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, di/dt = 100 A/ μ s, starting $T_J = 25$ °C

**THERMAL RESISTANCE RATINGS**

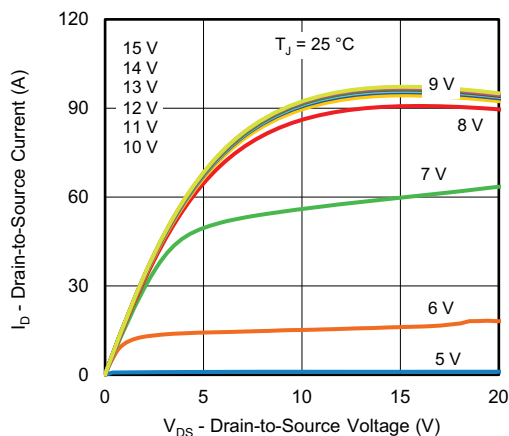
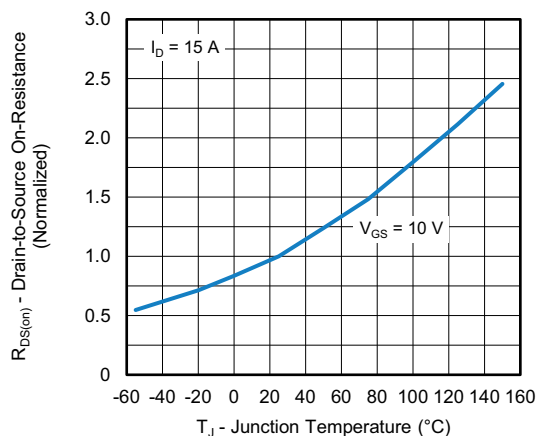
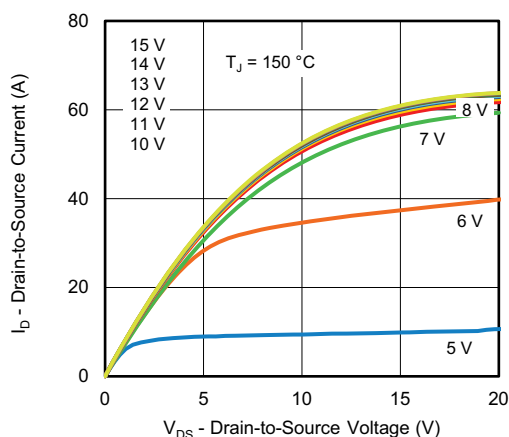
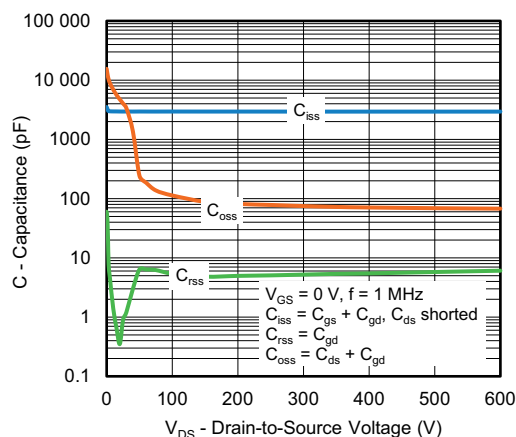
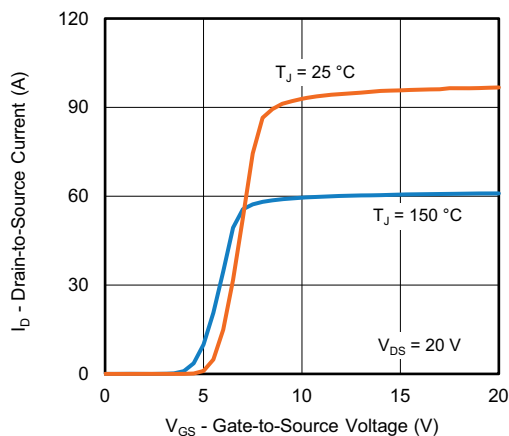
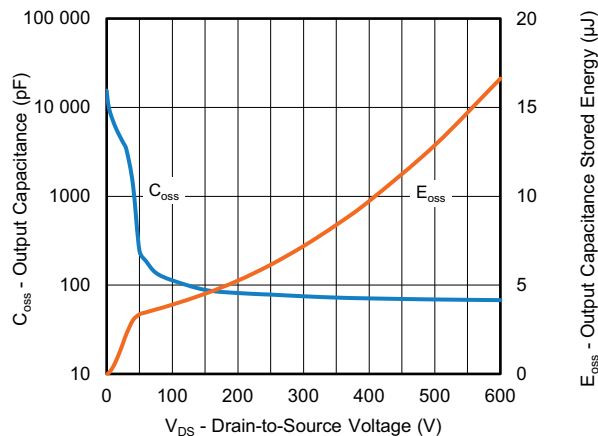
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	50 °C	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.65	

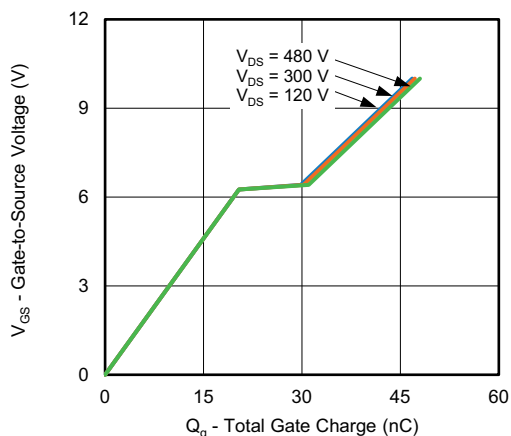
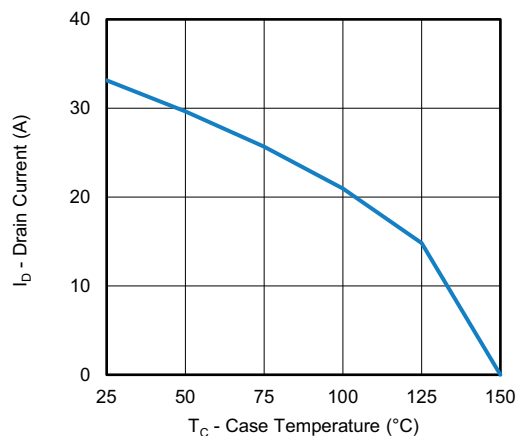
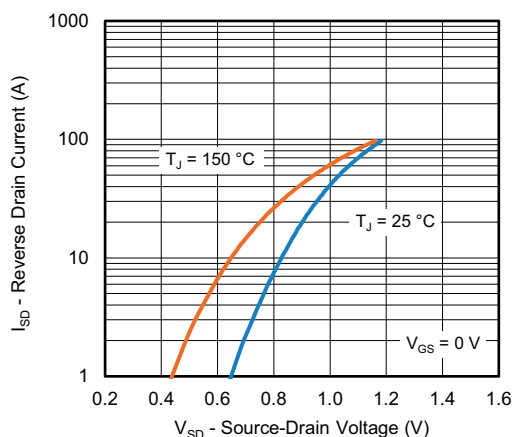
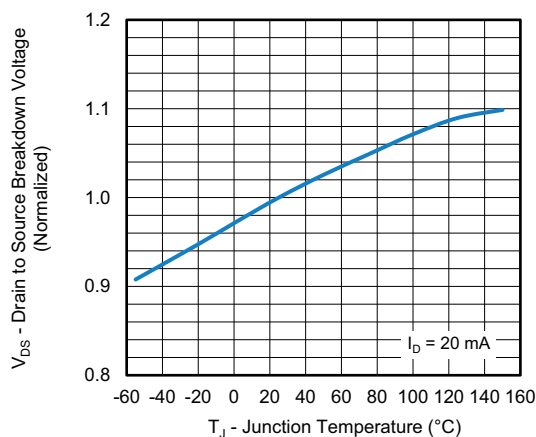
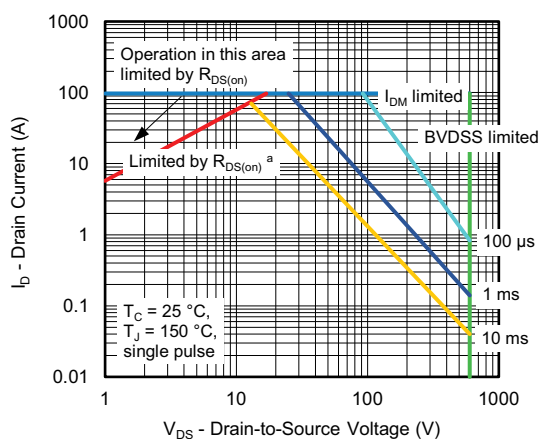
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		600	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1\text{ mA}$		-	0.62	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	± 1	μA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$		-	-	2	mA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}$	-	0.061	0.071	Ω
Forward transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 15\text{ A}$		-	4.5	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$		-	2954	-	pF
Output capacitance	C_{oss}			-	113	-	
Reverse transfer capacitance	C_{rss}			-	5	-	
Effective output capacitance, energy related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 400\text{ V}$, $V_{GS} = 0\text{ V}$		-	122	-	pF
Effective output capacitance, time related ^b	$C_{o(tr)}$			-	644	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}$, $V_{DS} = 480\text{ V}$	-	48	72	nC
Gate-source charge	Q_{gs}			-	20	-	
Gate-drain charge	Q_{gd}			-	11	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 480\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$		-	30	60	ns
Rise time	t_r			-	33	66	
Turn-off delay time	$t_{d(off)}$			-	46	92	
Fall time	t_f			-	26	52	
Gate input resistance	R_g	$f = 1\text{ MHz}$		0.3	0.7	1.4	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	33	A
Pulsed diode forward current	I_{SM}			-	-	97	
Diode forward voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 15\text{ A}$, $V_{GS} = 0\text{ V}$		-	-	1.2	V
Reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = I_S = 15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 400\text{ V}$		-	111	222	ns
Reverse recovery charge	Q_{rr}			-	0.7	1.4	μC
Reverse recovery current	I_{RRM}			-	12	-	A

Notes

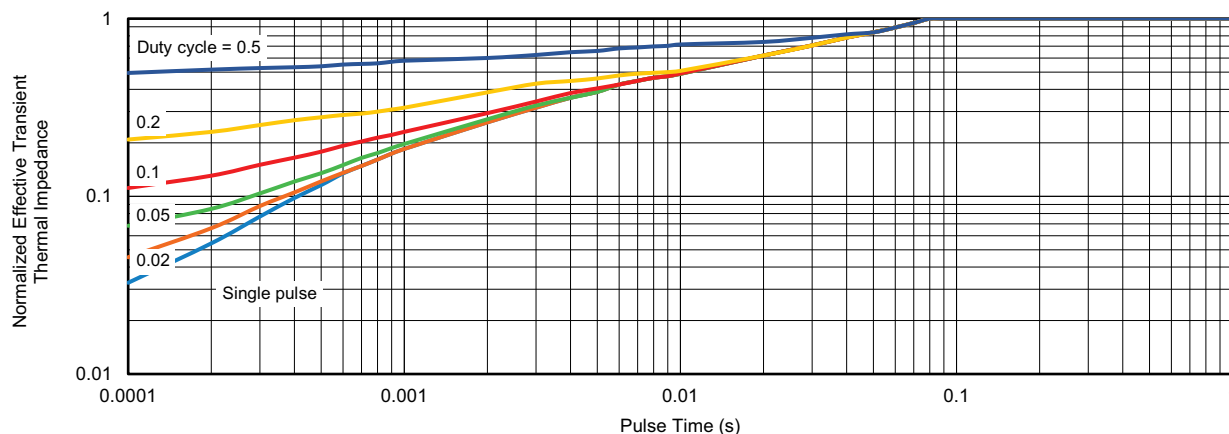
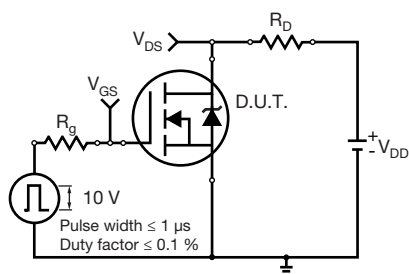
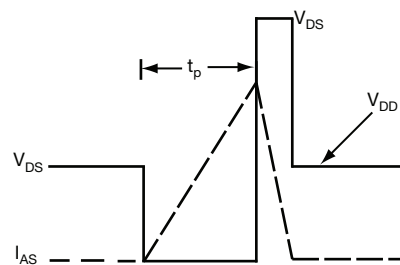
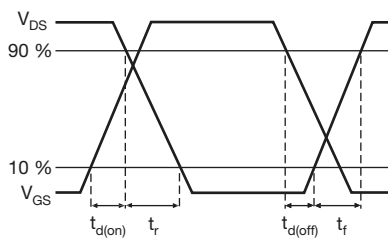
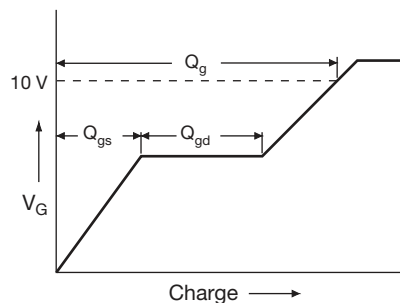
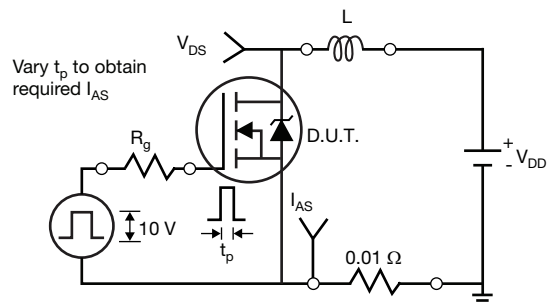
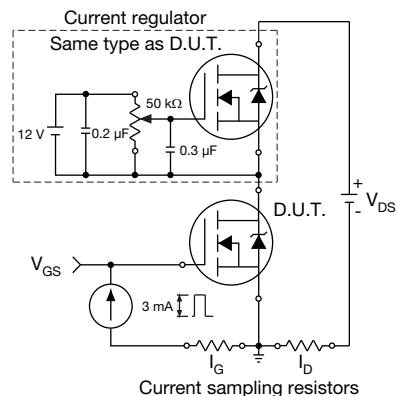
- e. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 V to 400 V
f. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to 400 V
g. When mounted on 1" x 1" FR4 board

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Temperature vs. Drain-to-Source Voltage

Fig. 9 - Maximum Safe Operating Area

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

Fig. 13 - Switching Time Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

Fig. 14 - Switching Time Waveforms

Fig. 17 - Basic Gate Charge Waveform

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Gate Charge Test Circuit

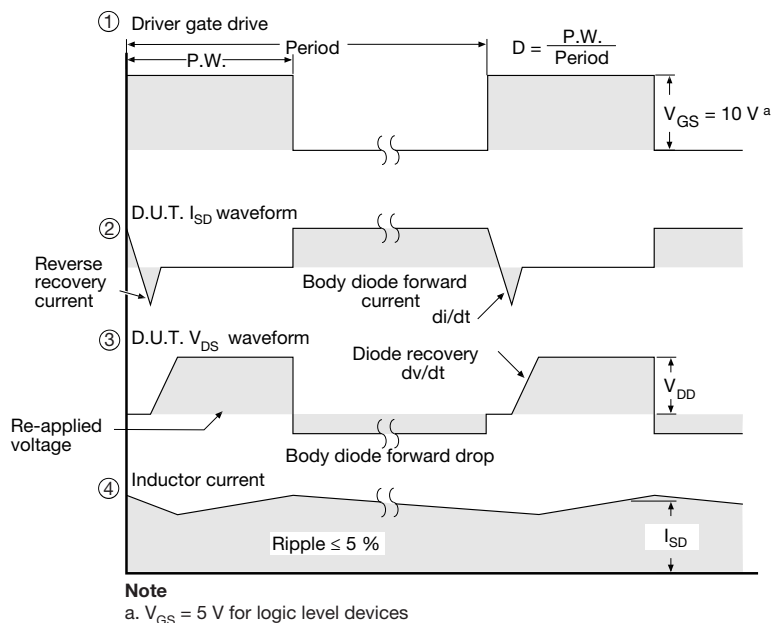
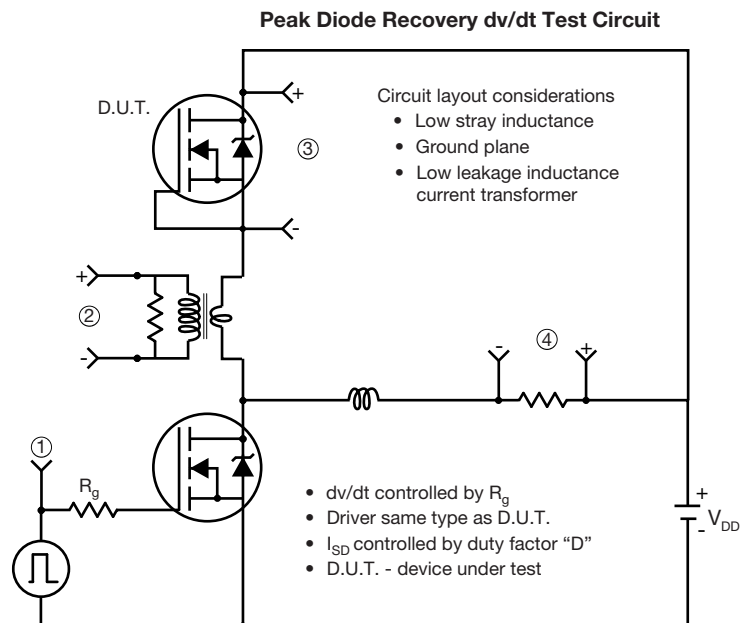


Fig. 19 - For N-Channel

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