

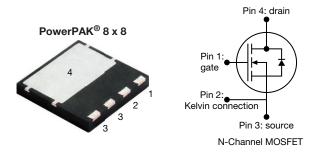
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Vishay Siliconix

HALOGEN

FREE GREEN

EF Series Power MOSFET With Fast Body Diode



PRODUCT SUMMARY				
V _{DS} (V) at T _J max.	650			
R _{DS(on)} typ. (Ω) at 25 °C	V _{GS} = 10 V 0.168			
Q _g max. (nC)	32			
Q _{gs} (nC)	7			
Q _{gd} (nC)	7	7		
Configuration	Single			

FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) R_{on} x Q_g
- Low effective capacitance (Co(er))
- · Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

ORDERING INFORMATION	
Package	PowerPAK 8 x 8
Lead (Pb)-free and halogen-free	SiHH186N60EF-T1GE3

ABSOLUTE MAXIMUM RATINGS (T	_C = 25 °C, unl	ess otherwis	se noted)		
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	600	V
Gate-source voltage			V_{GS}	± 30]
Continuous dusin surrent (T. 150 °C)	V at 10 V	T _C = 25 °C	- I _D	16	A
Continuous drain current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 100 °C		10	
Pulsed drain current a			I _{DM}	43	
Linear derating factor				0.9	W/°C
Single pulse avalanche energy b			E _{AS}	24	mJ
Maximum power dissipation			P_{D}	114	W
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C
Drain-source voltage slope $T_J = 125 ^{\circ}\text{C}$			dv/dt	100	- V/ns
Reverse diode dv/dt ^c				50	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b. V_{DD} = 120 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω , I_{AS} = 1.3 A
- c. $I_{SD} \le I_D$, di/dt = 700 A/ μ s, starting T_J = 25 °C



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THERMAL RESISTANCE RATINGS						
PARAMETER SYMBOL TYP. MAX. UNIT						
Maximum junction-to-ambient	R_{thJA}	42	55	°C/W		
Maximum junction-to-case (drain)	R_{thJC}	0.76	1.10	G/ VV		

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static		•					
Drain-source breakdown voltage	V _{DS}	V _{GS} =	= 0 V, I _D = 250 μA	600	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I _D = 1 mA	-	0.69	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} =	- V _{GS} , I _D = 250 μA	3.0	-	5.0	V
Onto anima lankana		,	V _{GS} = ± 20 V	-	-	± 100	nA
Gate-source leakage	I _{GSS}	,	$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μΑ
7		V _{DS} =	V _{DS} = 480 V, V _{GS} = 0 V		-	1	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 480 V	', V _{GS} = 0 V, T _J = 125 °C	-	-	2	mA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 9.5 A	-	0.168	0.193	Ω
Forward transconductance ^a	9 _{fs}	V _{DS} :	= 20 V, I _D = 9.5 A	-	5.4	-	S
Dynamic							
Input capacitance	C _{iss}		V _{GS} = 0 V,	-	1081		
Output capacitance	C _{oss}	1	$V_{DS} = 100 V$	-	52	-	
Reverse transfer capacitance	C _{rss}	1	f = 1 MHz	-	5	-	
Effective output capacitance, energy related ^a	C _{o(er)}	V 0.	V to 480 V, V _{GS} = 0 V	-	40	-	pF
Effective output capacitance, time related ^b	$C_{o(tr)}$	V _{DS} = 0	v to 460 v, v _{GS} = 0 v	-	247	-	
Total gate charge	Qg			-	21	32	
Gate-source charge	Q _{gs}	V _{GS} = 10 V	$I_D = 9.5 \text{ A}, V_{DS} = 480 \text{ V}$	-	7	-	nC
Gate-drain charge	Q_{gd}			-	7	-	
Turn-on delay time	t _{d(on)}			-	14	28	
Rise time	t _r	V _{DD} = 480 V, I _D = 9.5 A,		-	23	46	no
Turn-off delay time	t _{d(off)}	V _{GS} =	= 10 V, $R_g = 9.1 \Omega$	-	25	50	ns
Fall time	t _f			-	16	32	
Gate input resistance	R _g		f = 1 MHz	0.3	0.7	1.4	Ω
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	I _S	showing the	MOSFET symbol showing the		-	16	
Pulsed diode forward current	I _{SM}	integral revers p - n junction		-	-	43	A
Diode forward voltage	V _{SD}	T _J = 25 °C	C, I _S = 9.5 A, V _{GS} = 0 V	-	-	1.2	V
Reverse recovery time	t _{rr}			-	111	222	ns
Reverse recovery charge	Q _{rr}		5 °C, I _F = I _S = 9.5 A,	-	0.6	1.2	μC
Reverse recovery current	I _{RRM}	u/ut = 1	$00 \text{ A/}\mu\text{s}, V_{\text{R}} = 400 \text{ V}$	-	10	-	Α

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

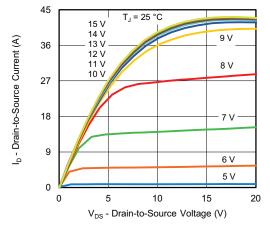


Fig. 1 - Typical Output Characteristics

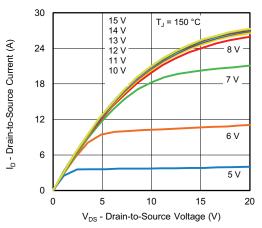


Fig. 2 - Typical Output Characteristics

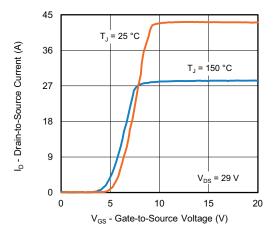


Fig. 3 - Typical Transfer Characteristics

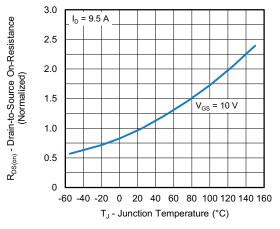


Fig. 4 - Normalized On-Resistance vs. Temperature

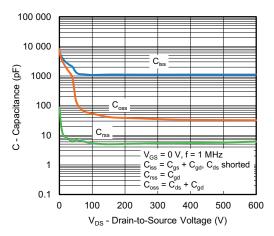


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

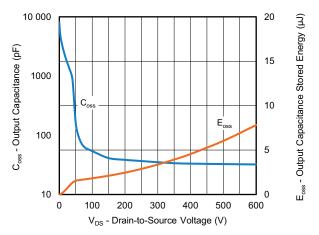


Fig. 6 - Coss and Eoss vs. VDS



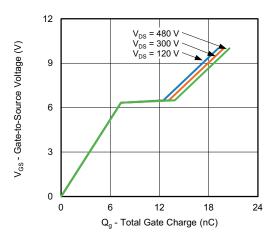


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

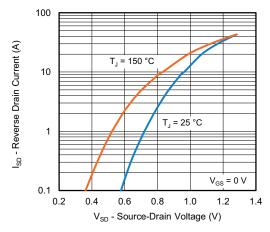


Fig. 8 - Typical Source-Drain Diode Forward Voltage

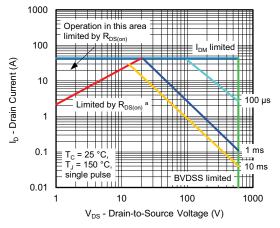


Fig. 9 - Maximum Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

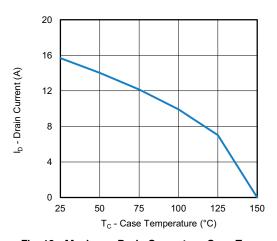


Fig. 10 - Maximum Drain Current vs. Case Temperature

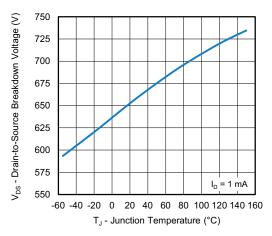


Fig. 11 - Temperature vs. Drain-to-Source Voltage



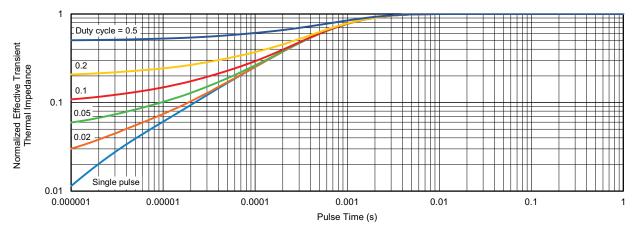


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

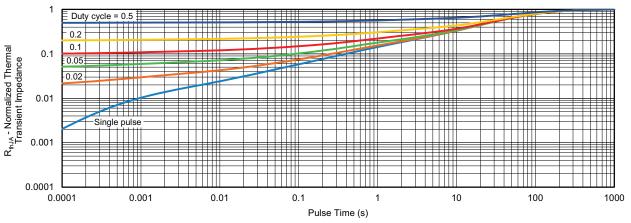


Fig. 13 - Normalized Transient Thermal Impedance, Junction-to-Ambient

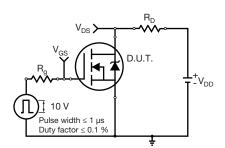


Fig. 14 - Switching Time Test Circuit

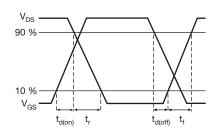


Fig. 15 - Switching Time Waveforms

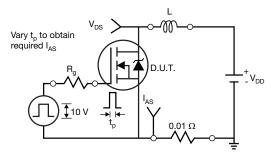


Fig. 16 - Unclamped Inductive Test Circuit

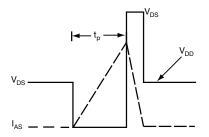


Fig. 17 - Unclamped Inductive Waveforms

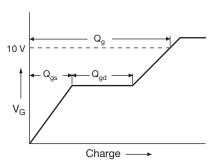


Fig. 18 - Basic Gate Charge Waveform

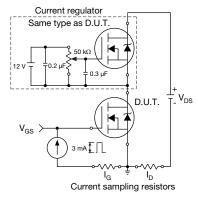
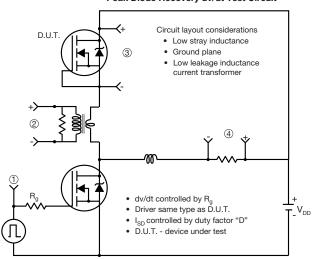


Fig. 19 - Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



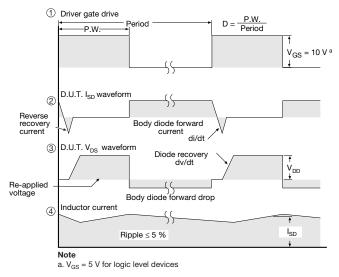


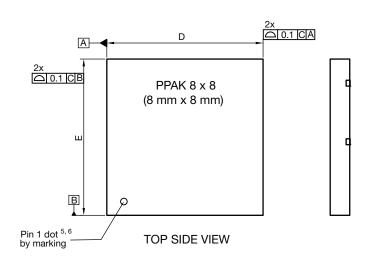
Fig. 20 - For N-Channel

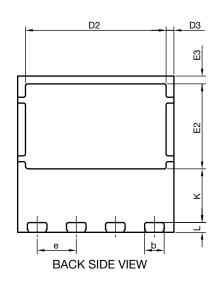
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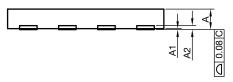


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PowerPAK® 8 x 8 Case Outline







DIM.	MILLIMETERS			INCHES			
DIIVI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.95	1.00	1.05	0.037	0.039	0.041	
A1	0.00	-	0.05	0.000	-	0.002	
A2	020 ref.			0.008 ref.			
b	0.95	1.00	1.05	0.037	0.039	0.041	
D	7.90	8.00	8.10	0.311	0.315	0.319	
D2	7.10	7.20	7.30	0.280	0.283	0.287	
D3	0.40 BSC			0.016 BSC			
е	2.00 BSC		0.079 BSC				
Е	7.90	8.00	8.10	0.311	0.315	0.319	
E2	4.30	4.35	4.40	0.169	0.171	0.173	
E3		0.40 BSC			0.016 BSC		
K	2.75 BSC		0.108 BSC				
L	0.45	0.50	0.55	0.018	0.020	0.022	
N ⁽³⁾	8				8		

Notes

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5 M 1994
- (3) N is the number of terminals
- (4) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (5) Exact shape and size of this feature is optional

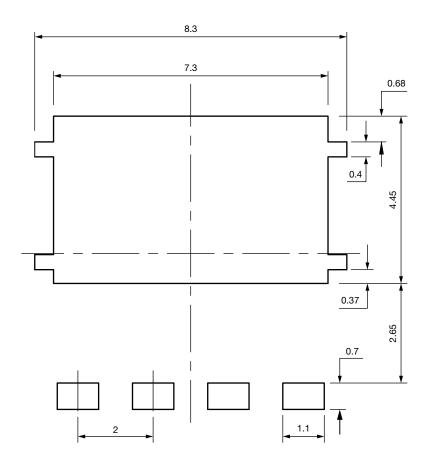
ECN: E20-0518-Rev. B, 28-Sep-2020

DWG: 6041

Revision: 28-Sep-2020 1 Document Number: 67859



Recommended Minimum PADs for PowerPAK® 8 mm x 8 mm



Dimensions in millimeters



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