Vishay Siliconix

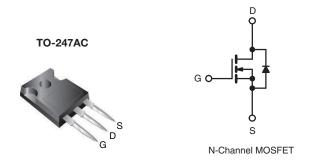
RoHS

COMPLIANT

HALOGEN FREE

E Series Power MOSFET

PRODUCT SUMMARY			
V _{DS} (V) at T _J max.	os (V) at T _J max. 650		
R _{DS(on)} max. at 25 °C (Ω)	V _{GS} = 10 V 0.125		
Q _g max. (nC)	130		
Q _{gs} (nC)	15		
Q _{gd} (nC)	39		
Configuration	Single		



FEATURES

- Low figure-of-merit (FOM) Ron x Qg
- Low input capacitance (Ciss)
- Reduced switching and conduction losses
- Ultra low gate charge (Q_q)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
 - LED lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
- · Battery chargers
- Renewable energy
 - Solar (PV inverters)

ORDERING INFORMATION			
Package	TO-247AC		
Lead (Pb)-free	SiHG30N60E-E3		
Lead (Pb)-free and Halogen-free	SiHG30N60E-GE3		

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	600	V
Gate-Source Voltage			V_{GS}	± 30	V
Continuous Drain Current (T _{.1} = 150 °C)	\/ at 10 \/	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$		29	
Continuous Drain Current (1) = 150 °C)	V _{GS} at 10 V	T _C = 100 °C	I _D	18	Α
Pulsed Drain Current ^a			I _{DM}	65	
Linear Derating Factor				2	W/°C
Single Pulse Avalanche Energy b			E _{AS}	690	mJ
Maximum Power Dissipation			P_{D}	250	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Drain-Source Voltage Slope V _{DS} = 0 V to 80 % V _{DS}		-15.77-11	70	V/ns	
Reverse Diode dV/dt ^d			dV/dt	18	V/fis
Soldering Recommendations (Peak Temperature) c	for	10 s		300	°C

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, L = 28.2 mH, $R_g = 25$ Ω , $I_{AS} = 7$ A.
- c. 1.6 mm from case.
- d. $I_{SD} \le I_D$, $dI/dt = 100 \text{ A/}\mu\text{s}$, starting $T_J = 25 \,^{\circ}\text{C}$.



Vishay Siliconix

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.5	G/ VV

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static				•	•	l .	
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		600	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I _D = 250 μA	-	0.64	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} =	- V _{GS} , I _D = 250 μA	2.0	2.8	4.0	V
Octo Course Legland		,	V _{GS} = ± 20 V	-	-	± 100	nA
Gate-Source Leakage	I_{GSS}	,	$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μΑ
Zava Cata Valtaga Dvain Cuwant		V _{DS} =	= 600 V, V _{GS} = 0 V	-	-	1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600 V	', V _{GS} = 0 V, T _J = 150 °C	-	-	100	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 15 A	-	0.104	0.125	Ω
Forward Transconductance a	9 _{fs}	V _{DS}	_S = 8 V, I _D = 3 A	-	5.4	-	S
Dynamic							
Input Capacitance	C _{iss}		$V_{GS} = 0 V$,	-	2600	-	
Output Capacitance	C_{oss}		V _{DS} = 100 V,	-	138	-	1
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz		-	3	-	_
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	- V _{DS} = 0 V to 480 V, V _{GS} = 0 V		-	98	-	pF
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	346	-	
Total Gate Charge	Qg			-	85	130	
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$I_D = 15 \text{ A}, V_{DS} = 480 \text{ V}$	-	15	-	nC
Gate-Drain Charge	Q_{gd}	1 [-	39	-	
Turn-On Delay Time	t _{d(on)}		•	-	19	40	
Rise Time	t _r		= 380 V, I _D = 15 A,	-	32	65	ns
Turn-Off Delay Time	t _{d(off)}	V _{GS} =	= 10 V, R_g = 4.7 Ω	-	63	95	115
Fall Time	t _f			-	36	75	
Gate Input Resistance	R_g	f = 1	MHz, open drain	-	0.63	-	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	29	
Pulsed Diode Forward Current	I _{SM}			-	-	65	- A
Diode Forward Voltage	V _{SD}	T _J = 25 °C	C, I _S = 15 A, V _{GS} = 0 V	-	-	1.3	V
Body Diode Reverse Recovery Time	t _{rr}			-	402	605	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 28$	5 °C, I _F = I _S = 15 A, 100 A/μs ^{, V} _R = 20 V	-	7	15	μC
Reverse Recovery Current	I _{RRM}	αι/αι = 100 A/μs ^{, -} R = 20 V		-	32	65	Α

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

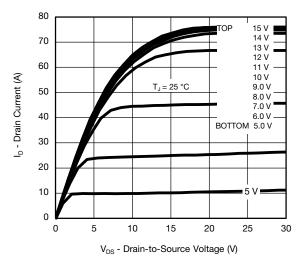


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

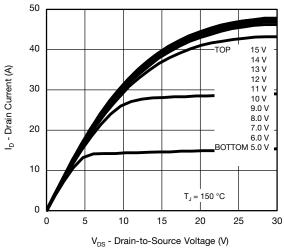


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

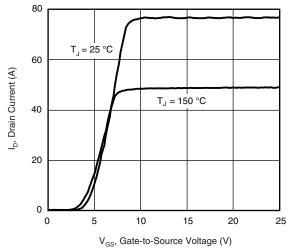


Fig. 3 - Typical Transfer Characteristics

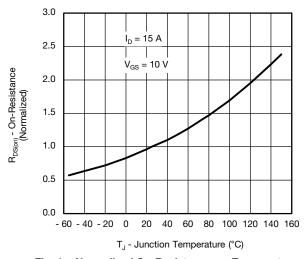


Fig. 4 - Normalized On-Resistance vs. Temperature

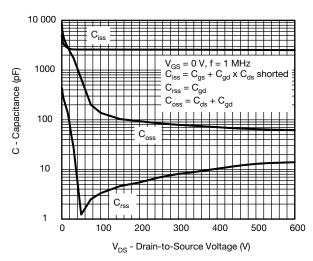


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

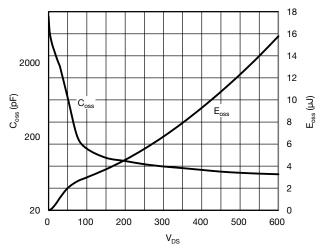


Fig. 6 - Coss and Eoss vs. VDS



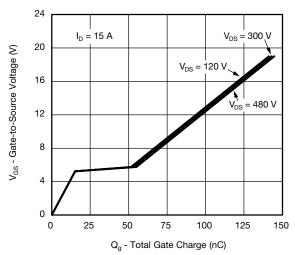


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

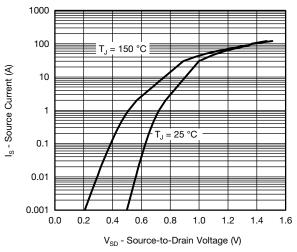


Fig. 8 - Typical Source-Drain Diode Forward Voltage

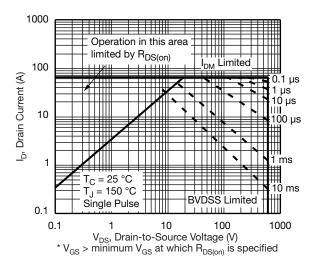


Fig. 9 - Maximum Safe Operating Area

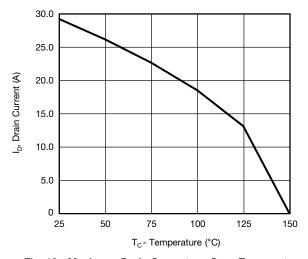


Fig. 10 - Maximum Drain Current vs. Case Temperature

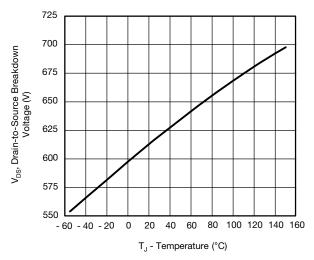
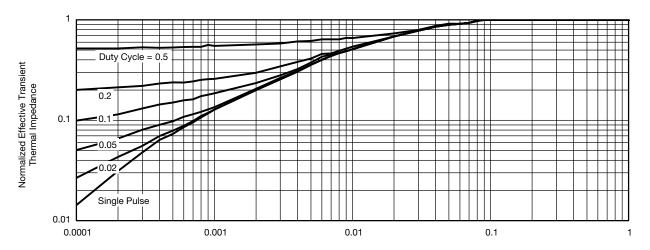
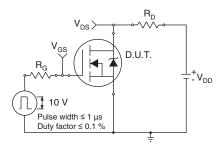


Fig. 11 - Temperature vs. Drain-to-Source Voltage





Square Wave Pulse Duration (s)
Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case



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Fig. 13 - Switching Time Test Circuit

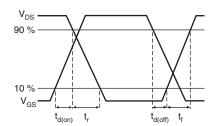


Fig. 14 - Switching Time Waveforms

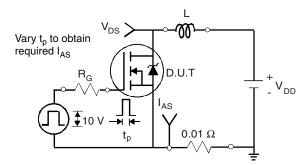


Fig. 15 - Unclamped Inductive Test Circuit

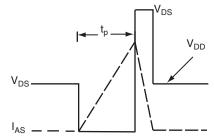


Fig. 16 - Unclamped Inductive Waveforms

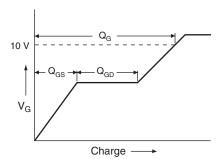


Fig. 17 - Basic Gate Charge Waveform

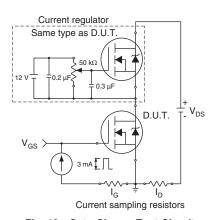
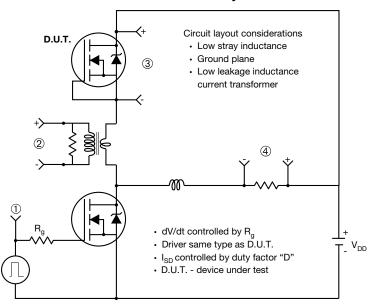


Fig. 18 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



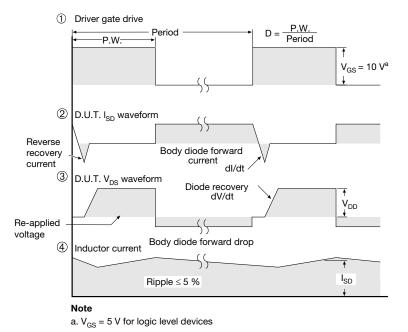


Fig. 19 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91455.



TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9







Section C--C,D-D,E-E

	MILLIMETERS				
DIM.	MIN.	NOM.	MAX.	NOTES	
Α	4.83	5.02	5.21		
A1	2.29	2.41	2.55		
A2	1.17	1.27	1.37		
b	1.12	1.20	1.33		
b1	1.12	1.20	1.28		
b2	1.91	2.00	2.39	6	
b3	1.91	2.00	2.34		
b4	2.87	3.00	3.22	6, 8	
b5	2.87	3.00	3.18		
С	0.40	0.50	0.60	6	
c1	0.40	0.50	0.56		
D	20.40	20.55	20.70	4	

		MILLIMETERS	S		
DIM.	MIN.	NOM.	MAX.	NOTES	
D1	16.46	16.76	17.06	5	
D2	0.56	0.66	0.76		
E	15.50	15.70	15.87	4	
E1	13.46	14.02	14.16	5	
E2	4.52	4.91	5.49	3	
е		5.46 BSC			
L	14.90	15.15	15.40		
L1	3.96	4.06	4.16	6	
ØΡ	3.56	3.61	3.65	7	
Ø P1	7.19 ref.				
Q	5.31	5.50	5.69		
S	5.51 BSC				

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- $^{(7)}$ Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



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VERSION 2: FACILITY CODE = Y



	MILLIM		
DIM.	MIN.	MAX.	NOTES
Α	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
С	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

	MILLIN		
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
Е	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.2	254	
L	14.20	16.25	
L1	3.71	4.29	
ØР	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



	MILLIMETERS		
DIM.	MIN.	MAX.	
Α	4.65	5.31	
A1	2.21	2.59	
A2	1.17	1.37	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.65	2.39	
b3	1.65	2.34	
b4	2.59	3.43	
b5	2.59	3.38	
С	0.38	0.89	
c1	0.38	0.84	
D	19.71	20.70	
D1	13.08	-	

	MILLIMETERS		
DIM.	MIN.	MAX.	
D2	0.51	1.35	
E	15.29	15.87	
E1	13.46	-	
е	5.46 BSC		
k	0.254		
L	14.20	16.10	
L1	3.71	4.29	
N	7.62	BSC	
Р	3.56	3.66	
P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

ECN: E22-0452-Rev. G, 31-Oct-2022

DWG: 5971

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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