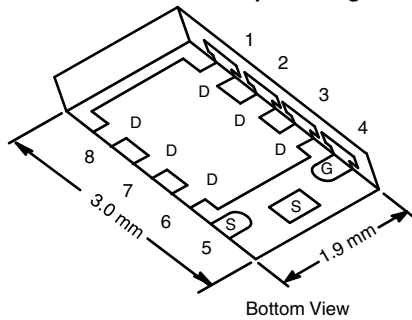


## N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) Max.	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
20	0.0100 at V <sub>GS</sub> = 4.5 V	25	16.6 nC
	0.0115 at V <sub>GS</sub> = 2.5 V	25	
	0.0135 at V <sub>GS</sub> = 1.8 V	25	

PowerPAK ChipFET Single



**Ordering Information:**  
Si5442DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- Thermally Enhanced PowerPAK<sup>®</sup> ChipFET<sup>®</sup> Package
  - Small Footprint Area
  - Low On-Resistance
  - Thin 0.8 mm Profile
- 100% R<sub>g</sub> Tested
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

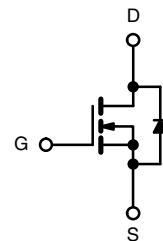
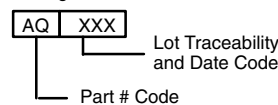


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Load Switch, PA Switch, and for Portable Applications
- Point-of-Load
- DC/DC Converters
- Power Management

#### Marking Code



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	± 8	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	25 <sup>a</sup>
		T <sub>C</sub> = 70 °C	25 <sup>a</sup>
		T <sub>A</sub> = 25 °C	12.4 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	9.9 <sup>b, c</sup>
Pulsed Drain Current (t = 300 μs)	I <sub>DM</sub>	60	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	2.6 <sup>b, c</sup>
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	31
		T <sub>C</sub> = 70 °C	20
		T <sub>A</sub> = 25 °C	3.1 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	2 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 s	R <sub>thJA</sub>	34	40	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	3	4	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile ([www.vishay.com/doc?27325Z](http://www.vishay.com/doc?27325Z)). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 90 °C/W.

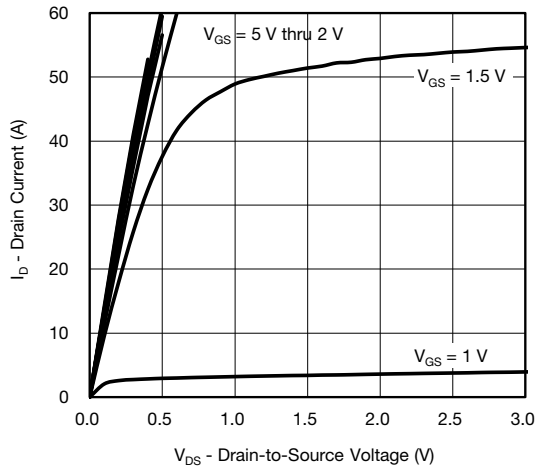
SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		21		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.4		0.9	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	20			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		0.0080	0.0100	$\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 7\text{ A}$		0.0090	0.0115	
		$V_{GS} = 1.8\text{ V}, I_D = 4\text{ A}$		0.0100	0.0135	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 8\text{ A}$		65		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1700		$\mu\text{F}$
Output Capacitance	$C_{oss}$			280		
Reverse Transfer Capacitance	$C_{rss}$			115		
Total Gate Charge	$Q_g$	$V_{DS} = 10\text{ V}, V_{GS} = 8\text{ V}, I_D = 15\text{ A}$		29	45	nC
			$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$		16.6	
$Q_{gs}$		1.9				
$Q_{gd}$		2				
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.28	1.4	2.8	$\Omega$
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		10	20	ns
Rise Time	$t_r$			15	30	
Turn-Off Delay Time	$t_{d(off)}$			35	70	
Fall Time	$t_f$			10	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 8\text{ V}, R_g = 1\text{ }\Omega$		10	20	
Rise Time	$t_r$			10	20	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	$t_f$			10	20	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			25	A
Pulse Diode Forward Current	$I_{SM}$				60	
Body Diode Voltage	$V_{SD}$	$I_S = 10\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		20	40	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			10	20	nC
Reverse Recovery Fall Time	$t_a$			11		ns
Reverse Recovery Rise Time	$t_b$			9		

## Notes:

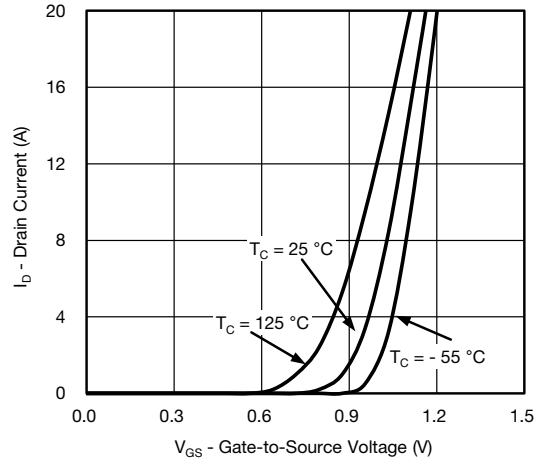
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

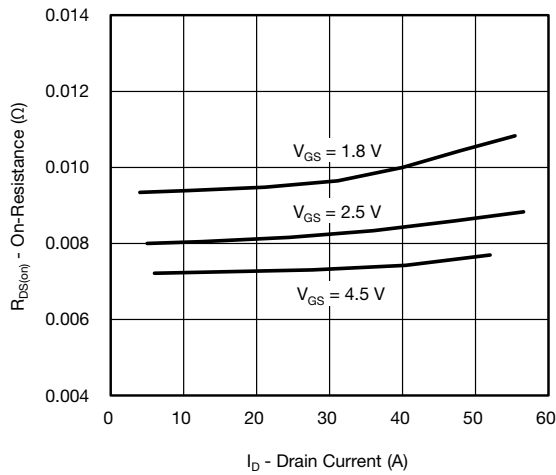
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



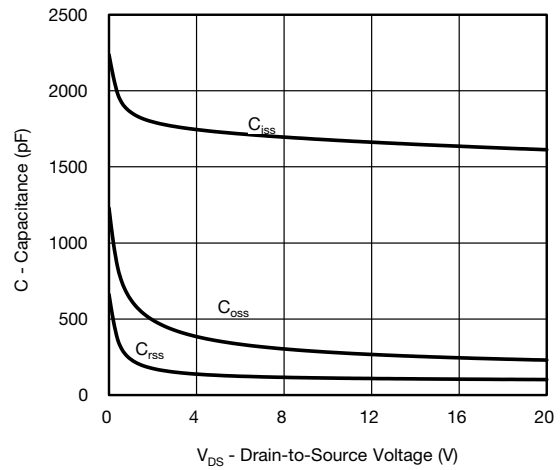
**Output Characteristics**



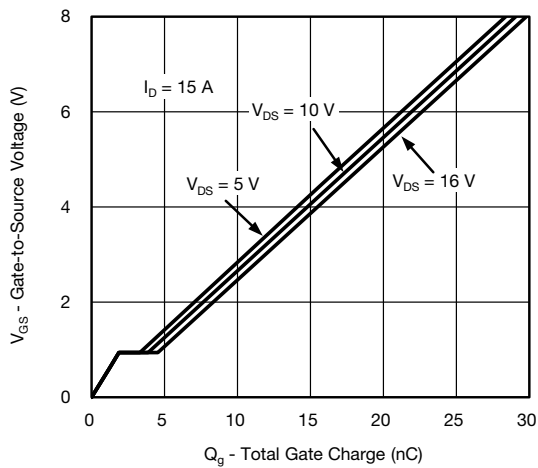
**Transfer Characteristics**



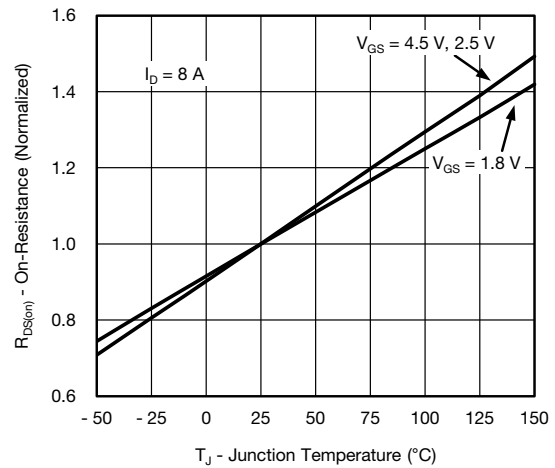
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

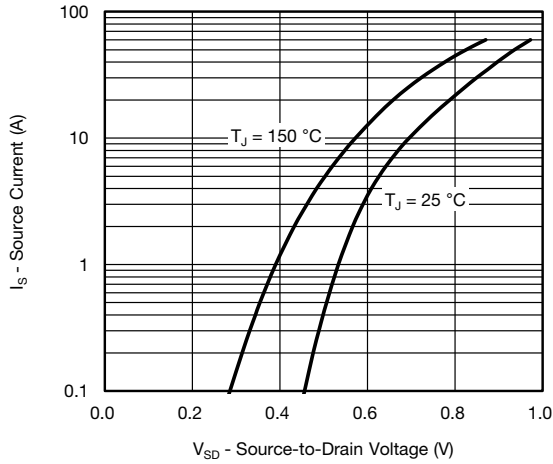


**Gate Charge**

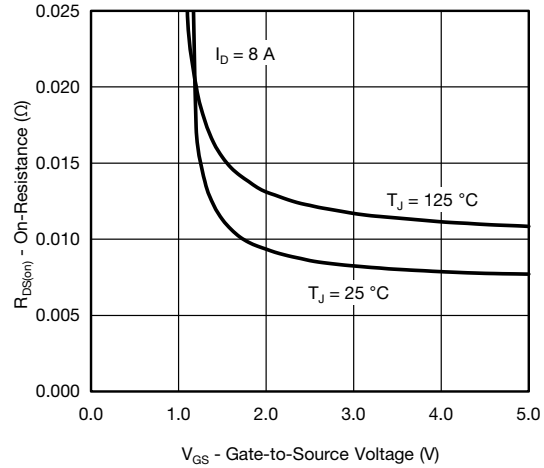


**On-Resistance vs. Junction Temperature**

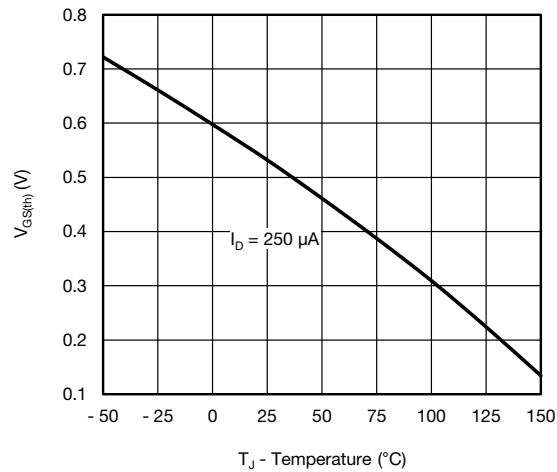
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



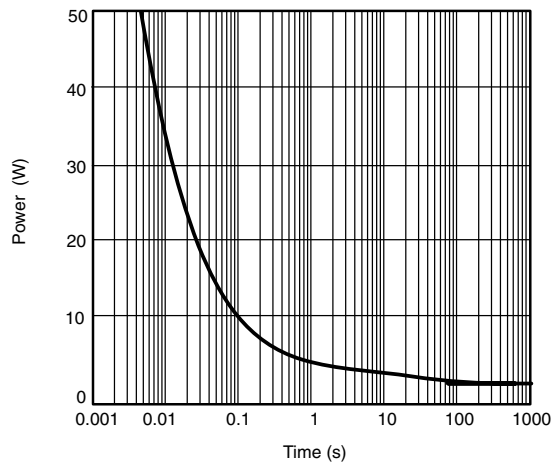
Source-Drain Diode Forward Voltage



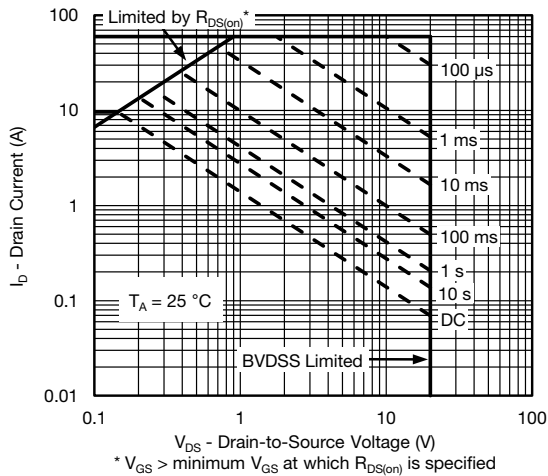
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

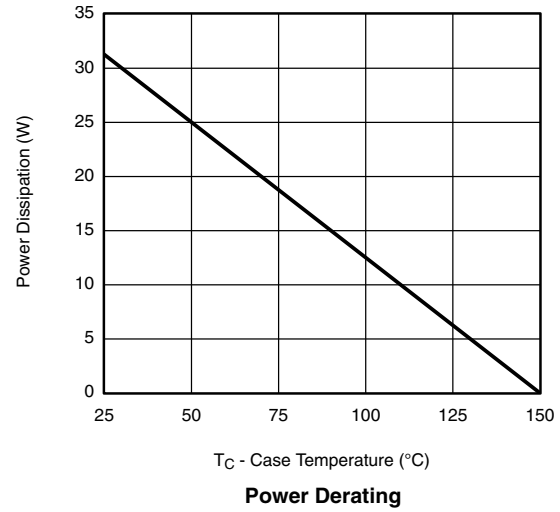
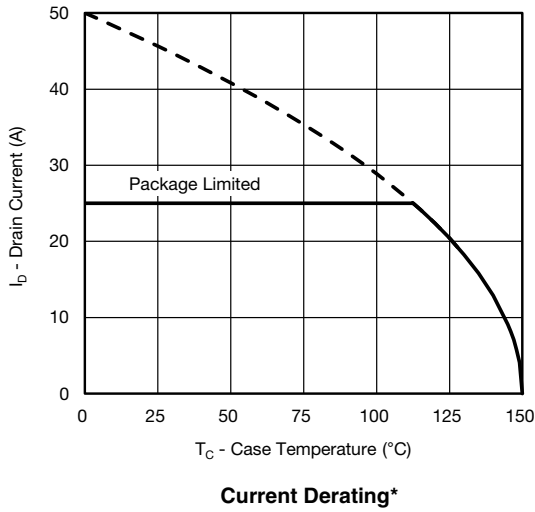


Single Pulse Power, Junction-to-Ambient



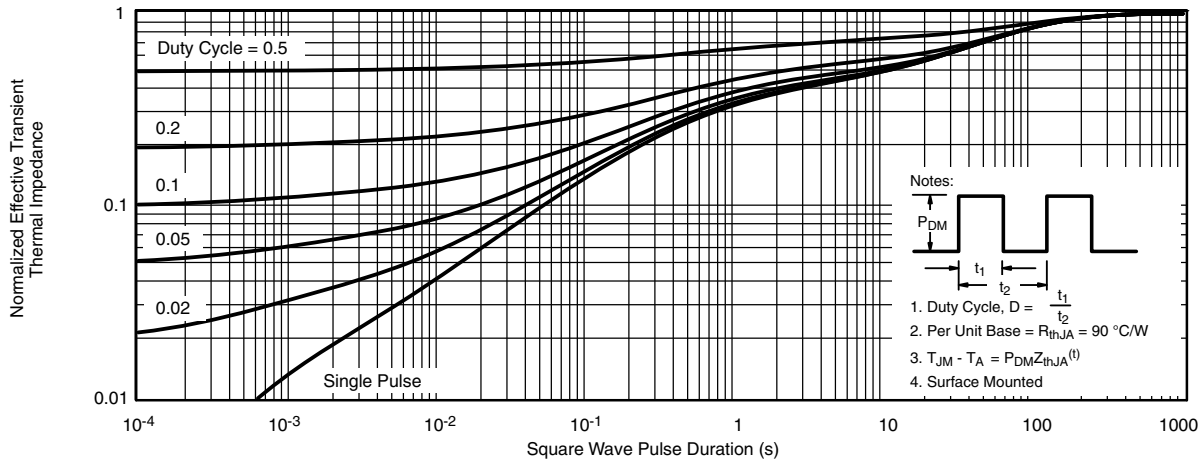
Safe Operating Area, Junction-to-Ambient

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

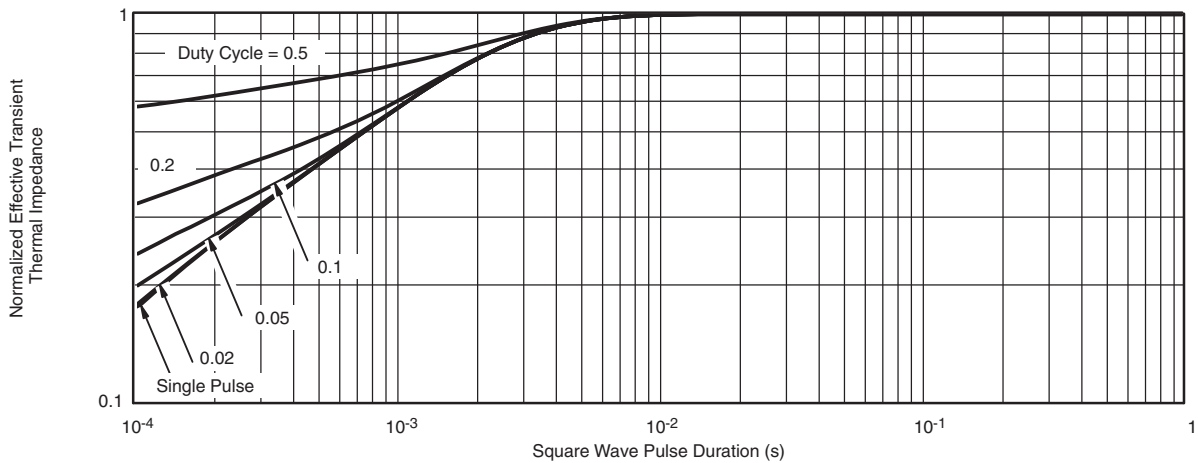


\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?63233](http://www.vishay.com/ppg?63233).

PowerPAK® ChipFET® Case Outline



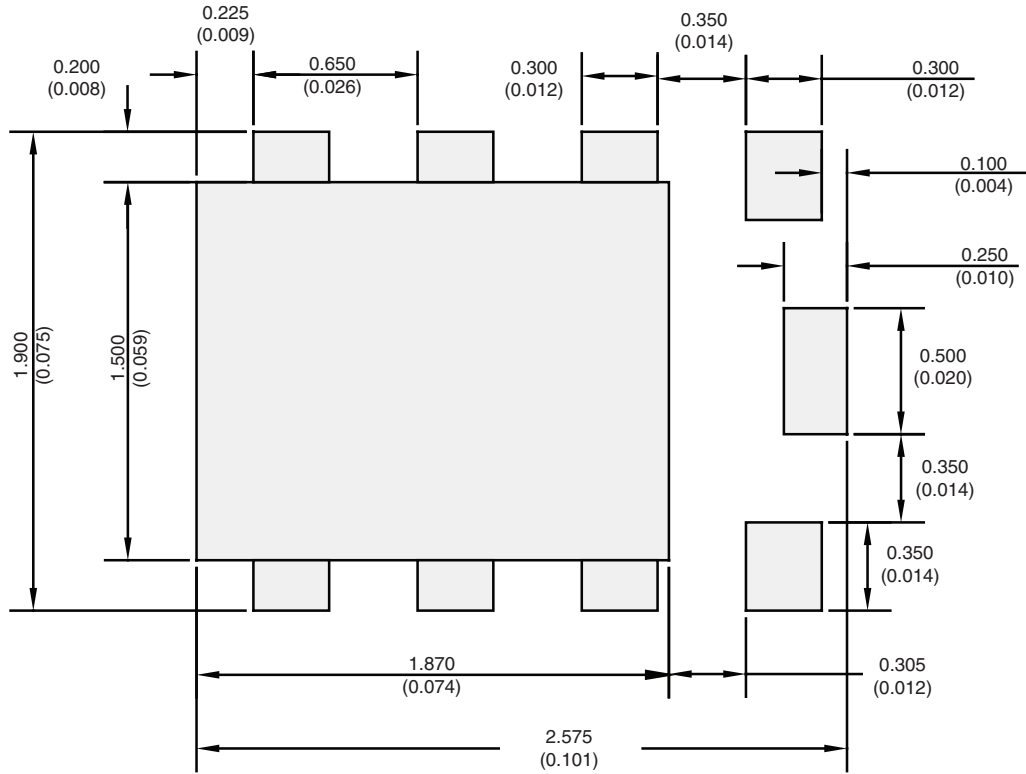
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

C14-0630-Rev. E, 21-Jul-14  
DWG: 5940

Note

- Millimeters will govern

## RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads  
Dimensions in mm/(Inches)

[Return to Index](#)





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