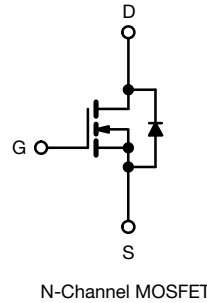
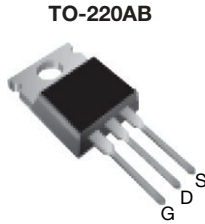


## Power MOSFET



### FEATURES

- Low gate charge  $Q_g$  results in simple drive requirement
- Improved gate, avalanche and dynamic  $dV/dt$  ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective  $C_{oss}$  specified
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS\***  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

### APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptable power supply
- High speed power switching

### TYPICAL SMPS TOPOLOGIES

- Two transistor forward
- Half bridge
- Full bridge

### PRODUCT SUMMARY

$V_{DS}$ (V)	500	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	3.0
$Q_g$ (Max.) (nC)	17	
$Q_{gs}$ (nC)	4.3	
$Q_{gd}$ (nC)	8.5	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF820APbF
Lead (Pb)-free and halogen-free	IRF820APbF-BE3


### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	500	V	
Gate-source voltage	$V_{GS}$	$\pm 30$		
Continuous drain current	$V_{GS}$ at 10 V	$T_C = 25$ °C	2.5	
		$T_C = 100$ °C	1.6	
Pulsed drain current <sup>a</sup>	$I_{DM}$	10	A	
Linear derating factor		0.40	W/°C	
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	140	mJ	
Repetitive avalanche current <sup>a</sup>	$I_{AR}$	2.5	A	
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	5.0	mJ	
Maximum power dissipation	$T_C = 25$ °C	$P_D$	50	W
Peak diode recovery $dV/dt$ <sup>c</sup>		$dV/dt$	3.4	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300 <sup>d</sup>		
Mounting torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting  $T_J = 25$  °C,  $L = 45$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 2.5$  A (see fig. 12)
- $I_{SD} \leq 2.5$  A,  $dI/dt \leq 270$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C
- 1.6 mm from case

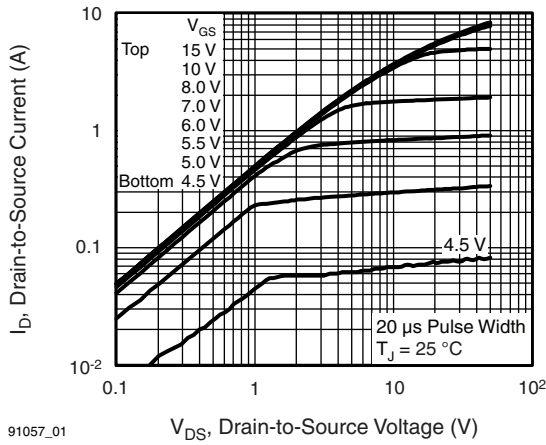
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Case-to-sink, flat, greased surface	$R_{thCS}$	0.50	-	
Maximum junction-to-case (drain)	$R_{thJC}$	-	2.5	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		500	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.60	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.5	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.5\text{ A}^b$	-	-	3.0	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 1.5\text{ A}^b$		1.4	-	-	S
<b>Dynamic</b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$ , see fig. 5		-	340	-	pF
Output capacitance	$C_{oss}$			-	53	-	
Reverse transfer capacitance	$C_{rss}$			-	2.7	-	
Output capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}; V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$		-	490	-	
Output capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$		-	15	-	
Effective output capacitance	$C_{oss\text{ eff.}}$	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ V to } 400\text{ V}^c$		-	28	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 2.5\text{ A}, V_{DS} = 400\text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	-	17	nC
Gate-source charge	$Q_{gs}$			-	-	4.3	
Gate-drain charge	$Q_{gd}$			-	-	8.5	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 2.5\text{ A},$ $R_g = 21\text{ }\Omega, R_D = 97\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	8.1	-	ns
Rise time	$t_r$			-	12	-	
Turn-Off delay time	$t_{d(off)}$			-	16	-	
Fall time	$t_f$			-	13	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	2.5	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$			-	-	10	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 2.5\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 2.5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	330	500	ns
Body diode reverse recovery charge	$Q_{rr}$			-	760	1140	nC
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

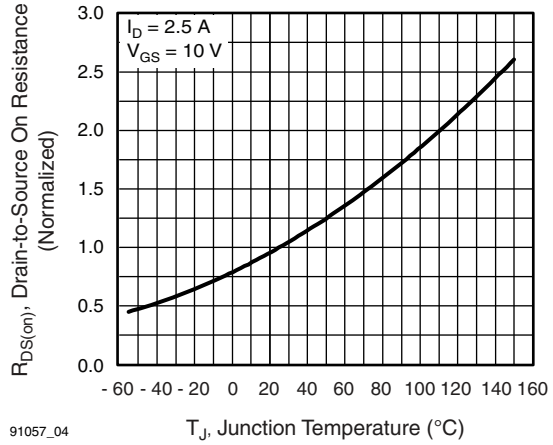
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



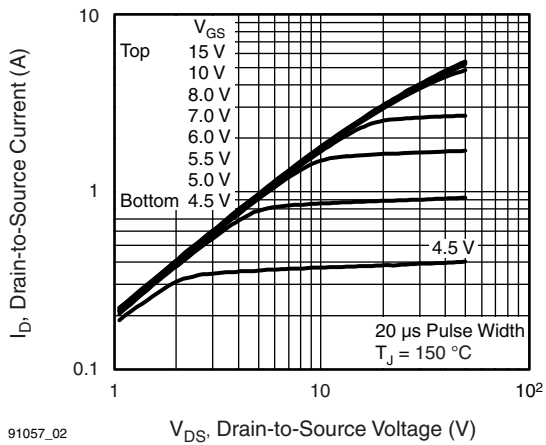
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**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$**



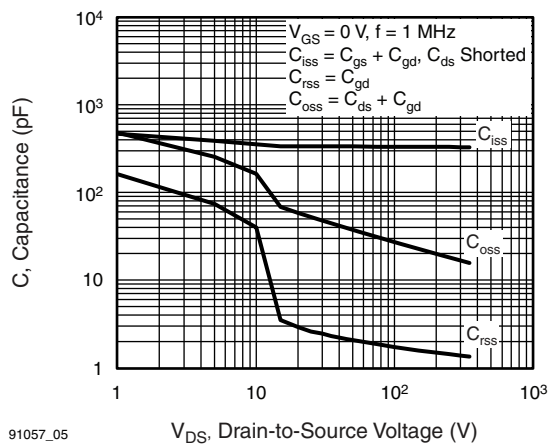
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**Fig. 4 - Normalized On-Resistance vs. Temperature**



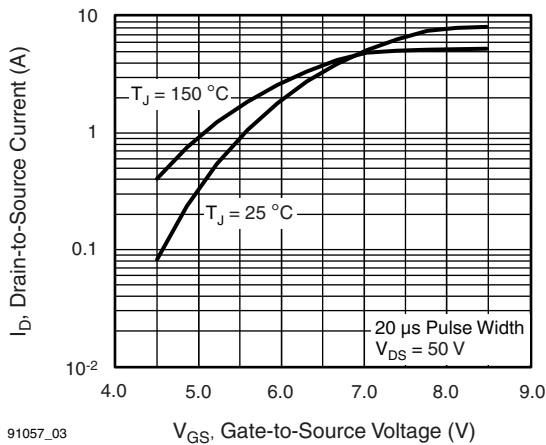
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**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$**



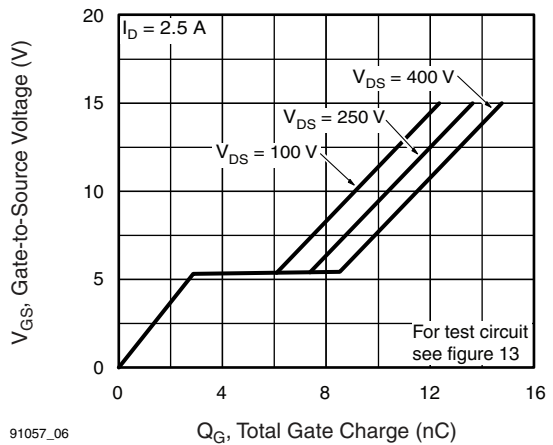
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**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



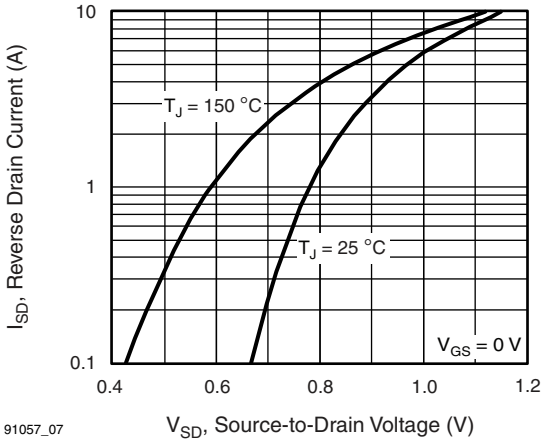
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**Fig. 3 - Typical Transfer Characteristics**



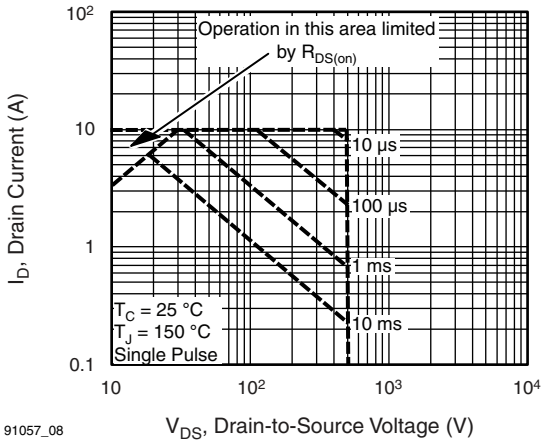
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**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



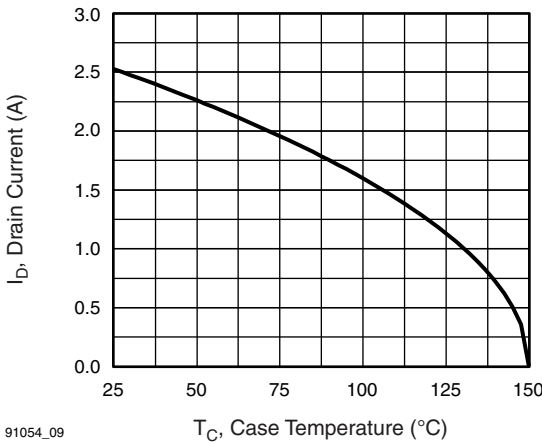
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 8 - Maximum Safe Operating Area



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Fig. 9 - Maximum Drain Current vs. Case Temperature

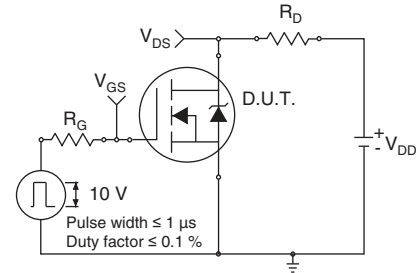


Fig. 10 - Switching Time Test Circuit

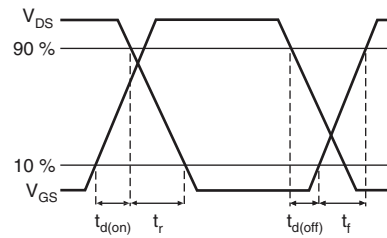
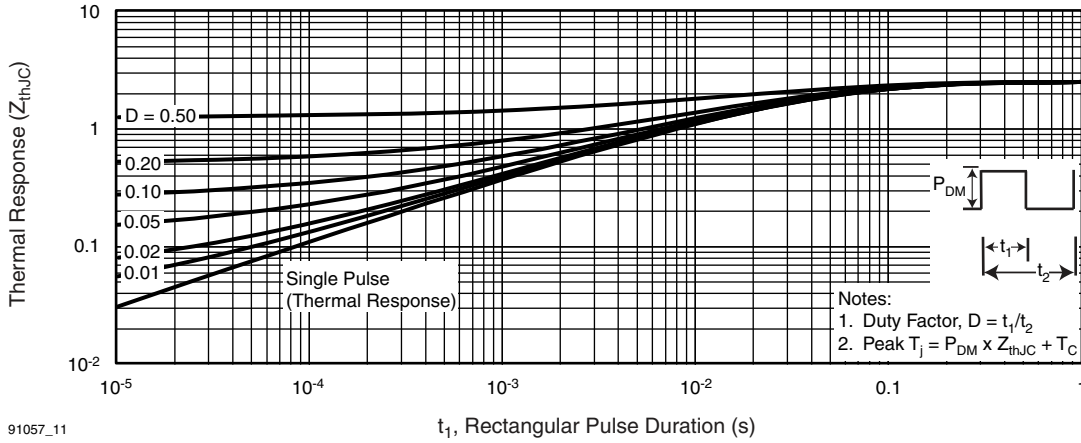


Fig. 11 - Switching Time Waveforms



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Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

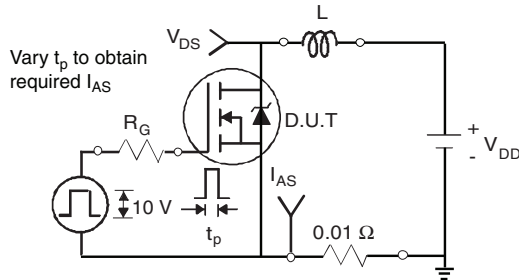


Fig. 13 - Unclamped Inductive Test Circuit

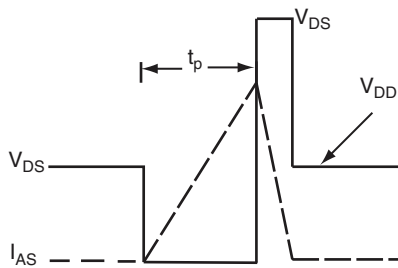
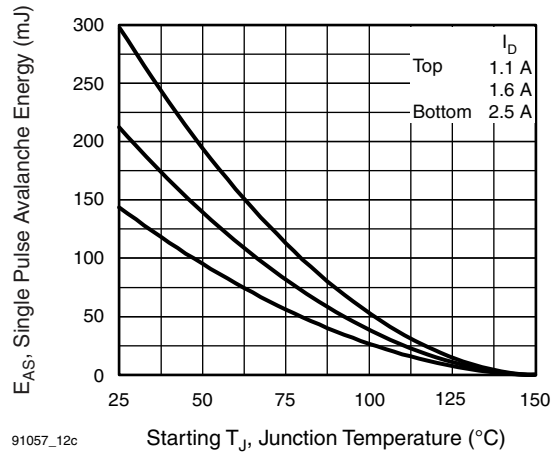


Fig. 14 - Unclamped Inductive Waveforms



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Fig. 15 - Maximum Avalanche Energy vs. Drain Current

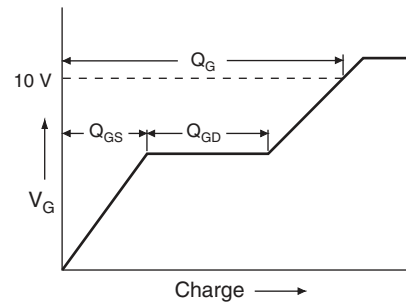
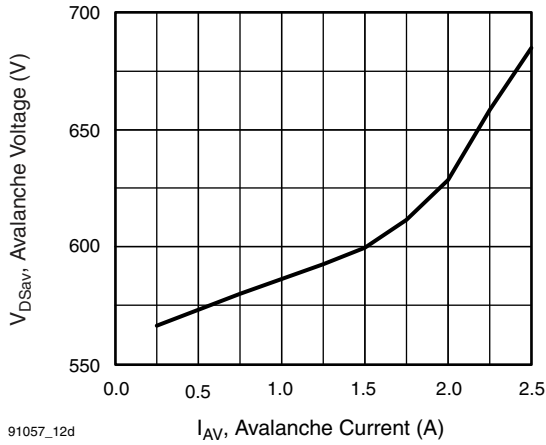
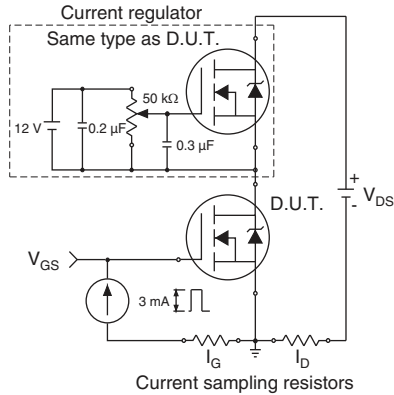


Fig. 16 - Basic Gate Charge Waveform



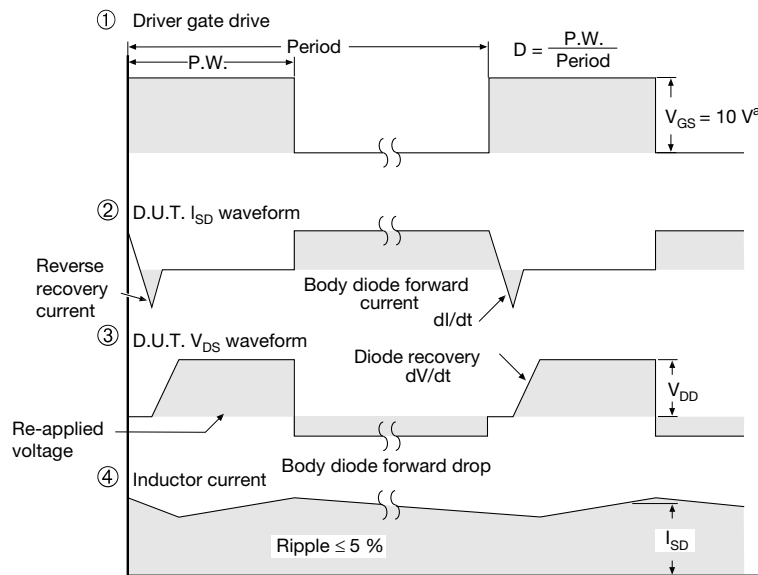
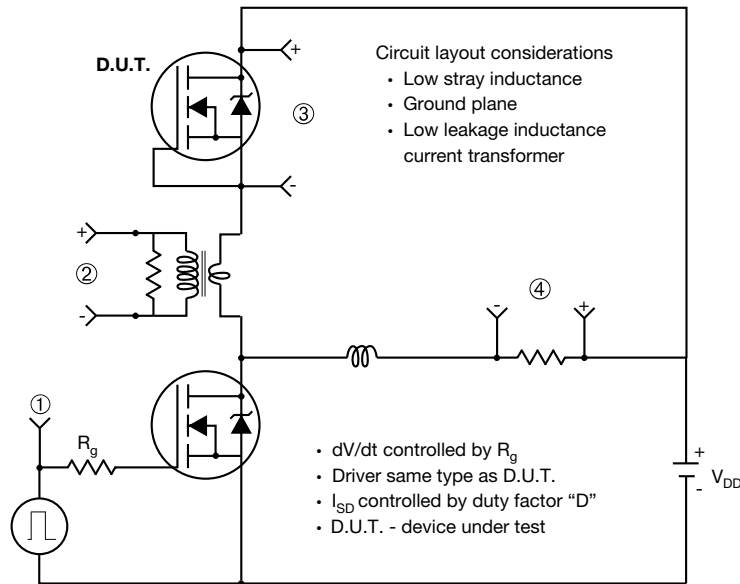
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**Fig. 17 - Typical Drain-to-Source Voltage vs. Avalanche Current**



**Fig. 18 - Gate Charge Test Circuit**

Peak Diode Recovery dV/dt Test Circuit



Note

a.  $V_{GS} = 5 V$  for logic level devices

Fig. 19 - For N-Channel

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