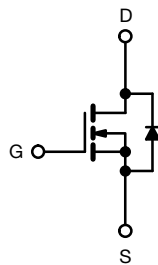
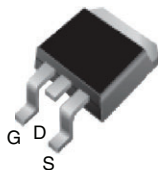


Power MOSFET

D²PAK (TO-263)

N-Channel MOSFET

PRODUCT SUMMARY

V _{DS} (V)	400	
R _{DS(on)} (Ω)	V _{GS} = 10 V	3.6
Q _g max. (nC)	17	
Q _{gs} (nC)	3.4	
Q _{gd} (nC)	8.5	
Configuration	Single	

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dv/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN
FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHF710S-GE3	SiHF710STRL-GE3 ^a
Lead (Pb)-free	IRF710SPbF	IRF710STRLPbF ^a

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	400	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current	V _{GS} at 10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed drain current ^a	I _{DM}	6.0	W/°C
Linear derating factor		0.29	
Linear derating factor (PCB mount) ^e		0.025	
Single pulse avalanche energy ^b	E _{AS}	120	mJ
Avalanche current ^a	I _{AR}	2.0	A
Repetitive avalanche energy ^a	E _{AR}	3.6	mJ
Maximum power dissipation	P _D	T _C = 25 °C	W
Maximum power dissipation (PCB mount) ^e		T _A = 25 °C	
Peak diode recovery dv/dt ^c	dv/dt	4.0	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V_{DD} = 50 V, starting T_J = 25 °C, L = 52 mH, R_g = 25 Ω, I_{AS} = 2.0 A (see fig. 12)
- I_{SD} ≤ 2.0 A, di/dt ≤ 40 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material).

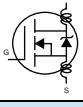
**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-ambient (PCB mount) ^a	R_{thJA}	-	40	
Maximum junction-to-case (drain)	R_{thJC}	-	3.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		400	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1\text{ mA}$		-	0.47	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.2\text{ A}^b$	-	-	3.6	Ω
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 1.2\text{ A}^b$		1.0	-	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5		-	170	-	pF
Output capacitance	C_{oss}			-	34	-	
Reverse transfer capacitance	C_{rss}			-	6.3	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 2.0\text{ A}, V_{DS} = 320\text{ V},$ see fig. 6 and 13 ^b	-	-	17	nC
Gate-source charge	Q_{gs}			-	-	3.4	
Gate-drain charge	Q_{gd}			-	-	8.5	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 200\text{ V}, I_D = 2.0\text{ A},$ $R_g = 24\text{ }\Omega, R_D = 95\text{ }\Omega,$ see fig. 10 ^b		-	8.0	-	ns
Rise time	t_r			-	9.9	-	
Turn-off delay time	$t_{d(off)}$			-	21	-	
Fall time	t_f			-	11	-	
Gate input resistance	R_g	$f = 1\text{ MHz},$ open drain		1.7	-	11.2	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	2.0	A
Pulsed diode forward current ^a	I_{SM}			-	-	6.0	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 2.0\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 2.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	240	540	ns
Body diode reverse recovery charge	Q_{rr}			-	0.85	1.6	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width $\leq 300\ \mu\text{s}$; duty cycle $\leq 2\ \%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

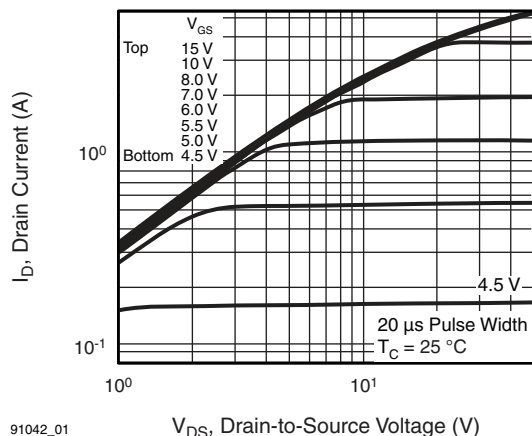


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ °C}$

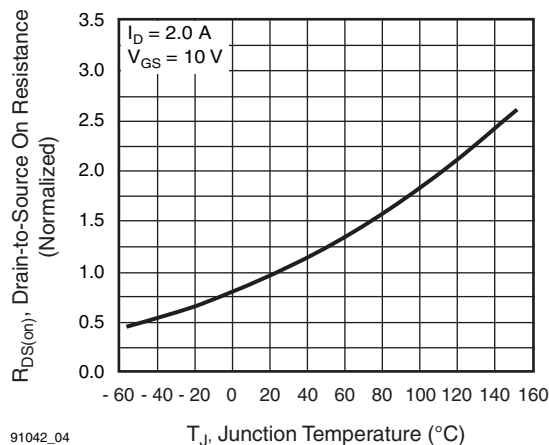


Fig. 4 - Normalized On-Resistance vs. Temperature

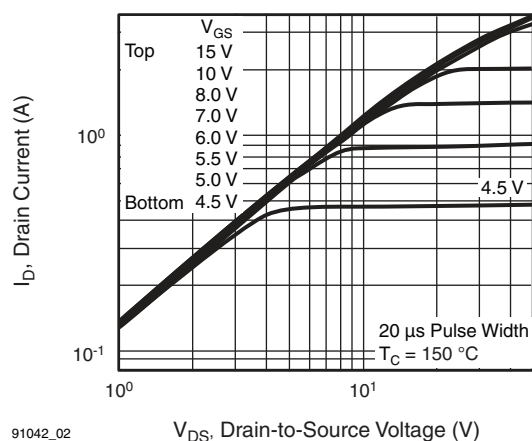


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ °C}$

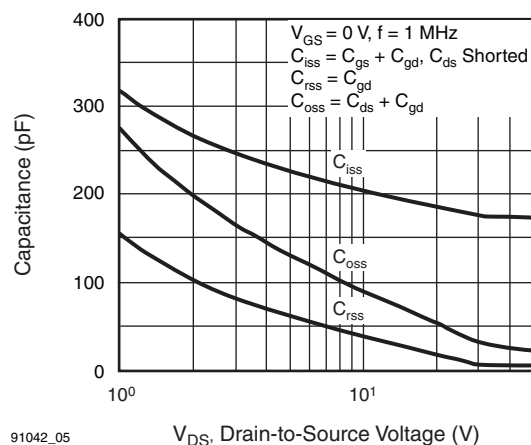


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

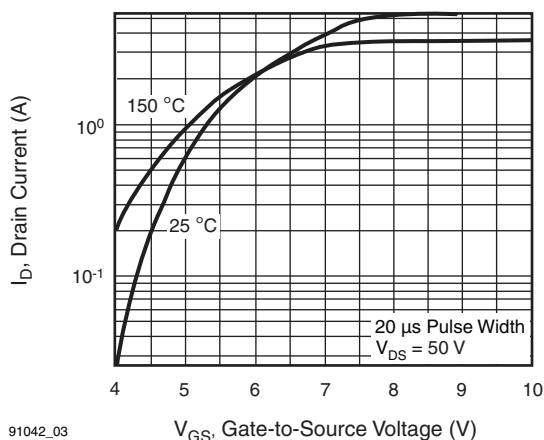


Fig. 3 - Typical Transfer Characteristics

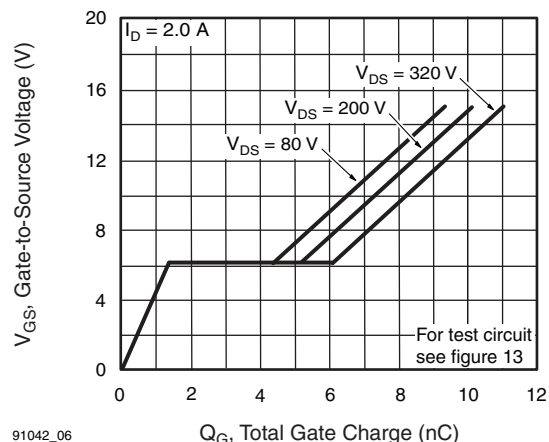
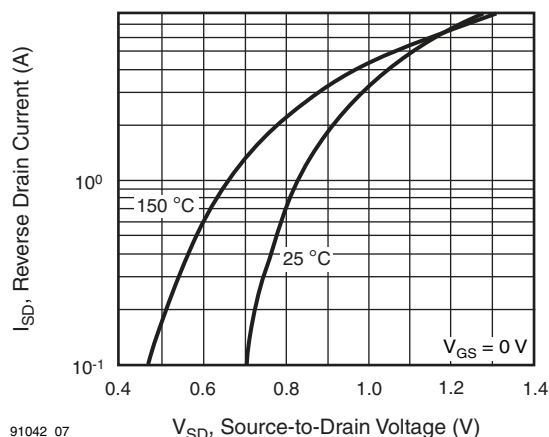
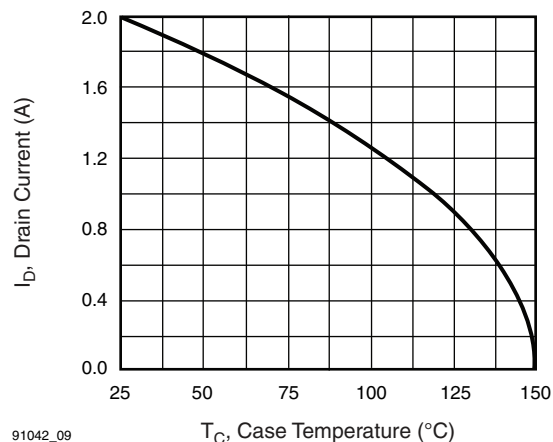
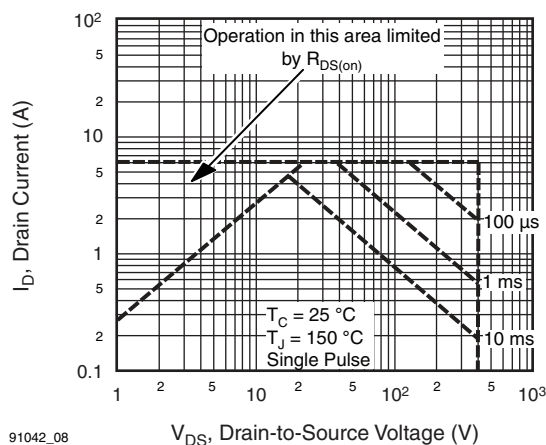
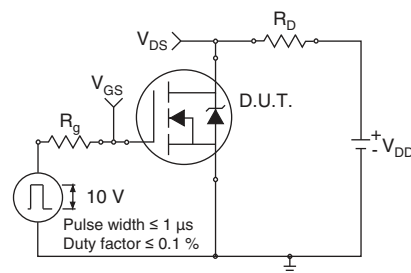
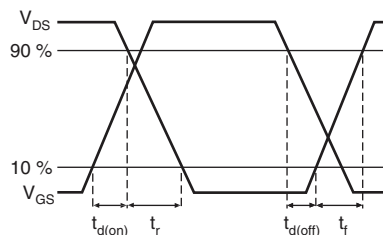
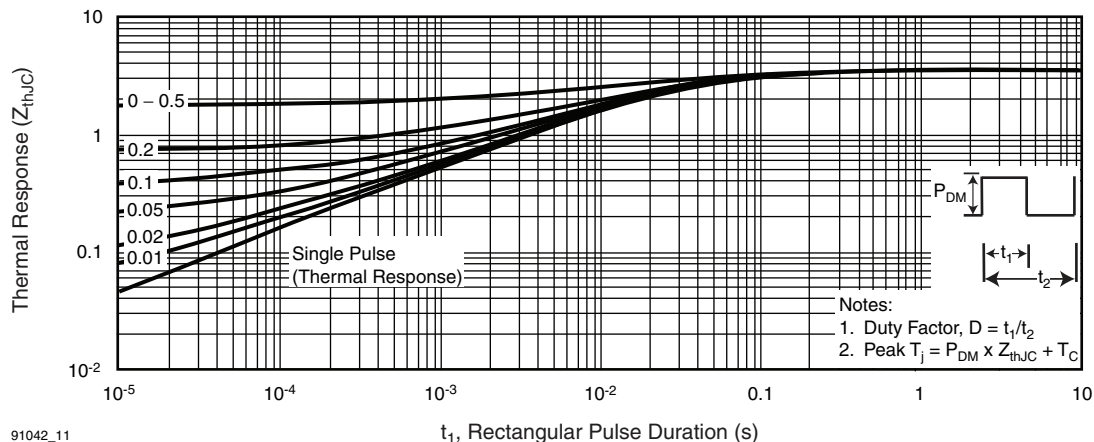
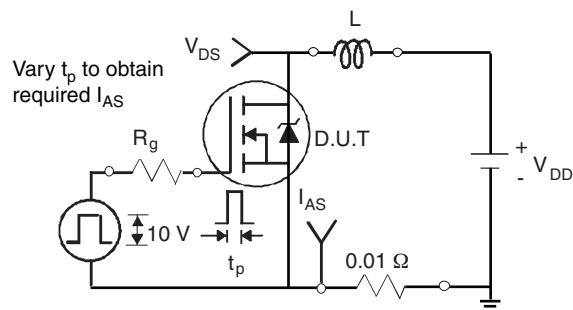
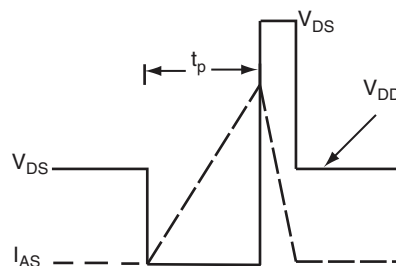
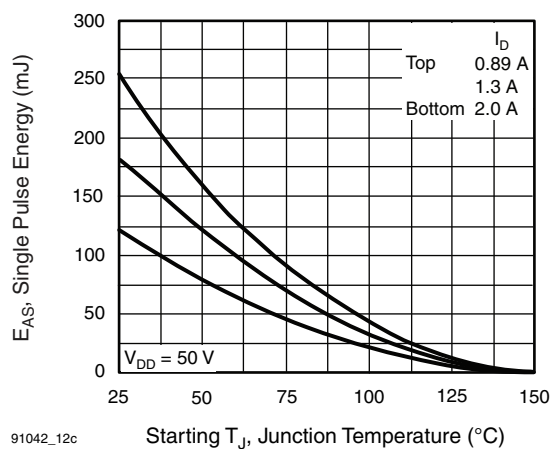
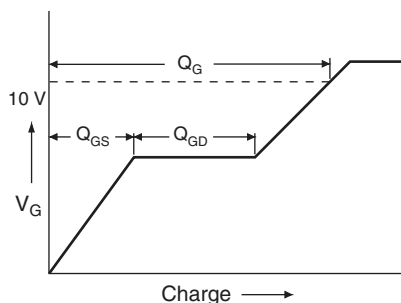
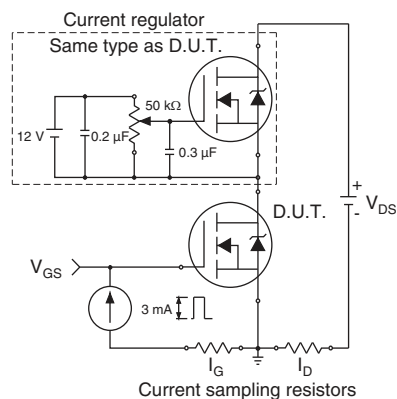
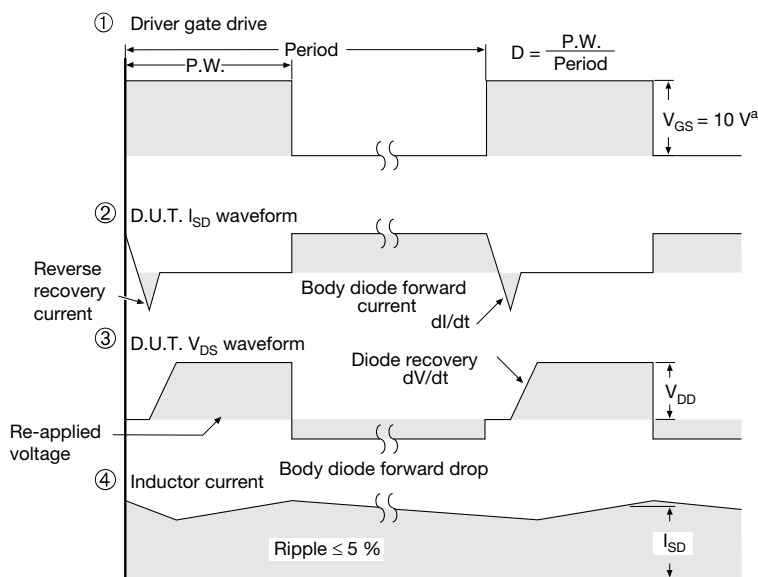
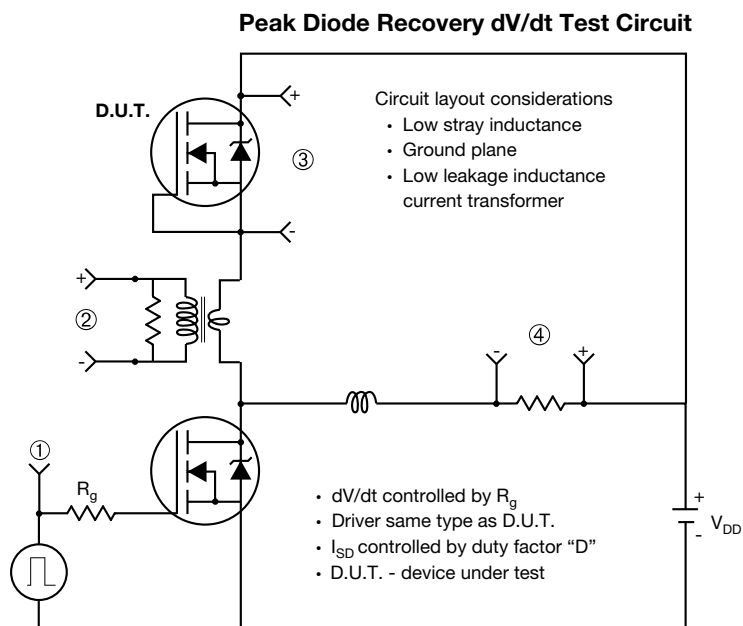


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Maximum Safe Operating Area

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

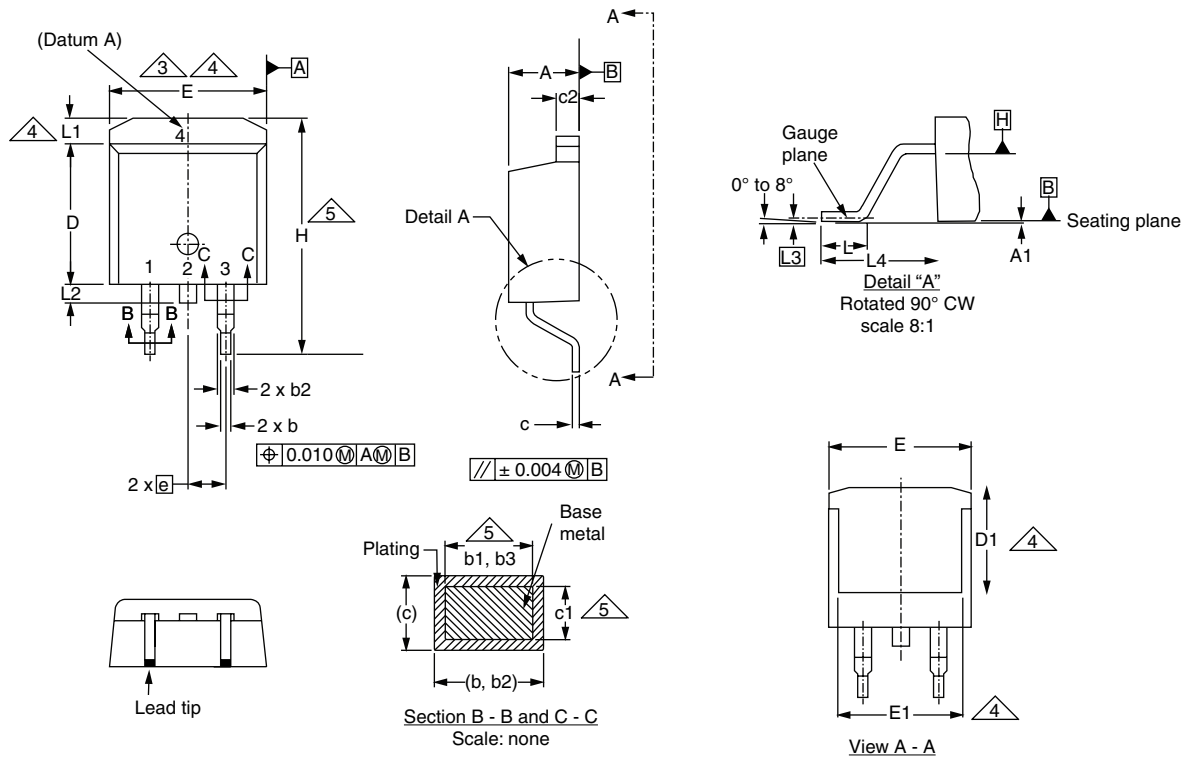

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91042.

TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

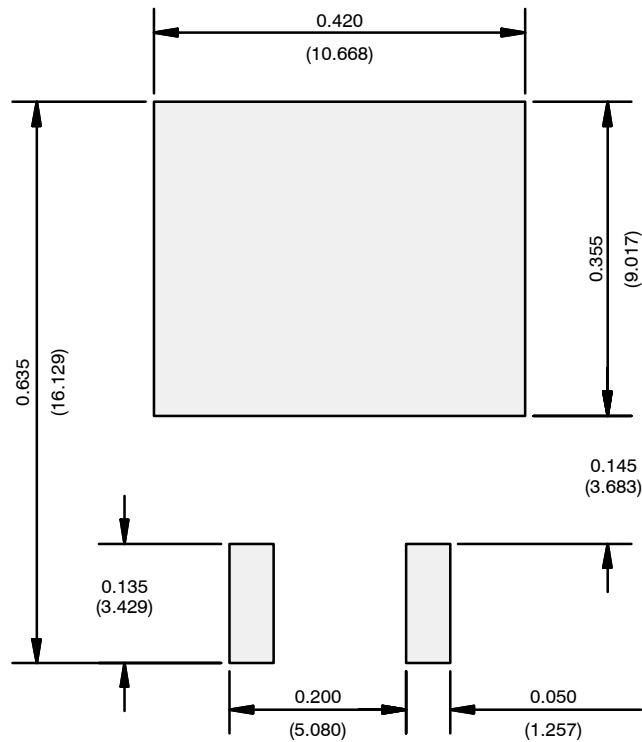
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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