

MOSFET – Power, Single N-Channel

60 V, 1.3 mΩ, 262 A

NVMJS1D4N06CL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPK8 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	60	V
Gate-to-Source Voltage			V _{GS}	20	V
Continuous Drain Current R _{θJC} (Notes 1, 3)	Steady State	T _C = 25°C	I _D	262	A
		T _C = 100°C		185	
Power Dissipation R _{θJC} (Note 1)		T _C = 25°C	P _D	180	W
		T _C = 100°C		90	
Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	Steady State	T _A = 25°C	I _D	39	A
		T _A = 100°C		28	
Power Dissipation R _{θJA} (Notes 1 & 2)		T _A = 25°C	P _D	4.0	W
		T _A = 100°C		2.0	
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		I _{DM}	900	A
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to + 175	°C
Source Current (Body Diode)			I _S	150	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 18.7 A)			E _{AS}	1376	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	0.83	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	37.8	

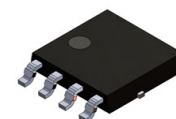
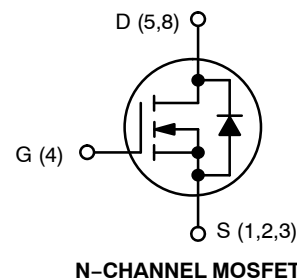
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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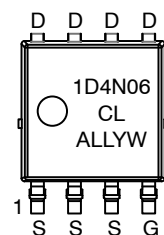
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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	1.3 mΩ @ 10 V	262 A
	1.8 mΩ @ 4.5 V	



LFPK8
CASE 760AA

MARKING DIAGRAM



1D4N06CL = Specific Device Code
 A = Assembly Location
 LL = Wafer Lot
 Y = Year
 W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMJS1D4N06CL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			25		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 280\text{ }\mu\text{A}$	1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.3		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$		1.45	1.8	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		1.07	1.3	
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 50\text{ A}$		244		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 30\text{ V}$		7430		pF
Output Capacitance	C_{OSS}			3500		
Reverse Transfer Capacitance	C_{RSS}			57		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 50\text{ A}$		47		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 50\text{ A}$		103		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 50\text{ A}$		10		
Gate-to-Source Charge	Q_{GS}			17		
Gate-to-Drain Charge	Q_{GD}			11		
Plateau Voltage	V_{GP}			2.6		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 50\text{ A}, R_G = 2.5\text{ }\Omega$		29		ns
Rise Time	t_r			21		
Turn-Off Delay Time	$t_{d(OFF)}$			52		
Fall Time	t_f			19		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 50\text{ A}$	$T_J = 25^{\circ}\text{C}$		0.78	1.2	V
			$T_J = 125^{\circ}\text{C}$		0.66		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 50\text{ A}$			86		ns
Charge Time	t_a				58		
Discharge Time	t_b				28		
Reverse Recovery Charge	Q_{RR}				175		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

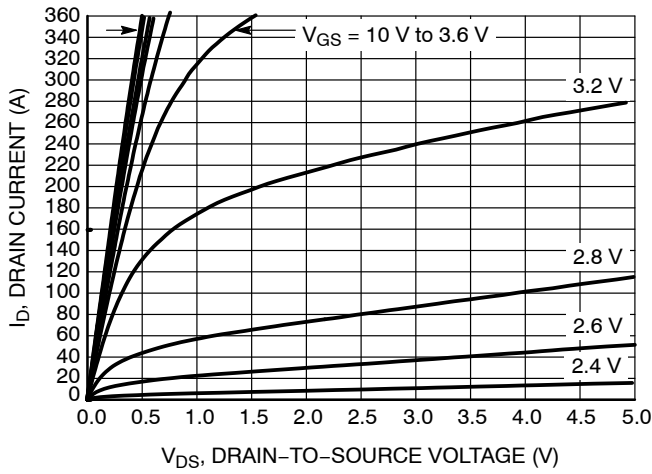


Figure 1. On-Region Characteristics

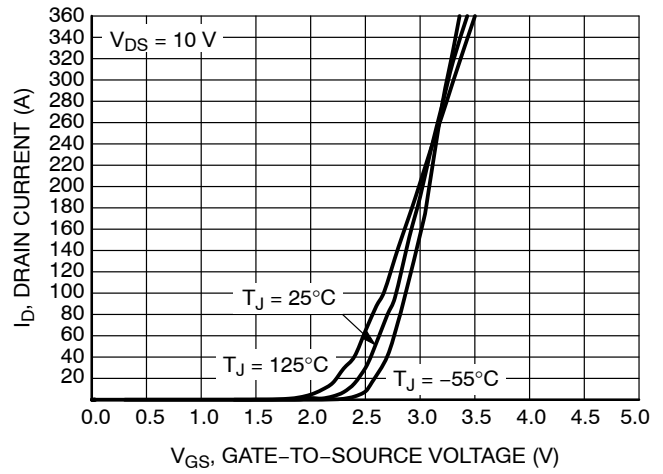


Figure 2. Transfer Characteristics

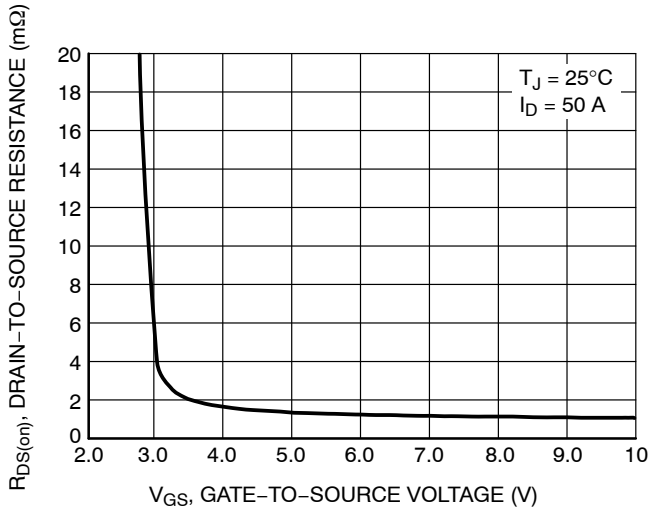


Figure 3. On-Resistance vs. Gate-to-Source Voltage

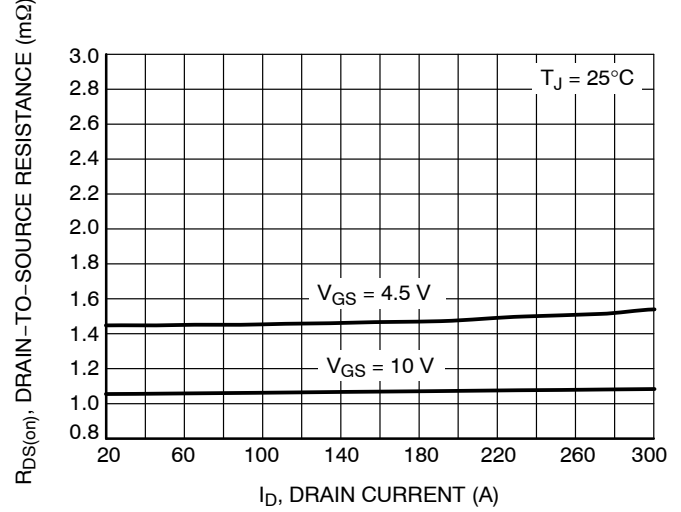


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

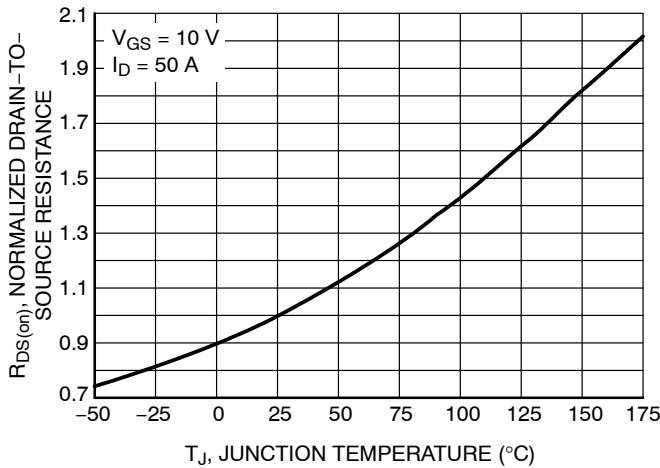


Figure 5. On-Resistance Variation with Temperature

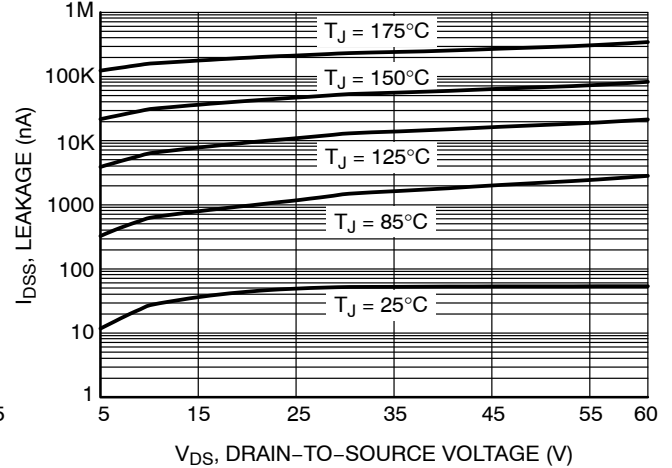


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

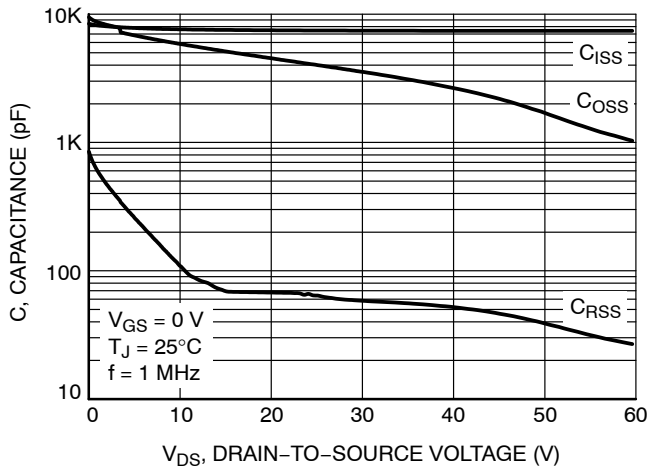


Figure 7. Capacitance Variation

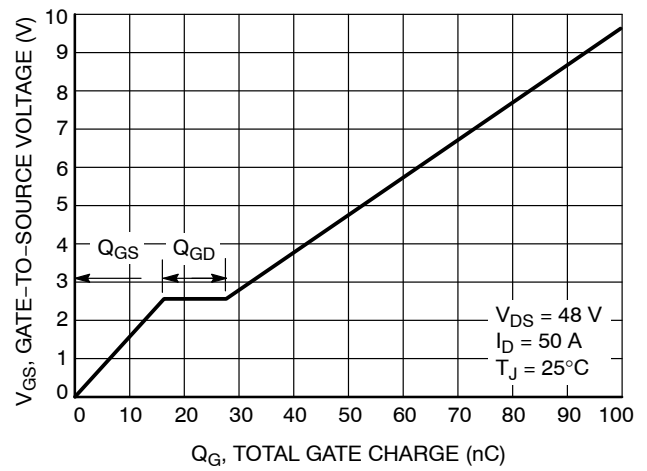


Figure 8. Gate-to-Source Voltage vs. Total Charge

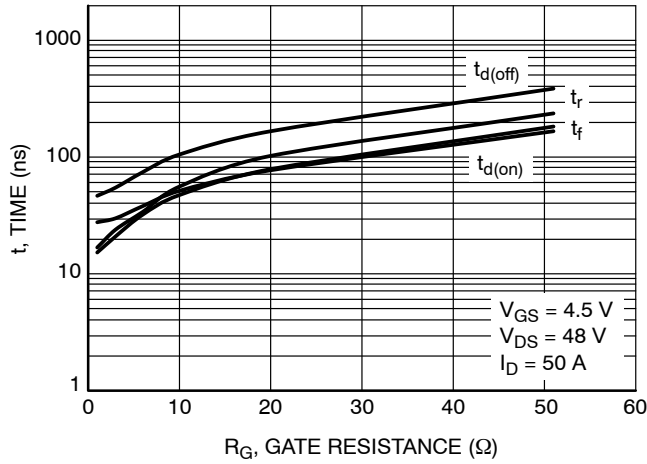


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

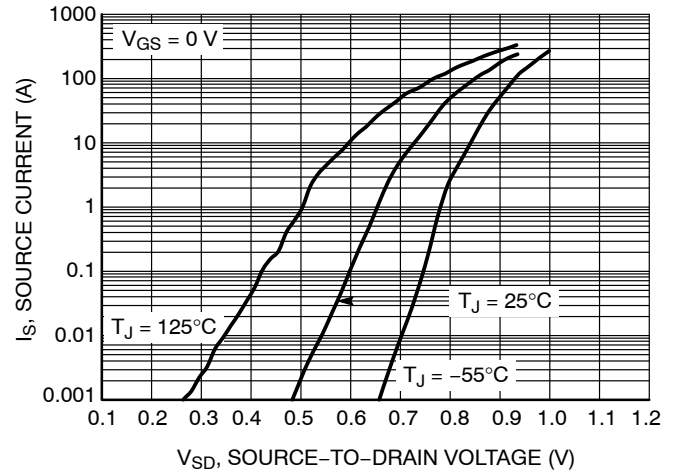


Figure 10. Diode Forward Voltage vs. Current

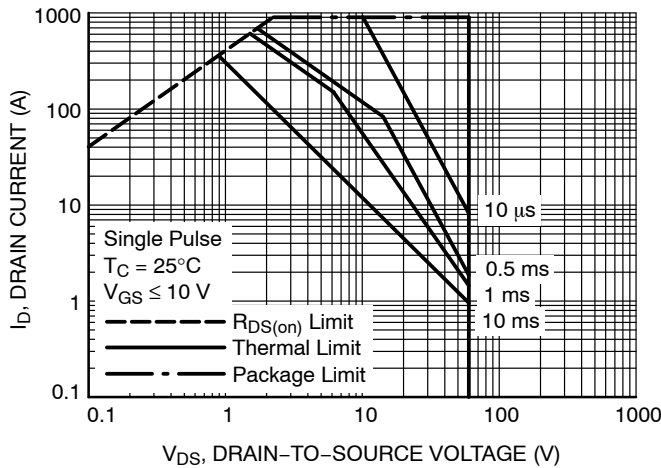


Figure 11. Maximum Rated Forward Biased Safe Operating Area

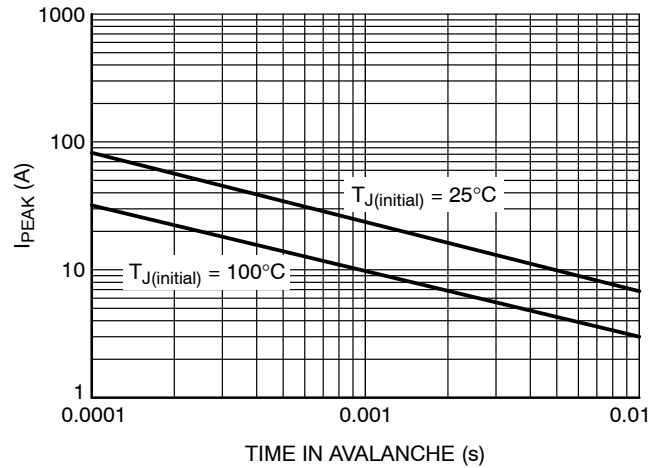


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

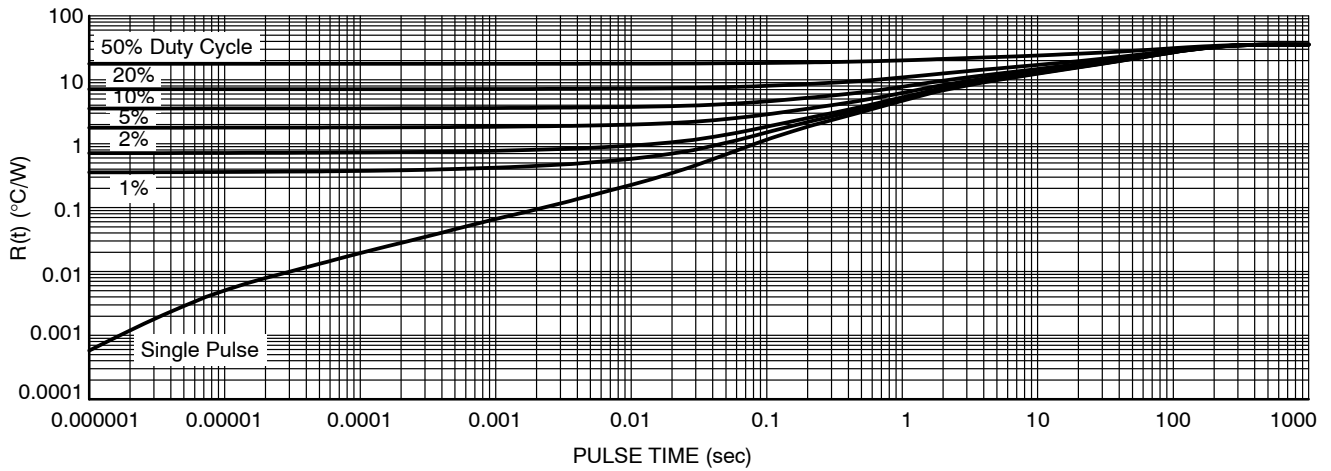


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMJS1D4N06CLTWG	1D4N06CL	LFPAK8 (Pb-Free)	3000 / Tape & Reel

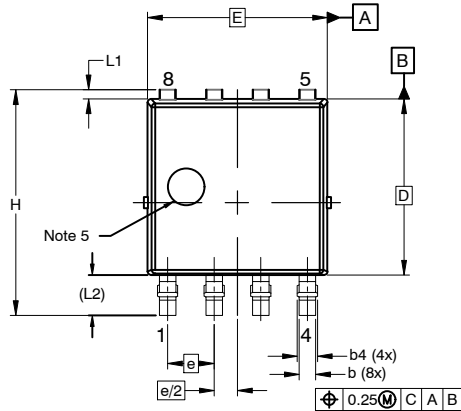
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

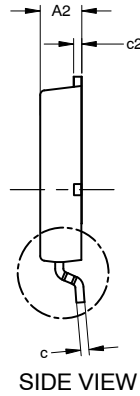


LPAK8 4.90x4.80x1.12MM, 1.27P
CASE 760AA
ISSUE D

DATE 22 APR 2024



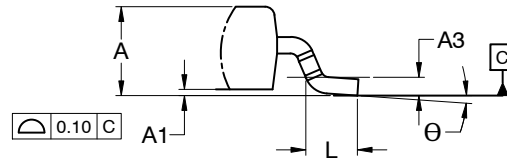
TOP VIEW



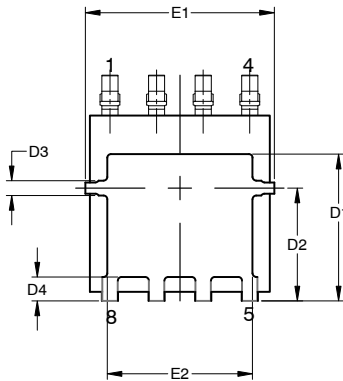
SIDE VIEW

NOTES:

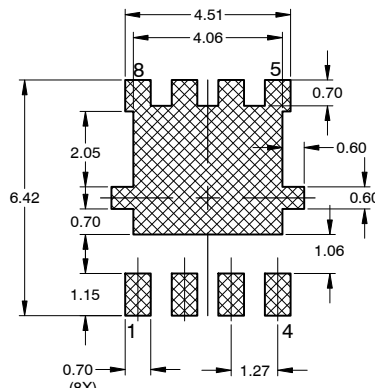
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. OPTIONAL MOLD FEATURE.



DETAIL 'A'



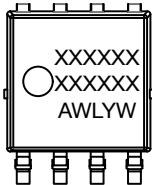
BOTTOM VIEW



RECOMMENDED LAND PAD

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 BSC		
b	0.40	0.45	0.50
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.70	4.80	4.90
D1	3.80	4.00	4.20
D2	2.98	3.08	3.18
D3	0.30	0.40	0.50
D4	0.55	0.65	0.75
E	4.80	4.90	5.00
E1	5.05	5.15	5.25
E2	3.91	3.96	4.01
e	1.27 BSC		
e/2	0.635 BSC		
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.15	0.25	0.35
L2	1.10 REF		
theta	0°	4°	8°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

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