

Silicon Carbide (SiC) MOSFET – 160 mohm, 1200 V, M1, TO-247-3L

NVHL160N120SC1

Features

- Typ. $R_{DS(on)} = 160 \text{ m}\Omega$
- Ultra Low Gate Charge (typ. $Q_{G(tot)} = 34 \text{ nC}$)
- Low Effective Output Capacitance (typ. $C_{oss} = 50 \text{ pF}$)
- 100% UIL Tested
- AEC-Q101 Qualified and PPAP Capable
- This Device is Halide Free and RoHS Compliant with exemption 7a, Pb-Free 2LI (on second level interconnection)

Typical Applications

- Automotive On Board Charger
- Automotive DC-DC Converter for EV/HEV

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	1200	V
Gate-to-Source Voltage	V_{GS}	-15/+25	V
Recommended Operation Values of Gate-to-Source Voltage	$T_C < 175^\circ\text{C}$ V_{GSop}	-5/+20	V
Continuous Drain Current	Steady State $T_C = 25^\circ\text{C}$ I_D	17	A
Power Dissipation	P_D	119	W
Continuous Drain Current	Steady State $T_C = 100^\circ\text{C}$ I_D	12	A
Power Dissipation	P_D	59	W
Pulsed Drain Current (Note 2)	$T_A = 25^\circ\text{C}$ I_{DM}	69	A
Single Pulse Surge Drain Current Capability	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$, $R_G = 4.7 \Omega$ I_{DSC}	140	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	11	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 23 \text{ A}$, $L = 1 \text{ mH}$) (Note 3)	E_{AS}	128	mJ

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

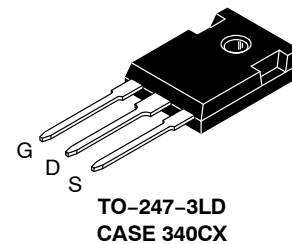
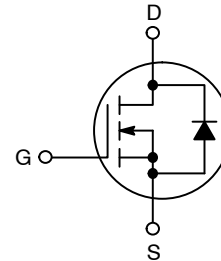
THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Junction-to-Case (Note 1)	$R_{\theta JC}$	1.3	$^\circ\text{C/W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	40	$^\circ\text{C/W}$

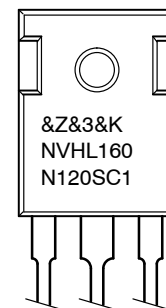
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Repetitive rating, limited by max junction temperature.
3. E_{AS} of 128 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 1 \text{ mH}$, $I_{AS} = 16 \text{ A}$, $V_{DD} = 120 \text{ V}$, $V_{GS} = 18 \text{ V}$.

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
1200 V	224 m Ω @ 20 V	17 A

N-CHANNEL MOSFET



MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Date Code (Year & Week)
&K = Lot
NVHL160N120SC1 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NVHL160N120SC1	TO247-3L	30 Units / Tube

NVHL160N120SC1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	1200	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = 1 mA, referenced to 25°C	–	600	–	mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 1200 V, T _J = 25°C	–	–	100	μA
		V _{GS} = 0 V, V _{DS} = 1200 V, T _J = 175°C	–	–	250	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = +25/-15 V, V _{DS} = 0 V	–	–	±1	μA

ON CHARACTERISTICS

Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 2.5 mA	1.8	3.1	4.3	V
Recommended Gate Voltage	V _{GOP}		–5	–	+20	V
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 20 V, I _D = 12 A, T _J = 25°C	–	162	224	mΩ
		V _{GS} = 20 V, I _D = 12 A, T _J = 175°C	–	271	377	
Forward Transconductance	g _{FS}	V _{DS} = 10 V, I _D = 12 A	–	3	–	S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 800 V	–	665	–	pF
Output Capacitance	C _{OSS}		–	50	–	
Reverse Transfer Capacitance	C _{RSS}		–	5	–	
Total Gate Charge	Q _{G(tot)}	V _{GS} = –5/20 V, V _{DS} = 600 V, I _D = 16 A	–	34	–	nC
Threshold Gate Charge	Q _{G(th)}		–	6	–	
Gate-to-Source Charge	Q _{GS}		–	12.5	–	
Gate-to-Drain Charge	Q _{GD}		–	9.6	–	
Gate Resistance	R _G	f = 1 MHz	–	1.4	–	Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(on)}	V _{GS} = –5/20 V, V _{DS} = 800 V, I _D = 16 A, R _G = 6 Ω, Inductive Load	–	11	–	ns
Rise Time	t _r		–	19	–	
Turn-Off Delay Time	t _{d(off)}		–	15	–	
Fall Time	t _f		–	8	–	
Turn-On Switching Loss	E _{ON}		–	200	–	μJ
Turn-Off Switching Loss	E _{OFF}		–	34	–	
Total Switching Loss	E _{TOT}		–	234	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

Continuous Drain-to-Source Diode Forward Current	I _{SD}	V _{GS} = –5 V, T _J = 25°C	–	–	11	A
Pulsed Drain-to-Source Diode Forward Current (Note 2)	I _{SDM}	V _{GS} = –5 V, T _J = 25°C	–	–	69	A
Forward Diode Voltage	V _{SD}	V _{GS} = –5 V, I _{SD} = 6 A, T _J = 25°C	–	4	10	V
Reverse Recovery Time	t _{RR}	V _{GS} = –5/20 V, I _{SD} = 16 A, dI _S /dt = 1000 A/μs	–	15	–	ns
Reverse Recovery Charge	Q _{RR}		–	45	–	nC
Reverse Recovery Energy	E _{REC}		–	3.9	–	μJ
Peak Reverse Recovery Current	I _{RRM}		–	6.2	–	A
Charge Time	T _a		–	7.4	–	ns
Discharge Time	T _b		–	7	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

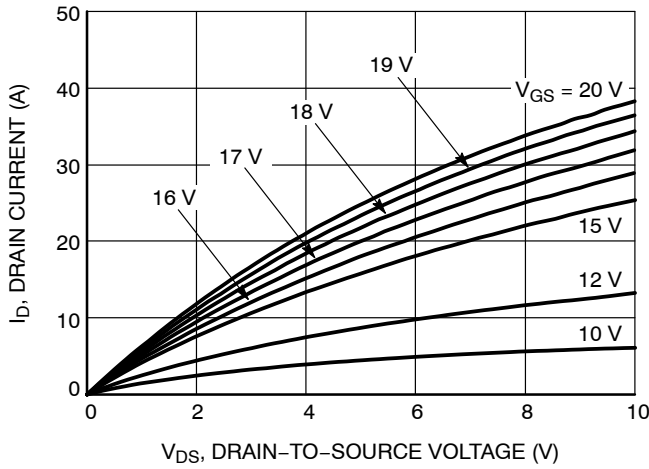


Figure 1. On-Region Characteristics

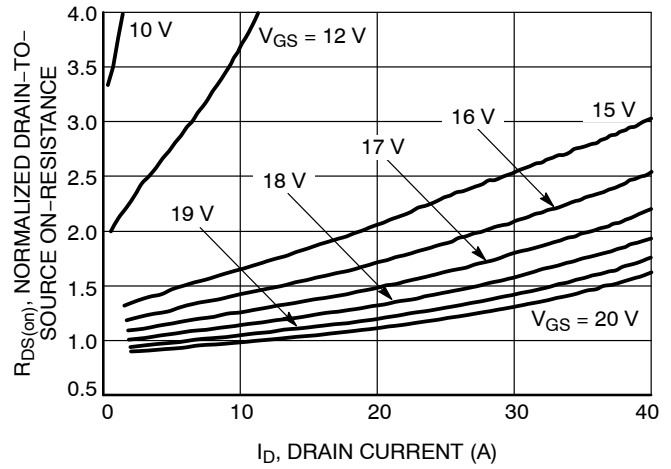


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

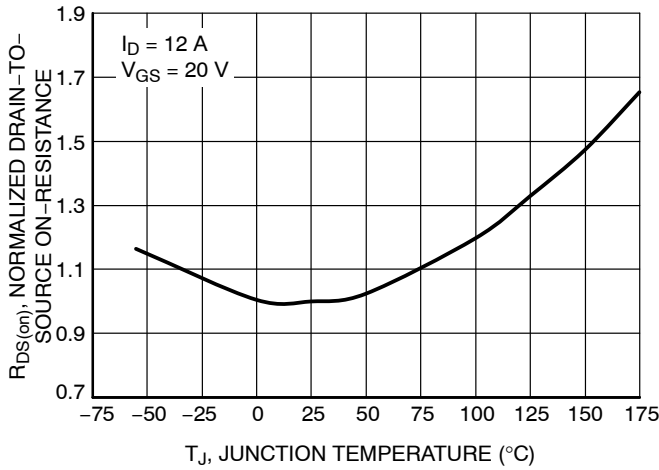


Figure 3. On-Resistance Variation with Temperature

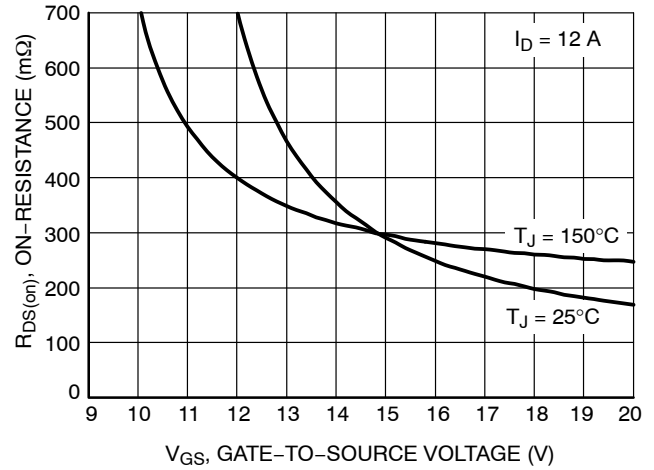


Figure 4. On-Resistance vs. Gate-to-Source Voltage

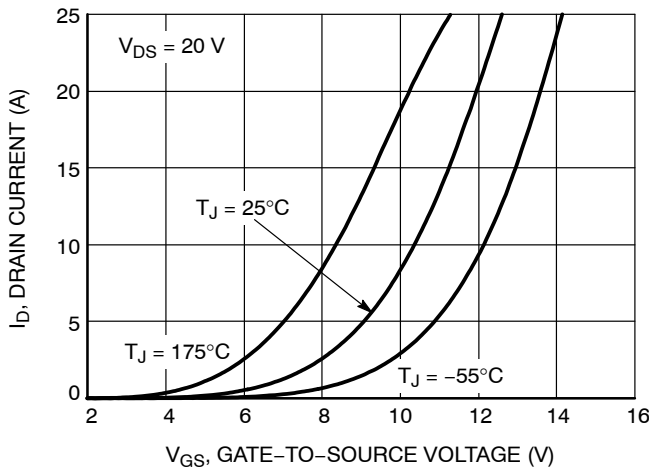


Figure 5. Transfer Characteristics

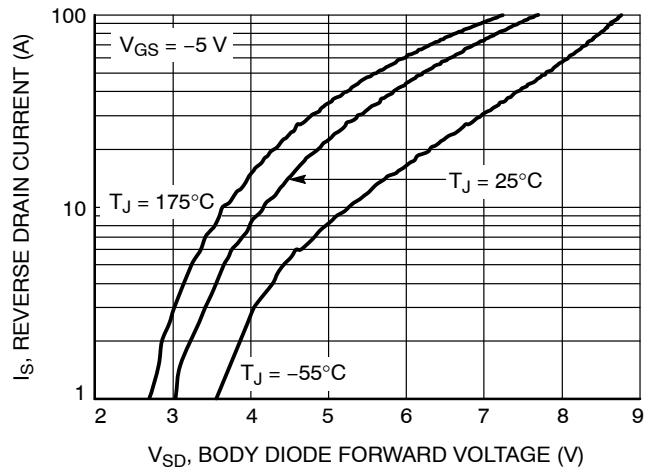


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS (continued)

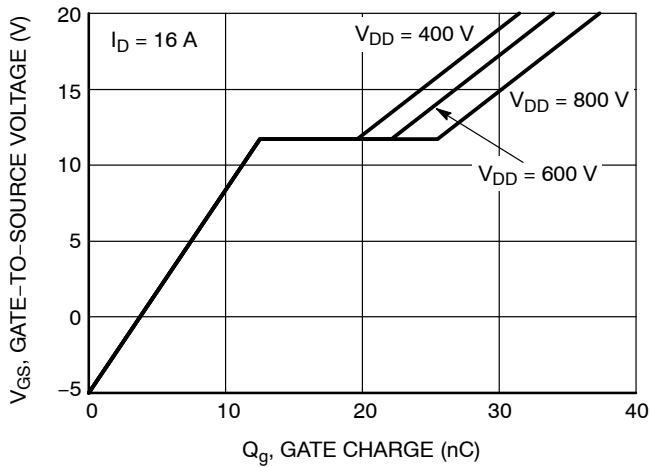


Figure 7. Gate-to-Source Voltage vs. Total Charge

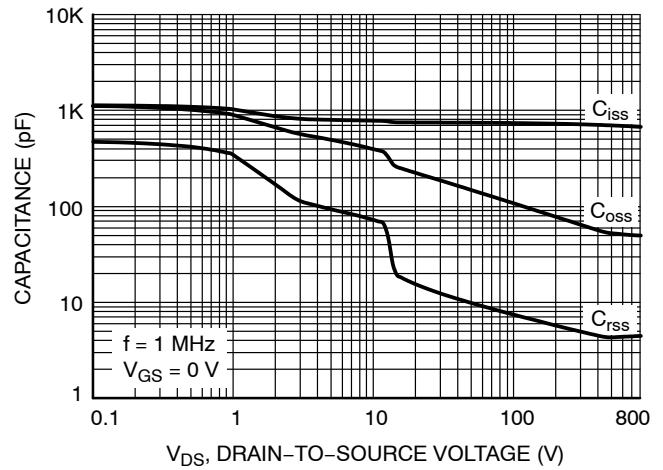


Figure 8. Capacitance vs. Drain-to-Source Voltage

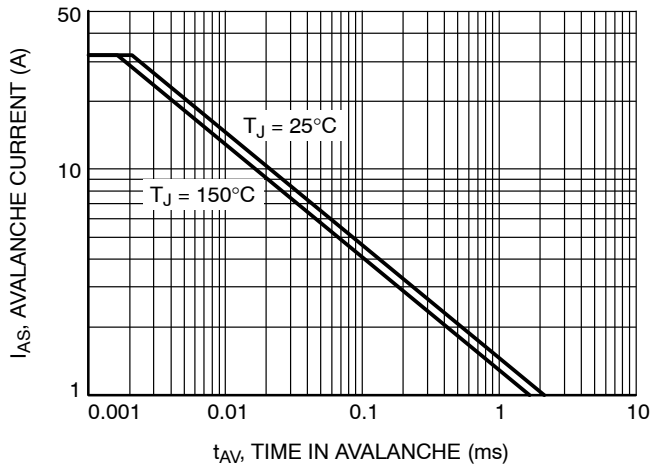


Figure 9. Unclamped Inductive Switching Capability

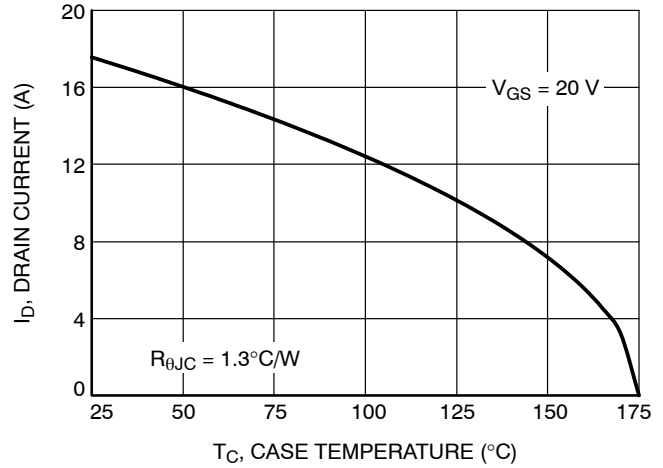


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

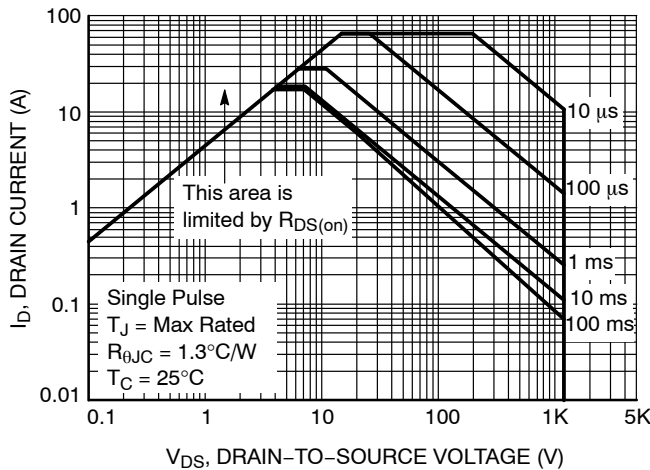


Figure 11. Safe Operating Area

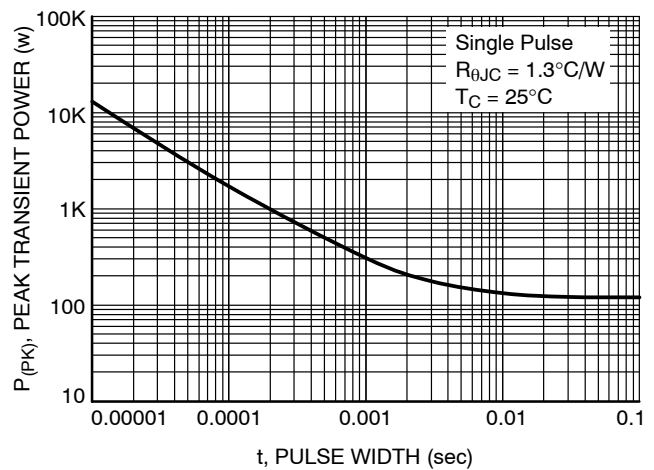


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

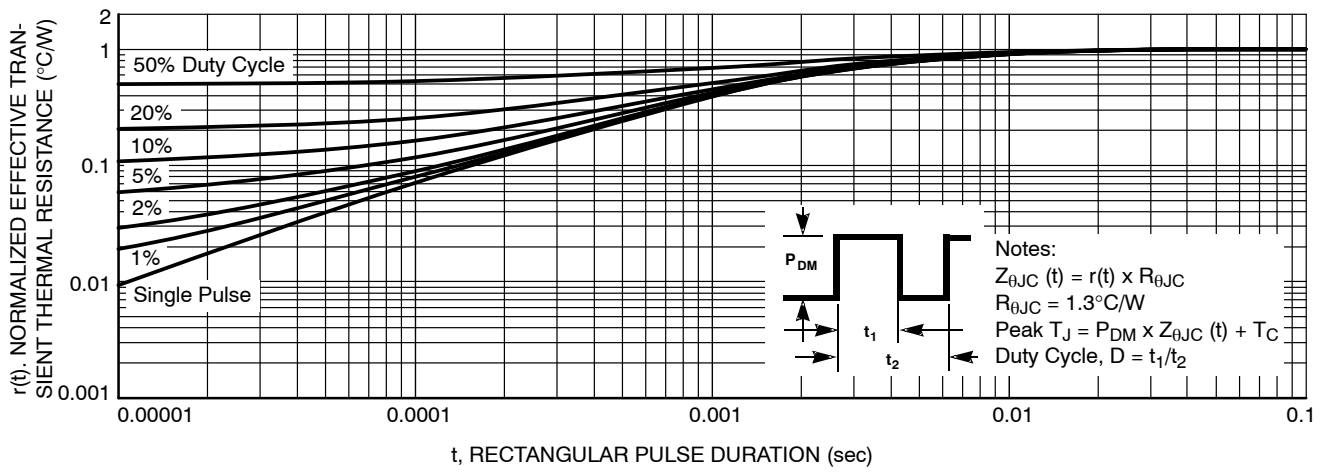


Figure 13. Junction-to-Ambient Thermal Response

MECHANICAL CASE OUTLINE

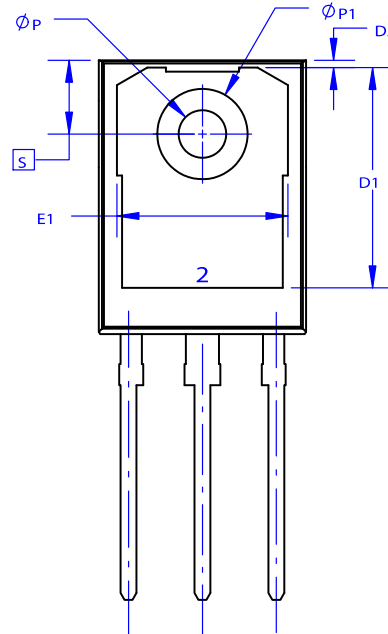
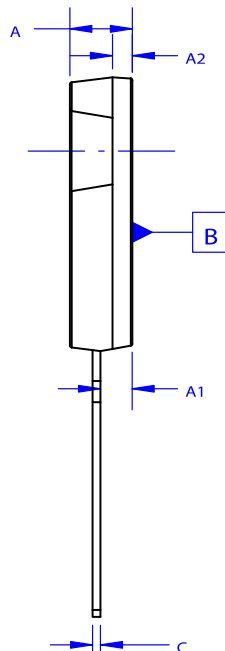
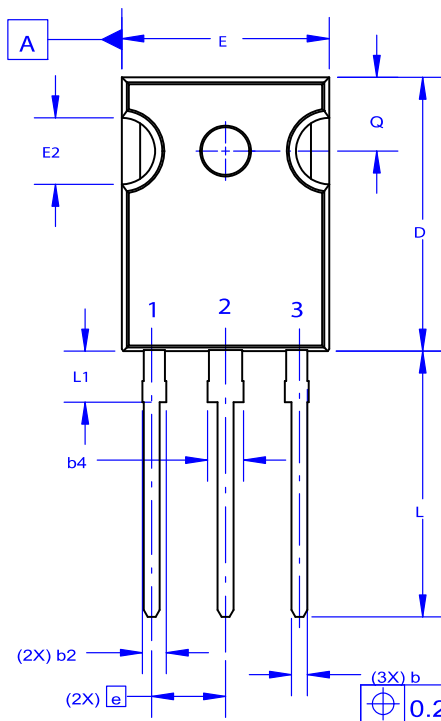
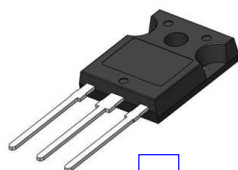
PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD
CASE 340CX
ISSUE A

DATE 06 JUL 2020



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

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