

MOSFET - Power, Single N-Channel, Small Signal

20 V, 220 mA

NTNS0K8N021Z

Features

- Low Profile Ultra Small Package, XDFN3 (0.62 x 0.42 x 0.4 mm) for Extremely Space-Constrained Applications
- 1.5 V Gate Drive
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Small Signal Load Switch
- High Speed Interfacing
- Level Shift

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	20	V
Gate-to-Source Voltage			V _{GS}	±8	V
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	220	mA
		T _A = 85°C		158	
	t ≤ 5 s	T _A = 25°C		253	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	125	mW
	t ≤ 5 s			166	
Pulsed Drain Current	t _p = 10 μs		I _{DM}	846	mA
Operating Junction and Storage Temperature Range			T _J , T _{STG}	-55 to 150	°C
Source Current (Body Diode) (Note 2)			I _S	200	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using the minimum recommended pad size, or 2 mm², 1 oz Cu.
2. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$

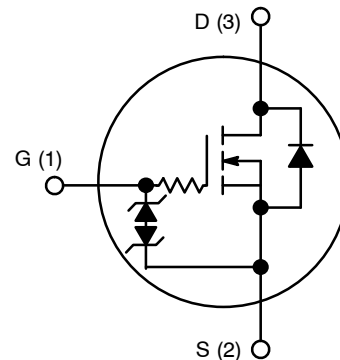


ON Semiconductor®

www.onsemi.com

$V_{(BR)DS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ Max}$
20 V	1.5 Ω @ 4.5 V	220 mA
	3.3 Ω @ 1.8 V	
	8.0 Ω @ 1.2 V	

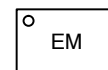
N-CHANNEL MOSFET



MARKING DIAGRAM



XDFN3
CASE 711BH



1

E = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NTNS0K8N021ZTCG	XDFN3 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	998	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	751	

3. Surface-mounted on FR4 board using the minimum recommended pad size, or 2 mm², 1 oz Cu.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 5\text{ V}, T_J = 25^\circ\text{C}$			50	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}, T_J = 25^\circ\text{C}$			100	nA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	0.4		1.0	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 100\text{ mA}$		0.8	1.5	Ω
		$V_{GS} = 1.8\text{ V}, I_D = 20\text{ mA}$		1.4	3.0	
		$V_{GS} = 1.2\text{ V}, I_D = 10\text{ mA}$		3.2	8.0	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 125\text{ mA}$		0.48		S
Source-Drain Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 10\text{ mA}$		0.6	1.0	V

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, \text{freq} = 1\text{ MHz}, V_{DS} = 15\text{ V}$		12.3		pF
Output Capacitance	C_{OSS}			3.4		
Reverse Transfer Capacitance	C_{RSS}			2.5		

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 15\text{ V}, I_D = 200\text{ mA}, R_G = 2\text{ }\Omega$		16.5		ns
Rise Time	t_r			25.5		
Turn-Off Delay Time	$t_{d(OFF)}$			142		
Fall Time	t_f			80		

4. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

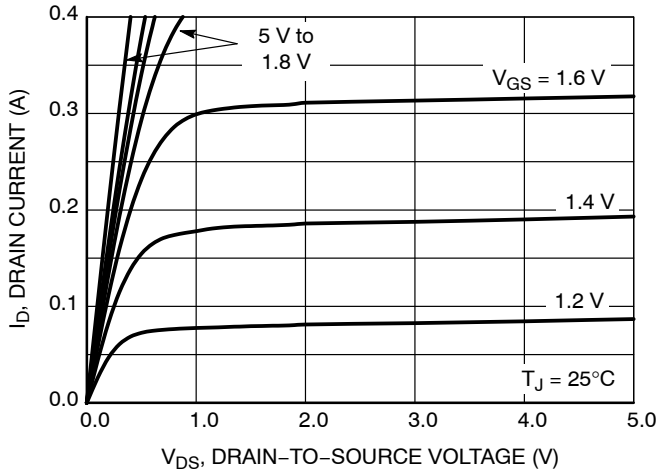


Figure 1. On-Region Characteristics

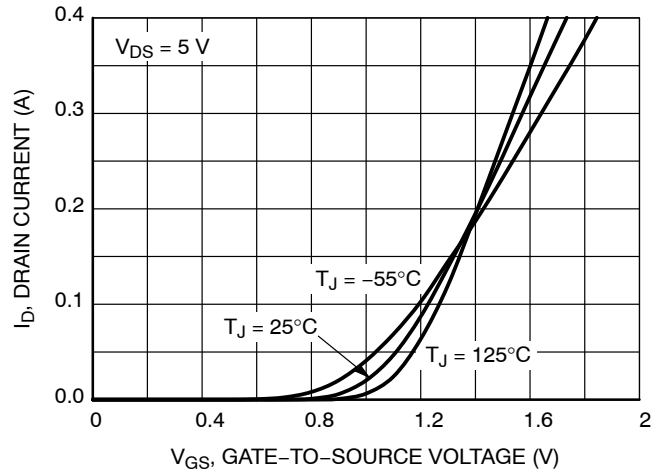


Figure 2. Transfer Characteristics

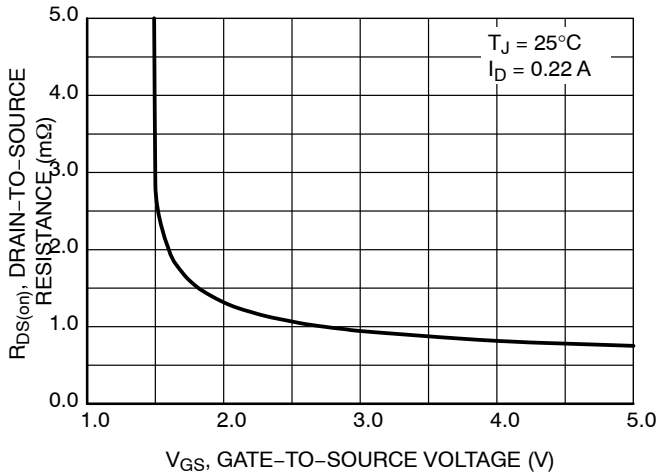


Figure 3. On-Resistance vs. Gate-to-Source Voltage

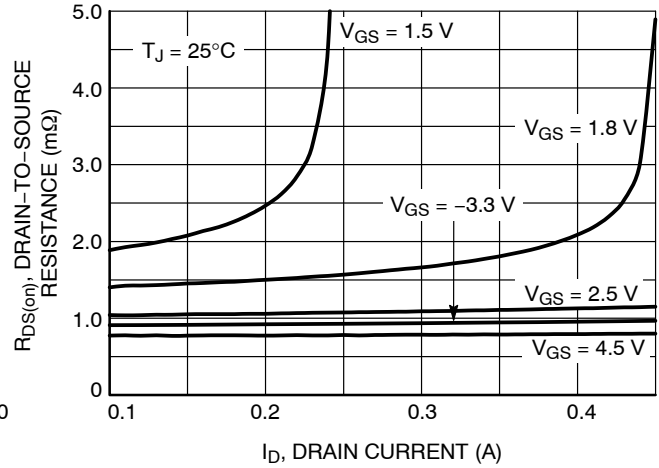


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

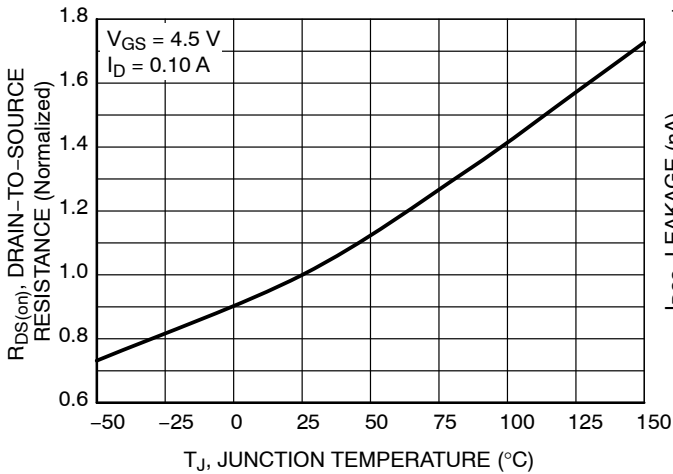


Figure 5. On-Resistance Variation with Temperature

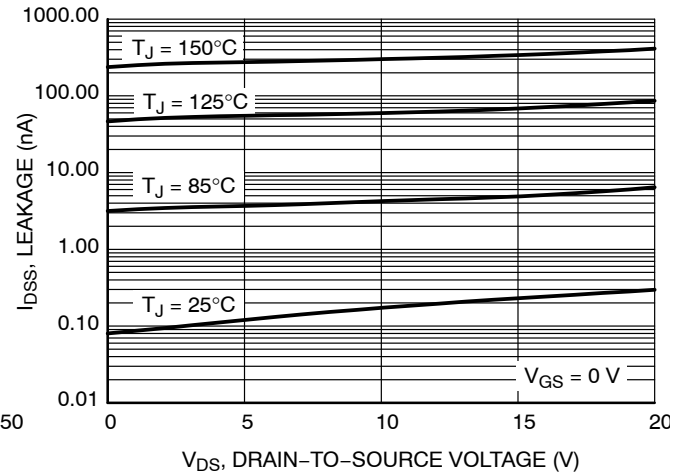


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

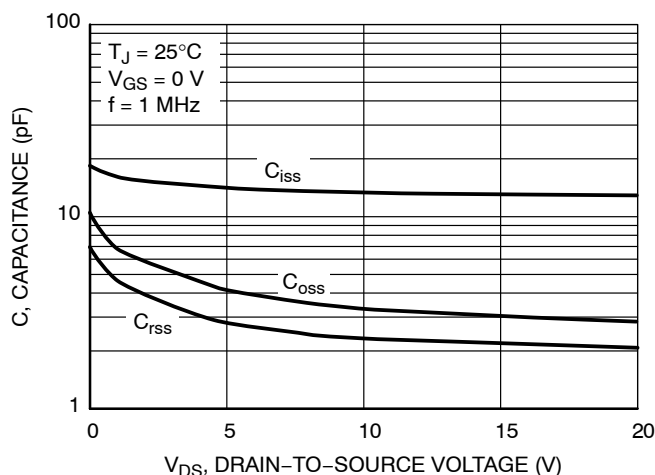


Figure 7. Capacitance Variation

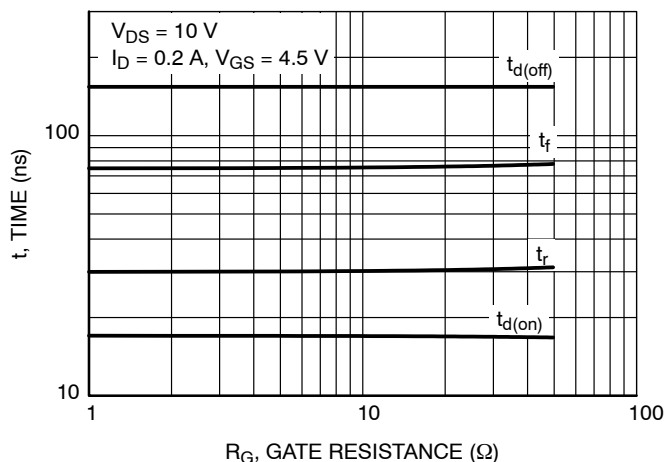


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

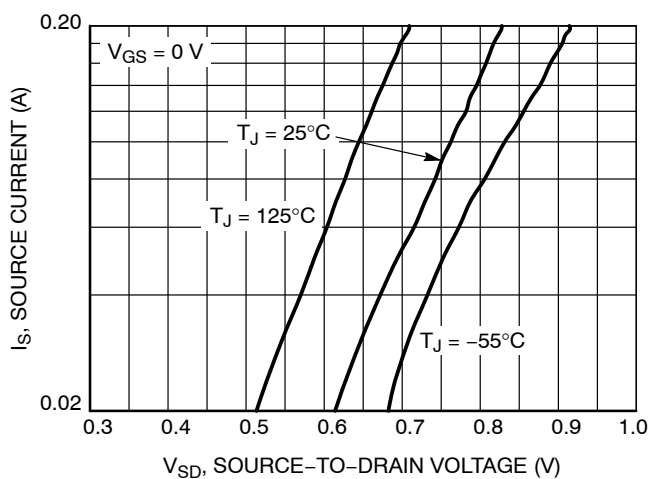


Figure 9. Diode Forward Voltage vs. Current

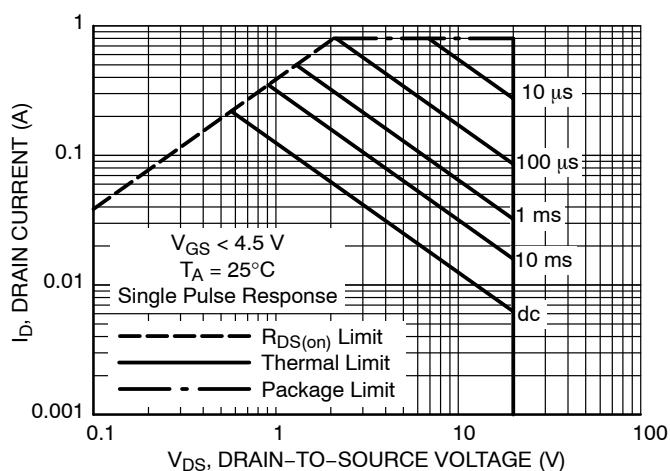


Figure 10. Maximum Rated Forward Biased Safe Operating Area

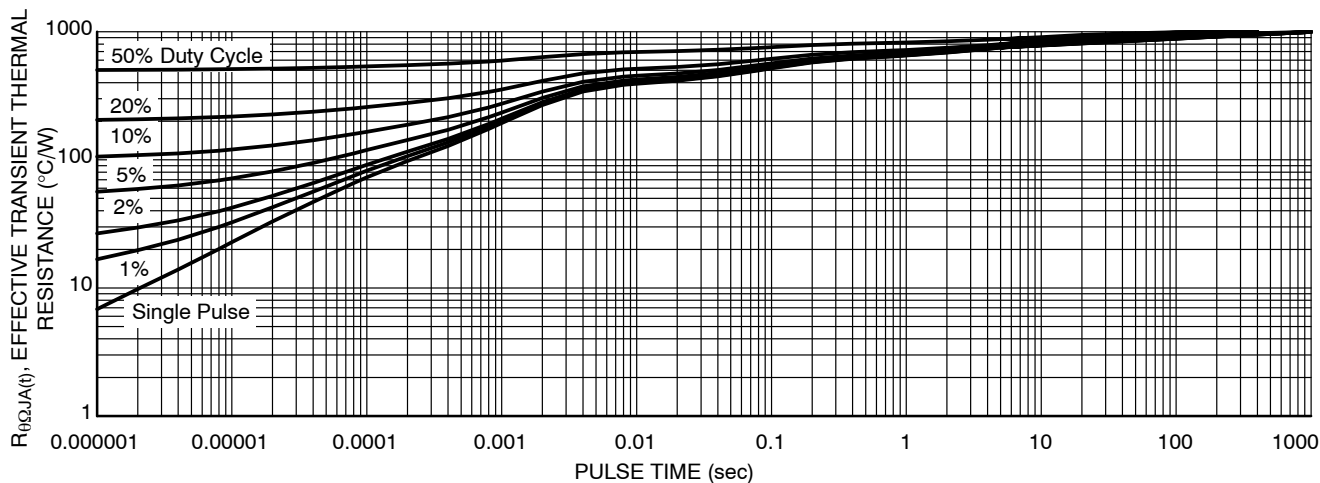
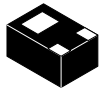


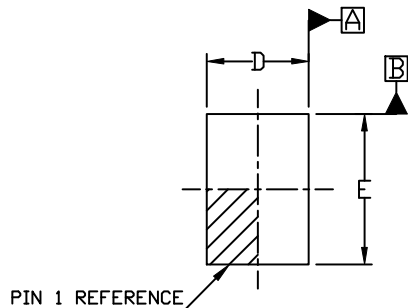
Figure 11. Thermal Response



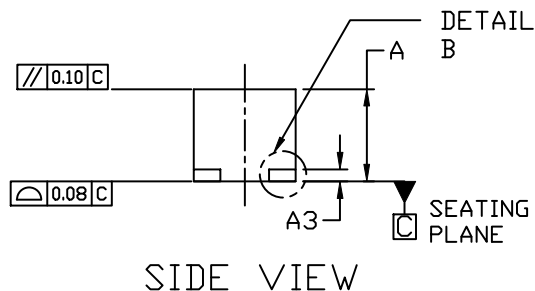
SCALE 8:1

XDFN3 0.42x0.62, 0.3P
CASE 711BH
ISSUE A

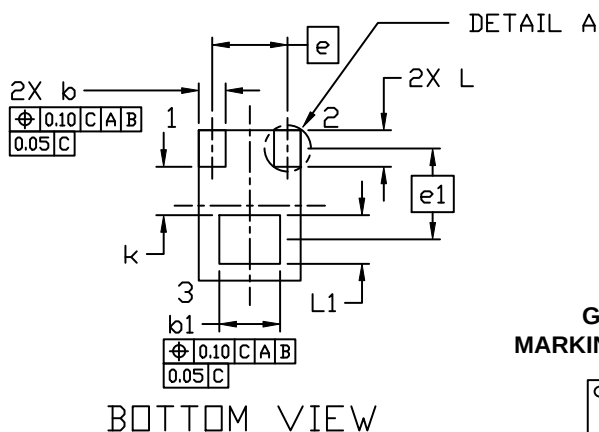
DATE 29 APR 2018



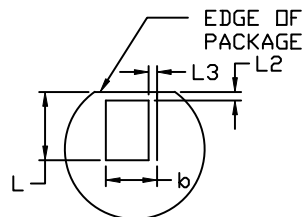
TOP VIEW



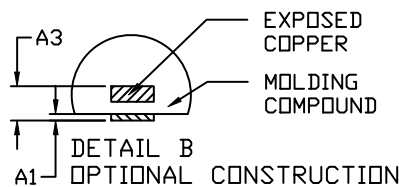
SIDE VIEW



BOTTOM VIEW



DETAIL A
OPTIONAL
CONSTRUCTION



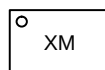
DETAIL B
OPTIONAL CONSTRUCTION

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b AND b1 APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.20 AND 0.25 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE PLATED TERMINALS.

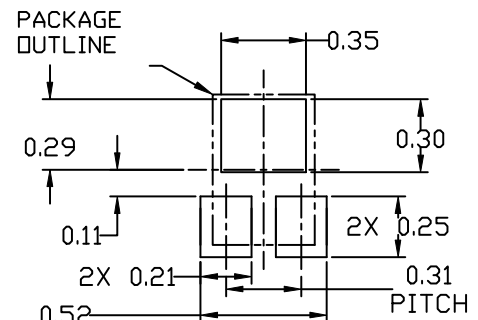
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.33	0.38	0.43
A1	---	---	0.07
A3	0.13 REF		
b	0.05	0.11	0.17
b1	0.20	0.25	0.30
D	0.32	0.42	0.52
E	0.52	0.62	0.72
e	0.30 BSC		
e1	0.38 BSC		
L	0.09	0.15	0.21
L1	0.15	0.20	0.25
L2	---	---	0.03
L3	---	---	0.03
k	0.20 REF		

**GENERIC
MARKING DIAGRAM***



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present. Some products may not follow the Generic Marking.



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DESCRIPTION:	XDFN3 0.42x0.62, 0.3P	PAGE 1 OF 1

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