

NTLJS4114N

MOSFET – Power, Single, N-Channel, μ Cool, WDFN, 2X2 mm 30 V, 7.8 A

Features

- WDFN Package Provides Exposed Drain Pad for Excellent Thermal Conduction
- 2x2 mm Footprint Same as SC-88
- Lowest $R_{DS(on)}$ in 2x2 mm Package
- 1.8 V $R_{DS(on)}$ Rating for Operation at Low Voltage Logic Level Gate Drive
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- This is a Pb-Free Device

Applications

- DC-DC Conversion
- Boost Circuits for LED Backlights
- Optimized for Battery and Load Management Applications in Portable Equipment such as, Cell Phones, PDA's, Media Players, etc.
- Low Side Load Switch for Noisy Environment

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	30	V
Gate-to-Source Voltage			V _{GS}	±12	V
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	6.0	A
		T _A = 85°C		4.4	
		t ≤ 5 s		T _A = 25°C	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.92	W
	t ≤ 5 s			3.3	
Continuous Drain Current (Note 2)	Steady State	T _A = 25°C	I _D	3.6	A
		T _A = 85°C		2.6	
Power Dissipation (Note 2)		T _A = 25°C	P _D	0.70	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	28	A
Operating Junction and Storage Temperature			T _J , T _{STG}	−55 to 150	°C
Source Current (Body Diode) (Note 2)			I _S	3.0	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

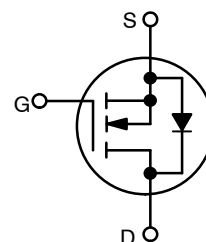
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



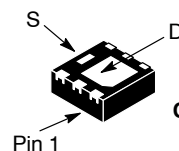
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX (Note 1)
30 V	35 m Ω @ 4.5 V	7.8 A
	45 m Ω @ 2.5 V	
	55 m Ω @ 1.8 V	

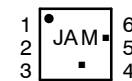


N-CHANNEL MOSFET



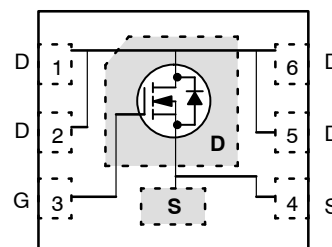
WDFN6
CASE 506AP
STYLE 1

MARKING DIAGRAM



JA = Specific Device Code
M = Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NTLJS4114NT1G	WDFN6 (Pb-Free)	3000/Tape & Reel
NTLJS4114NTAG	WDFN6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTLJS4114N

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm², 2 oz Cu.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	65	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	38	
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	180	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$, Ref to 25°C		20		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 85^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	0.4	0.55	1.0	V
Negative Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.18		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 2.0\text{ A}$		20.3	35	m Ω
		$V_{GS} = 2.5\text{ V}, I_D = 2.0\text{ A}$		25.8	45	
		$V_{GS} = 1.8\text{ V}, I_D = 1.8\text{ A}$		35.2	55	
Forward Transconductance	g_{FS}	$V_{DS} = 16\text{ V}, I_D = 2.0\text{ A}$		8		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 15\text{ V}$		650		pF
Output Capacitance	C_{OSS}			115.5		
Reverse Transfer Capacitance	C_{RSS}			70		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 2.0\text{ A}$		8.5	13	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.6		
Gate-to-Source Charge	Q_{GS}			0.9		
Gate-to-Drain Charge	Q_{GD}			2.1		
Gate Resistance	R_G			3.0		Ω

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 15\text{ V}, I_D = 2.0\text{ A}, R_G = 3.0\text{ }\Omega$		5		ns
Rise Time	t_r			9		
Turn-Off Delay Time	$t_{d(OFF)}$			20		
Fall Time	t_f			4		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Recovery Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 2.0\text{ A}$	$T_J = 25^\circ\text{C}$		0.71	1.2	V
			$T_J = 85^\circ\text{C}$		0.58		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}, I_S = 1.0\text{ A}$		14	35	ns	
Charge Time	t_a			8.0			
Discharge Time	t_b			6.0			
Reverse Recovery Time	Q_{RR}			5.0		nC	

5. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

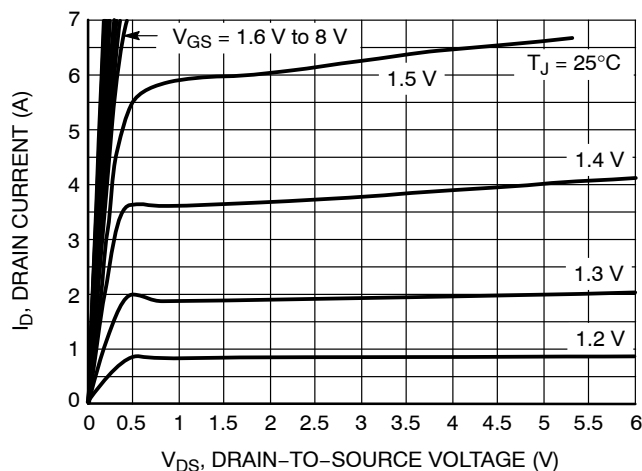


Figure 1. On-Region Characteristics

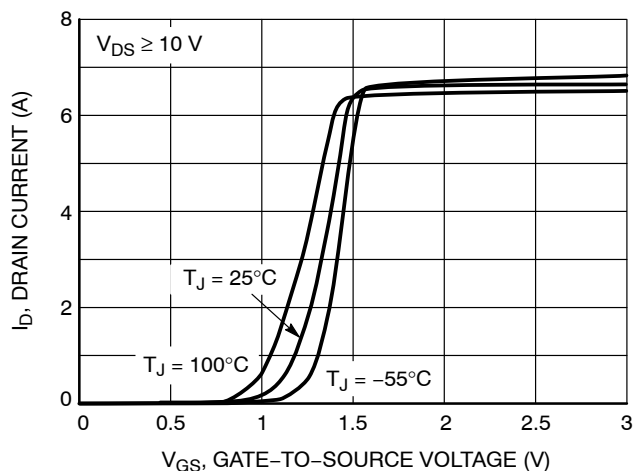


Figure 2. Transfer Characteristics

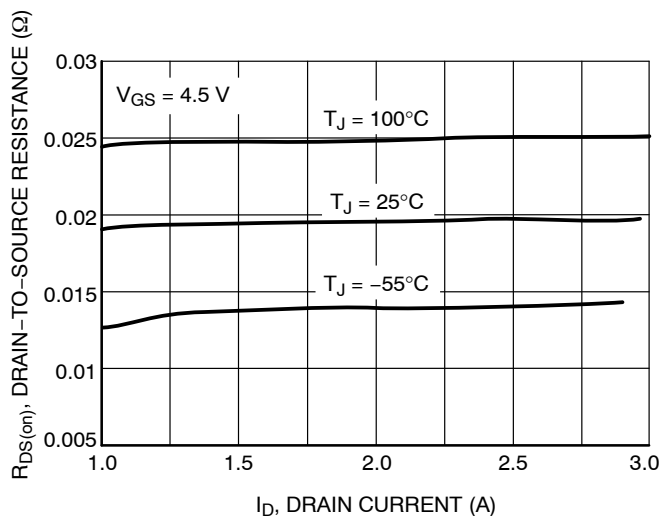


Figure 3. On-Resistance versus Drain Current

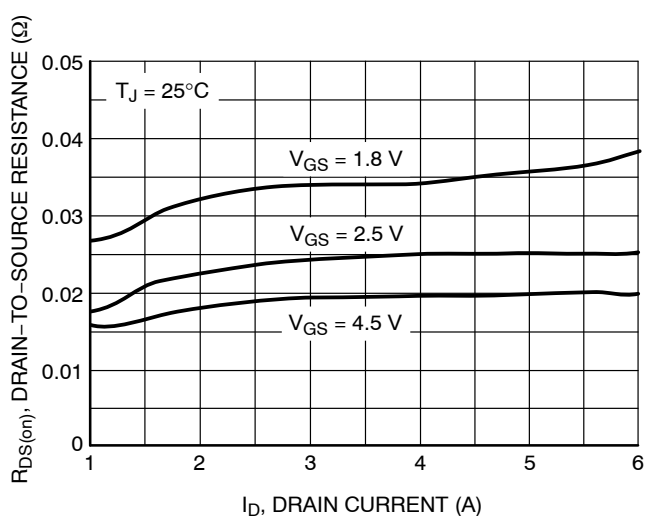


Figure 4. On-Resistance versus Drain Current and Gate Voltage

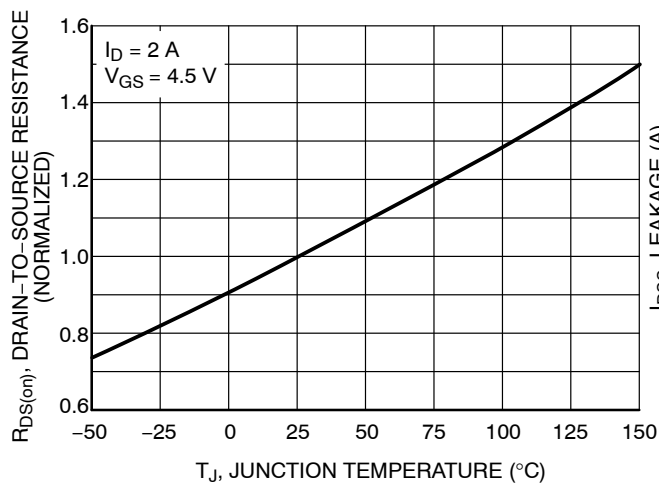


Figure 5. On-Resistance Variation with Temperature

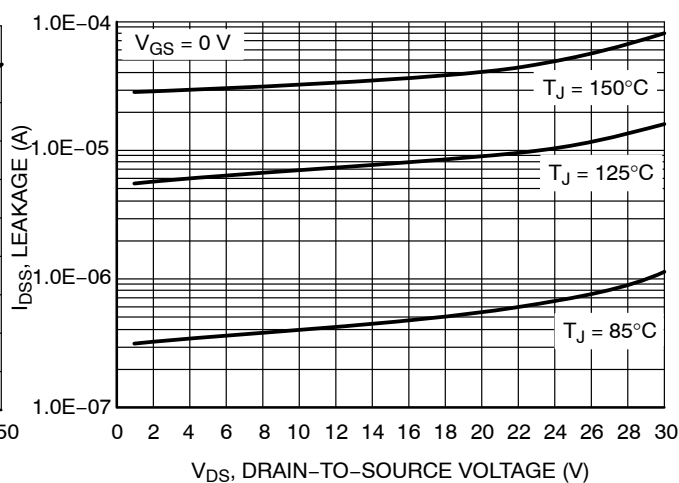


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

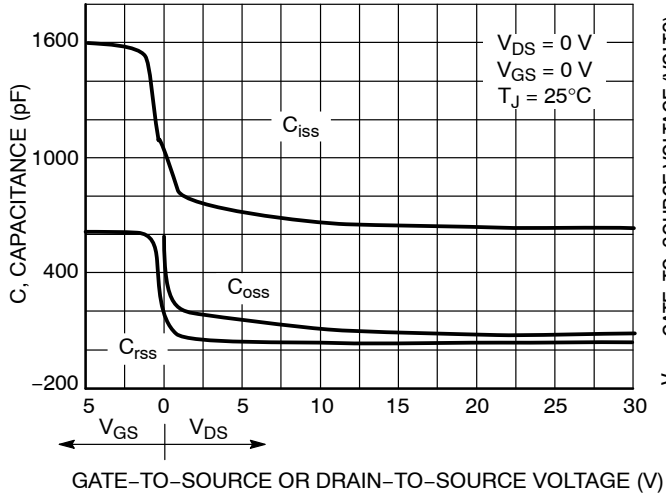


Figure 7. Capacitance Variation

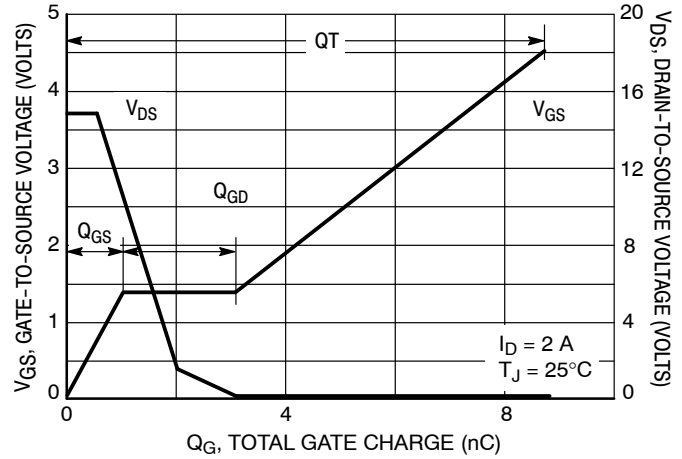


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

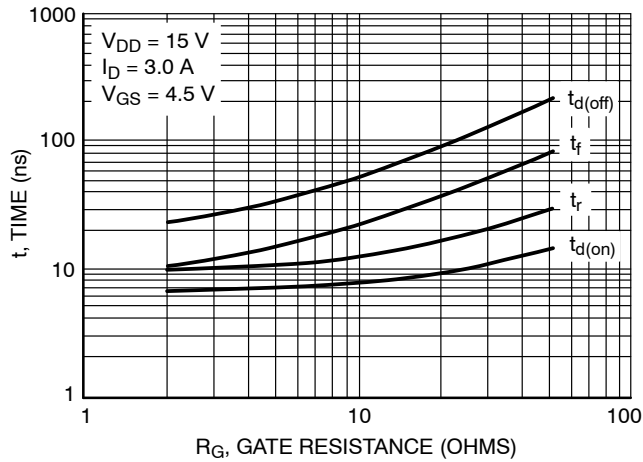


Figure 9. Resistive Switching Time Variation versus Gate Resistance

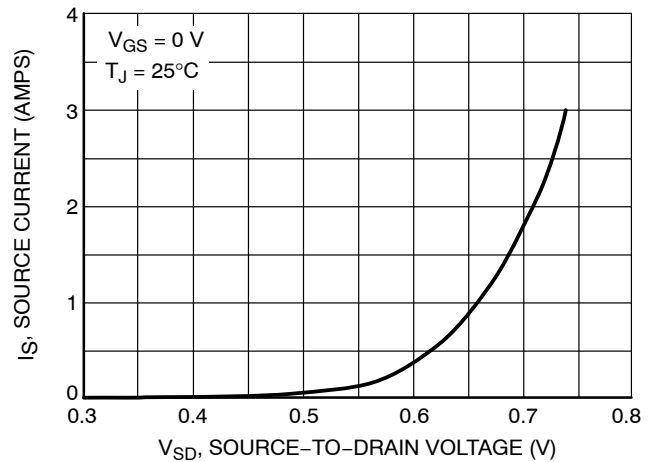


Figure 10. Diode Forward Voltage versus Current

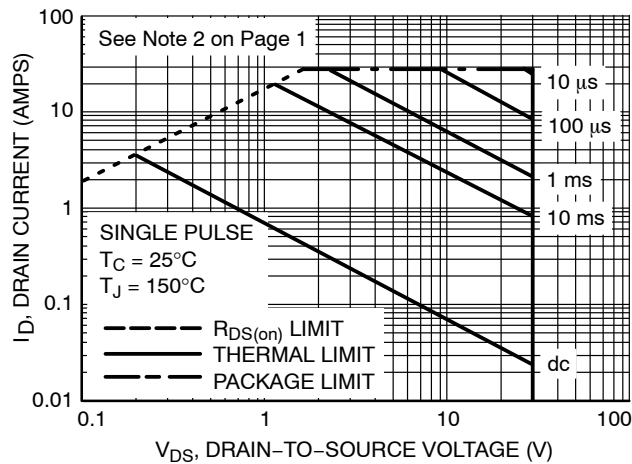


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTLJS4114N

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

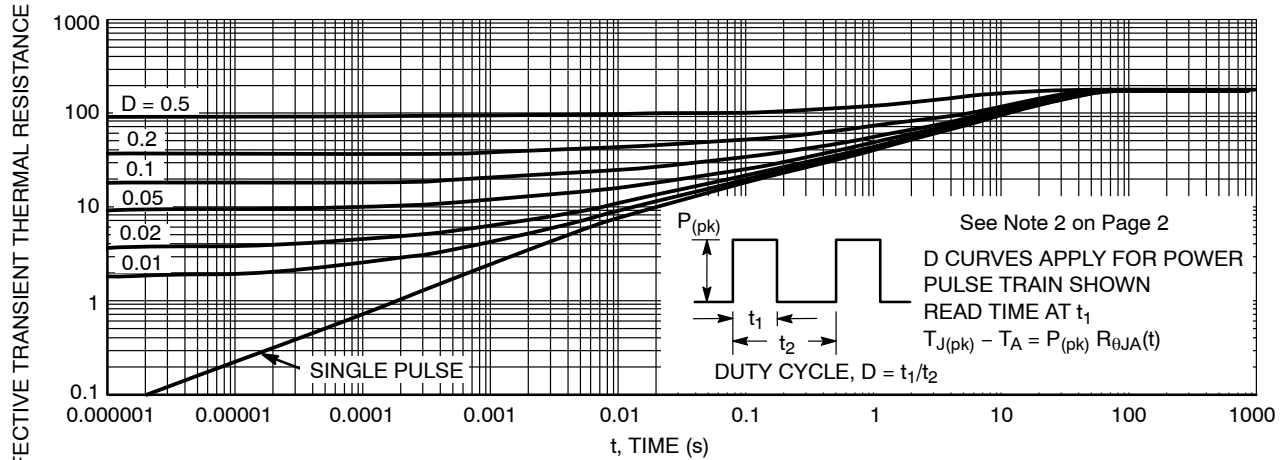


Figure 12. Thermal Response



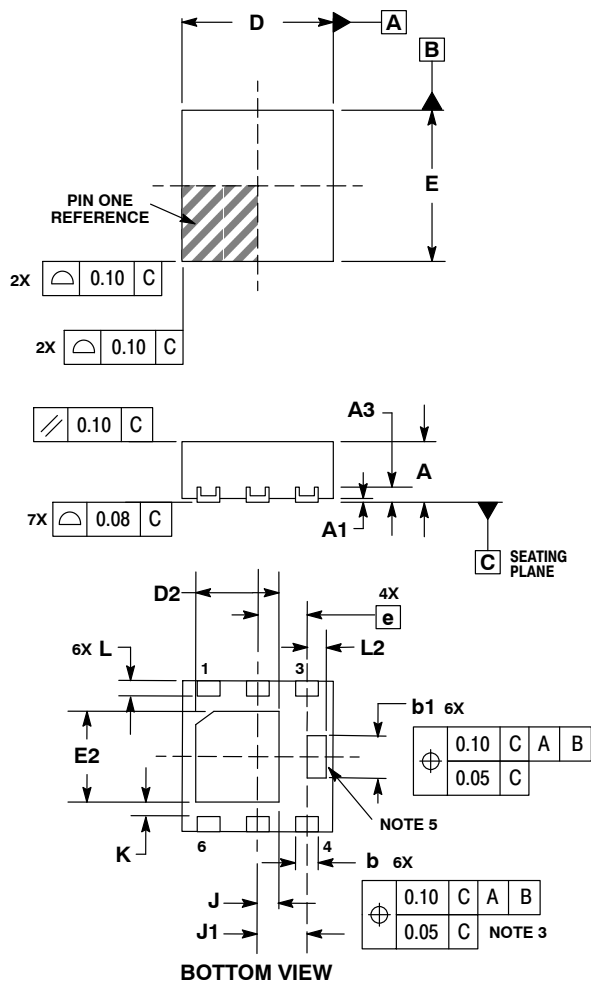
SCALE 4:1

WDFN6 2x2

CASE 506AP-01

ISSUE B

DATE 26 APR 2006

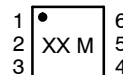


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
1. CENTER TERMINAL LEAD IS OPTIONAL. TERMINAL LEAD IS CONNECTED TO TERMINAL LEAD # 4.
2. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
L	0.20	0.30
L2	0.20	0.30
J	0.27 REF	
J1	0.65 REF	

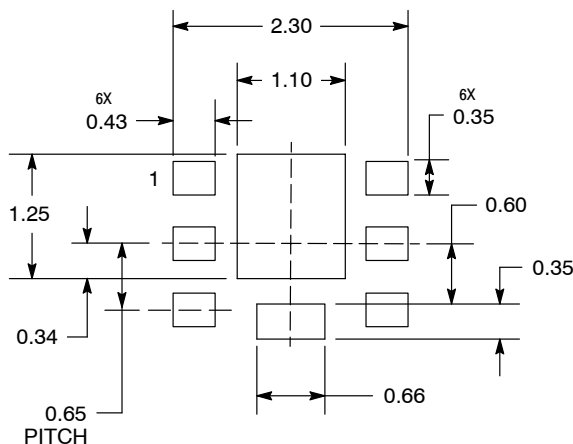
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1: DRAIN
2: DRAIN
3: GATE
4: SOURCE
5: DRAIN
6: DRAIN

STYLE 2:
PIN 1: COLLECTOR
2: COLLECTOR
3: BASE
4: EMITTER
5: COLLECTOR
6: COLLECTOR

DOCUMENT NUMBER:	98AON20860D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	6 PIN WDFN 2X2, 0.65P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales