

NTP30N06L, NTB30N06L

Power MOSFET

30 Amps, 60 Volts, Logic Level, N-Channel TO-220 and D²PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Pb-Free Packages are Available

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	60	Vdc
Drain-to-Gate Voltage (R _{GS} = 10 MΩ)	V _{DGR}	60	Vdc
Gate-to-Source Voltage	V _{GS}	± 15	Vdc
– Continuous	V _{GS}	± 20	Vdc
– Non-Repetitive (t _p ≤ 10 ms)			
Drain Current	I _D	30	A _{dc}
– Continuous @ T _A = 25°C	I _D	15	A _{dc}
– Continuous @ T _A = 100°C	I _{DM}	90	A _{pk}
– Single Pulse (t _p ≤ 10 μs)			
Total Power Dissipation @ T _A = 25°C	P _D	88.2	W
Derate above 25°C		0.59	W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	–55 to +175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T _J = 25°C (V _{DD} = 50 Vdc, V _{GS} = 5.0 Vdc, L = 0.3 mH I _{L(pk)} = 26 A, V _{DS} = 60 Vdc)	E _{AS}	101	mJ
Thermal Resistance, Junction-to-Case	R _{θJC}	1.7	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	T _L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

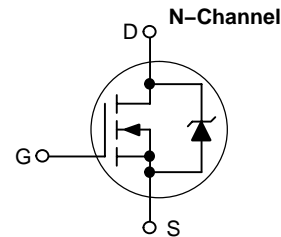


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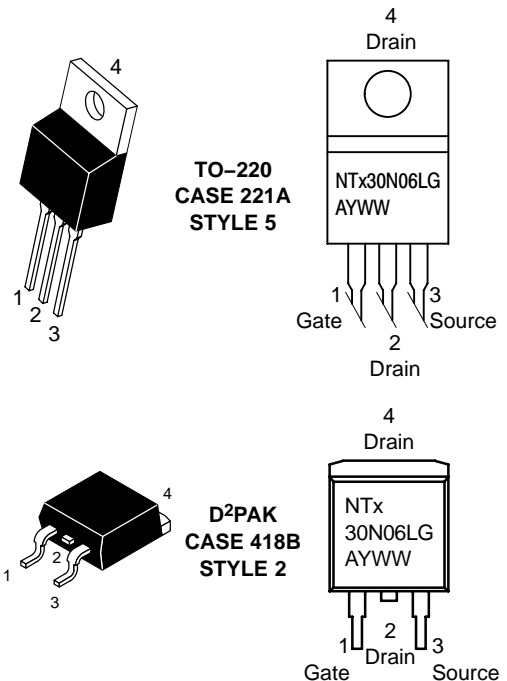
<http://onsemi.com>

30 AMPERES, 60 VOLTS

R_{DS(on)} = 46 mΩ



MARKING DIAGRAMS



NTx30N06L = Device Code
 x = P or B
 A = Assembly Location
 Y = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTP30N06L, NTB30N06L

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 1) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	60 –	71.8 69	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±15 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	±100	nAdc

ON CHARACTERISTICS (Note 1)

Gate Threshold Voltage (Note 1) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.7 4.8	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 1) (V _{GS} = 5.0 Vdc, I _D = 15 Adc)	R _{DS(on)}	–	38	46	mΩ
Static Drain-to-Source On-Voltage (Note 1) (V _{GS} = 5.0 Vdc, I _D = 30 Adc) (V _{GS} = 5.0 Vdc, I _D = 15 Adc, T _J = 150°C)	V _{DS(on)}	– –	1.3 1.06	1.7 –	Vdc
Forward Transconductance (Note 1) (V _{DS} = 7.0 Vdc, I _D = 15 Adc)	g _{FS}	–	21	–	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	810	1150	pF
Output Capacitance		C _{oss}	–	260	370	
Transfer Capacitance		C _{rss}	–	80	115	

SWITCHING CHARACTERISTICS (Note 2)

Turn-On Delay Time	(V _{DD} = 30 Vdc, I _D = 30 Adc, V _{GS} = 5.0 Vdc, R _G = 9.1 Ω) (Note 1)	t _{d(on)}	–	10	20	ns
Rise Time		t _r	–	200	400	
Turn-Off Delay Time		t _{d(off)}	–	15.6	30	
Fall Time		t _f	–	62	120	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 30 Adc, V _{GS} = 5.0 Vdc) (Note 1)	Q _T	–	16	32	nC
		Q ₁	–	3.9	–	
		Q ₂	–	10	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 30 Adc, V _{GS} = 0 Vdc) (Note 1) (I _S = 30 Adc, V _{GS} = 0 Vdc, T _J = 150°C)	V _{SD}	– –	1.01 1.03	1.2 –	Vdc
Reverse Recovery Time	(I _S = 30 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) (Note 1)	t _{rr}	–	50	–	ns
		t _a	–	32	–	
		t _b	–	17	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.082	–	μC

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperatures.

NTP30N06L, NTB30N06L

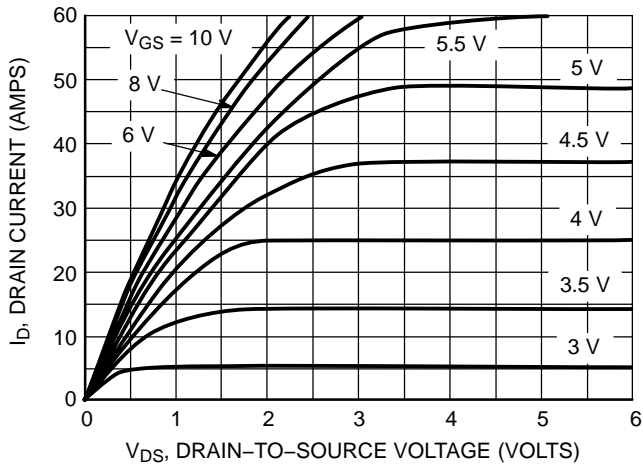


Figure 1. On-Region Characteristics

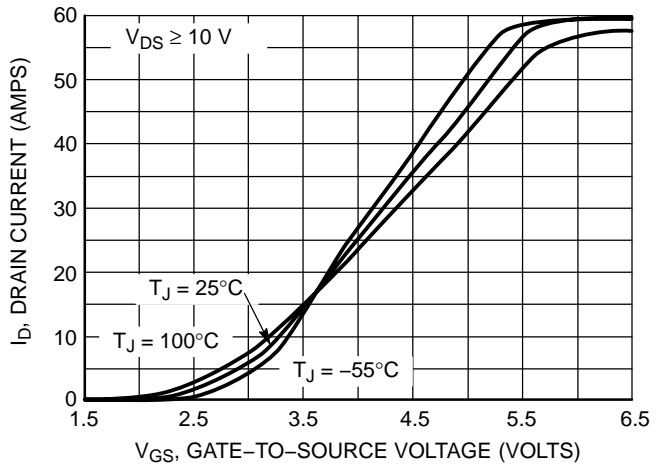


Figure 2. Transfer Characteristics

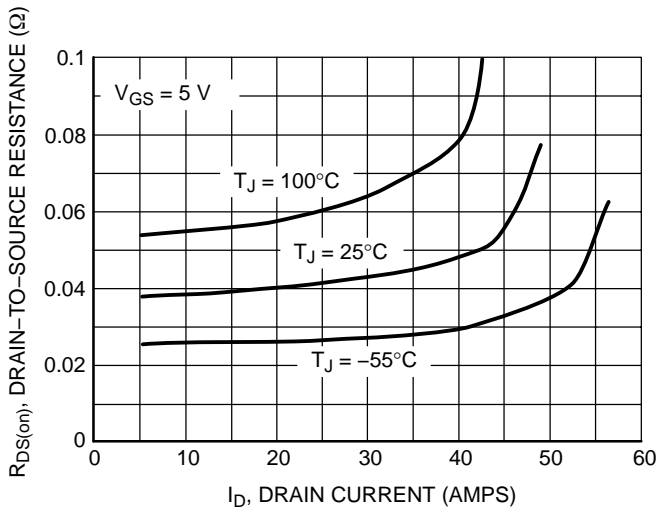


Figure 3. On-Resistance versus Gate-to-Source Voltage

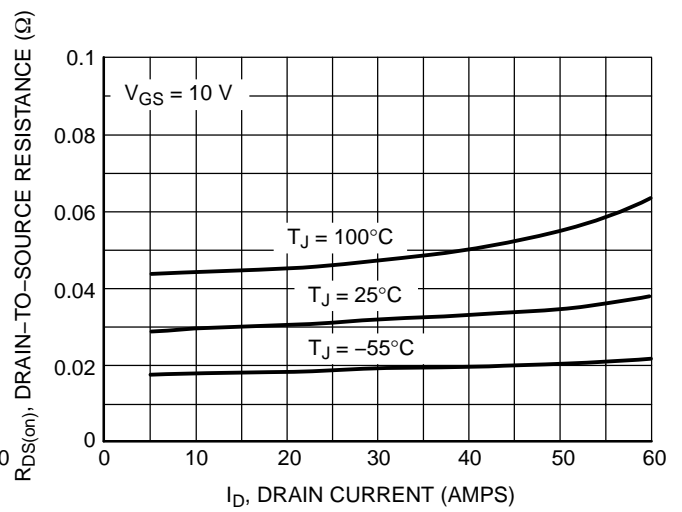


Figure 4. On-Resistance versus Drain Current and Gate Voltage

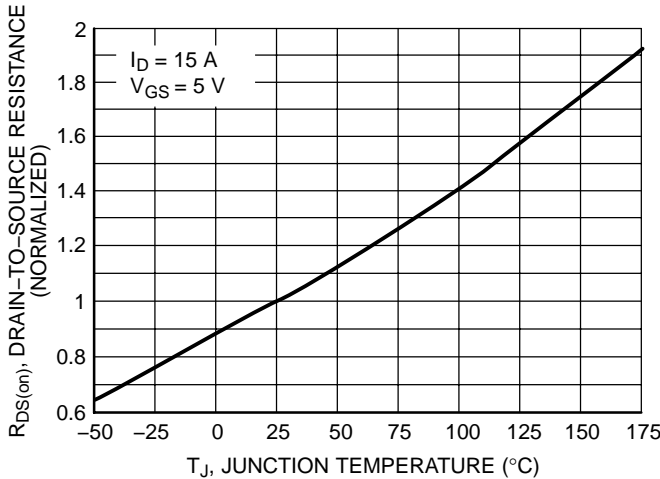


Figure 5. On-Resistance Variation with Temperature

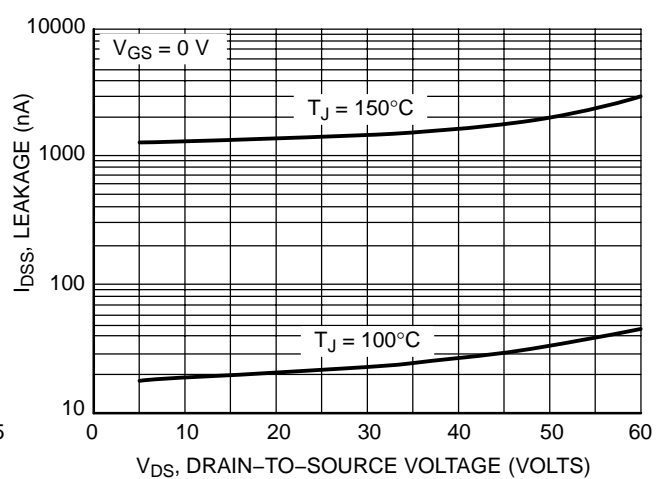


Figure 6. Drain-to-Source Leakage Current versus Voltage

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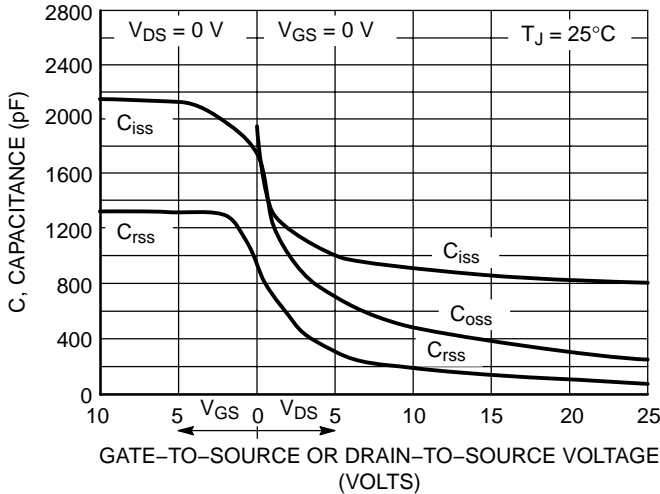


Figure 7. Capacitance Variation

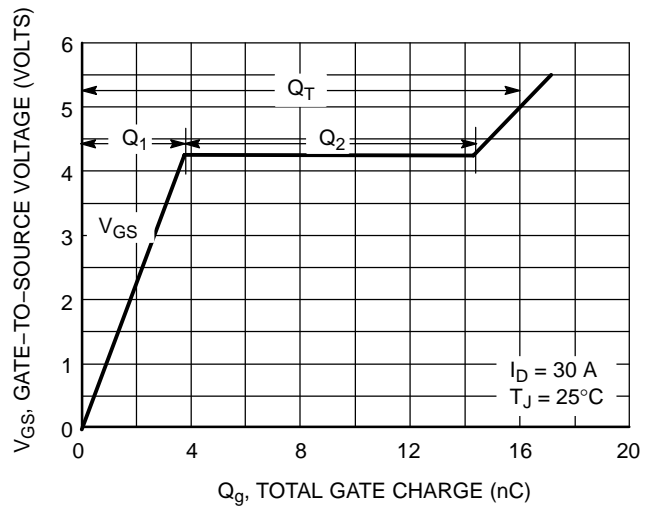


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

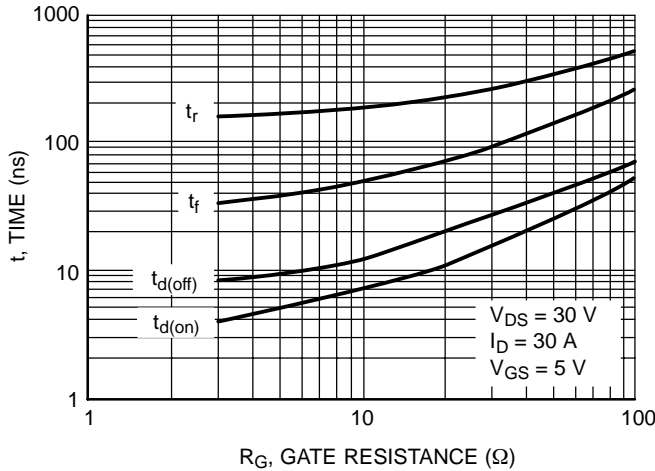


Figure 9. Resistive Switching Time Variation versus Gate Resistance

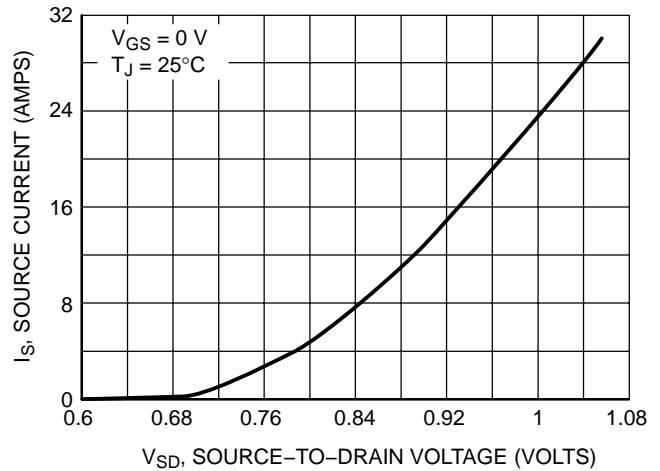


Figure 10. Diode Forward Voltage versus Current

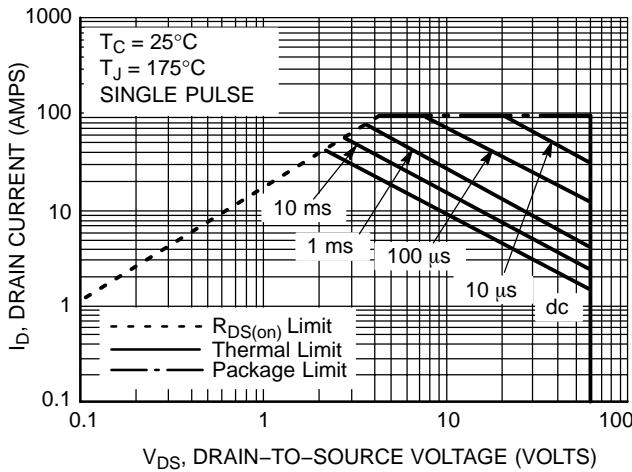


Figure 11. Maximum Rated Forward Biased Safe Operating Area

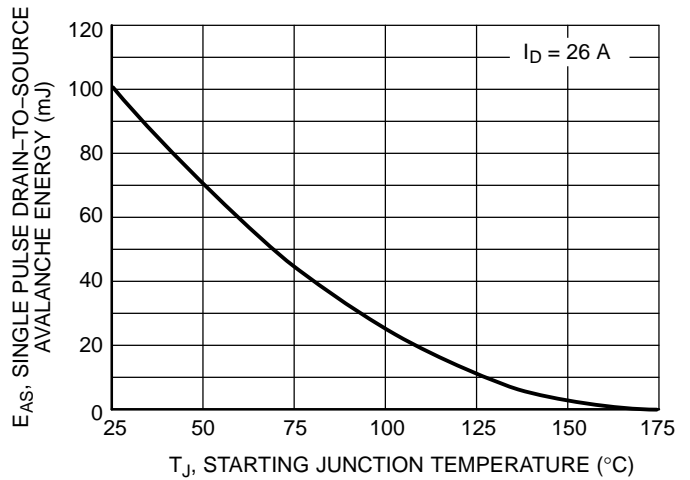


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

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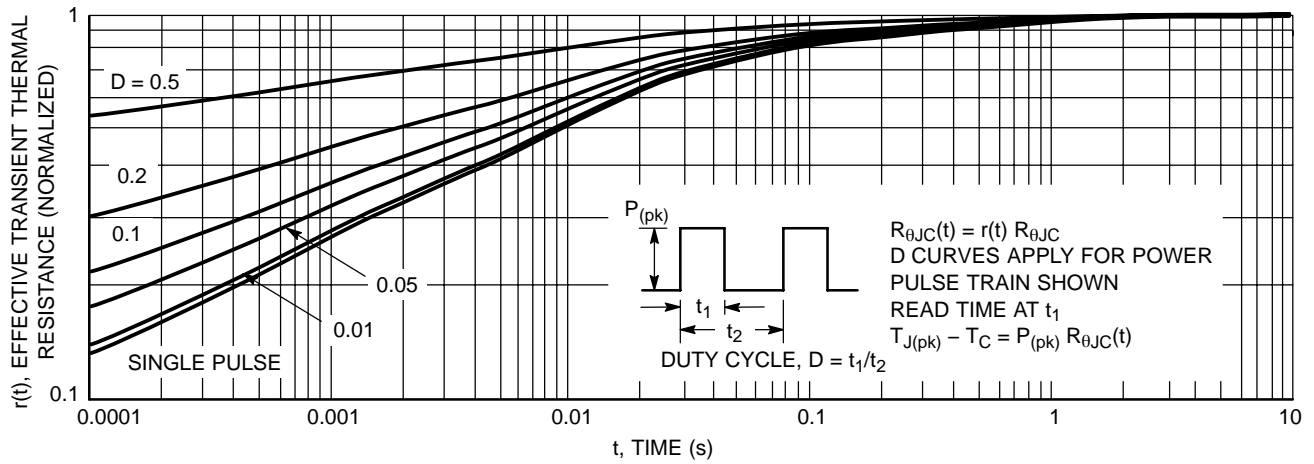


Figure 13. Thermal Response

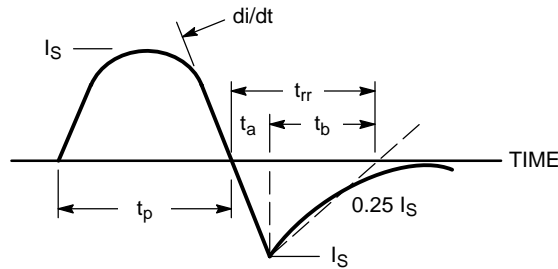


Figure 14. Diode Reverse Recovery Waveform

ORDERING INFORMATION

Device	Package	Shipping†
NTP30N06L	TO-220	50 Units / Rail
NTP30N06LG	TO-220 (Pb-Free)	50 Units / Rail
NTB30N06L	D ² PAK	50 Units / Rail
NTB30N06LG	D ² PAK (Pb-Free)	50 Units / Rail
NTB30N06LT4	D ² PAK	800 Tape & Reel
NTB30N06LT4G	D ² PAK (Pb-Free)	800 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

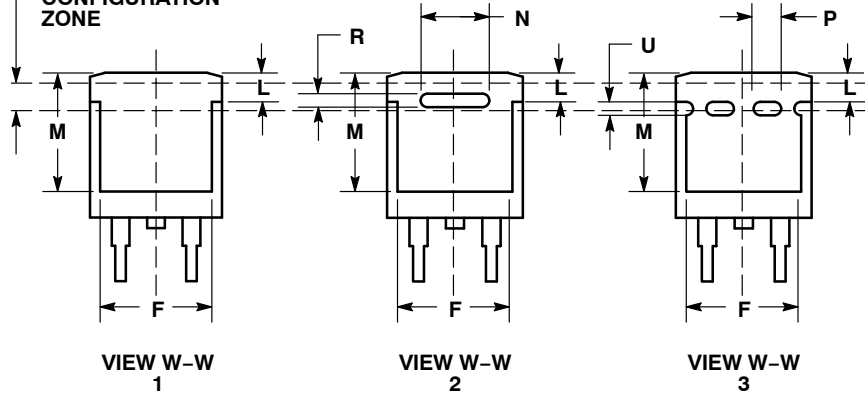


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE CONFIGURATION ZONE



- | | | | | | |
|--|---|---|--|---|--|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE | STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE |
|--|---|---|--|---|--|

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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

**GENERIC
MARKING DIAGRAM***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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