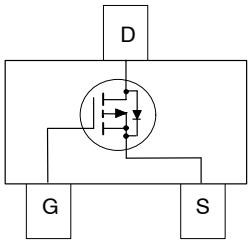
P-Channel Enhancement Mode Field Effect Transistor

NDS0610

SOT−23
CASE 318−08



General Description

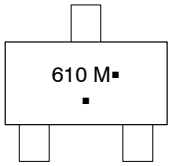
This P−Channel Enhancement Mode Field Effect Transistors are Produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on−state resistance, provide rugged and reliable performance and fast switching. They can be used, with a minimum of effort, in most applications requiring up to 120 mA DC and can deliver current up to 1 A.

This product is particularly suited to low voltage applications requiring a low current high side switch.

Features

- −0.12 A, −60 V
  - $R_{DS(on)}$ = 10 Ω @ V_{GS} = −10 V
  - $R_{DS(on)}$ = 20 Ω @ V_{GS} = −4.5 V
- Voltage Controlled P−Channel Small Signal Switch
- High Density Cell design for Low $R_{DS(on)}$
- High Saturation Current

MARKING DIAGRAM



610 = Device Code
M = Date Code*
▪ = Pb−Free Package

(NOTE: Microdot may be in either location)

*Date Code orientation and/or location may vary depending upon manufacturing location.

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Unit
V_{DSS}	Drain−to−Source Voltage	−60	V
V_{GSS}	Gate−to−Source Voltage	±20	V
I_D	Drain Current − Continuous (Note 1) − Pulsed	 −0.12 −1	A
P_D	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above 25°C	2.9	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
NDS0610	SOT−23 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1)	350	°C/W

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = −10 μA	−60	−	−	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −10 μA, Referenced to 25°C	−	−53	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −48 V, V_{GS} = 0 V	−	−	−1	μA
		V_{DS} = −48 V, V_{GS} = 0 V T_J = 125°C	−	−	−200	μA
I_{GSS}	Gate−Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V	−	−	±10	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −1 mA	−1	−1.7	−3.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = −1 mA, Referenced to 25°C	−	−3	−	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = −10 V, I_D = −0.5 A V_{GS} = −4.5 V, I_D = −0.25 A V_{GS} = −10 V, I_D = −0.5 A, T_J = 125°C	−	1.0 1.3 1.7	10 20 16	Ω
$I_{D(on)}$	On−State Drain Current	V_{GS} = −10 V, V_{DS} = −10 V	−0.6	−	−	A
g_{FS}	Forward Transconductance	V_{DS} = −10 V, I_D = −0.1 A	70	430	−	mS
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = −25 V, V_{GS} = 0 V, f = 1.0 MHz	−	79	−	pF
C_{oss}	Output Capacitance		−	10	−	pF
C_{rss}	Reverse Transfer Capacitance		−	4	−	pF
R_G	Gate Resistance	V_{DS} = −15 mV, f = 1.0 MHz	−	10	−	Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −25 V, I_D = −0.12 A, V_{GS} = −10 V, R_{GEN} = 6 Ω	−	2.5	5	ns
t_r	Turn−On Rise Time		−	6.3	12.6	ns
$t_{d(off)}$	Turn−Off Delay Time		−	10	15	ns
t_f	Turn−Off Fall Time		−	7.5	15	ns
Q_g	Total Gate Change	V_{DS} = −48 V, I_D = −0.5 A, V_{GS} = −10 V	−	1.8	2.5	nC
Q_{gs}	Gate−Source Change		−	0.3	−	nC
Q_{gd}	Gate−Drain Change		−	0.4	−	nC
Drain−Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain−Source Diode Forward Current		−	−	−0.24	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −0.24 A (Note 2)	−	−0.8	−1.5	V
t_{rr}	Diode Reverse Recovery Time	I_F = −0.5 A, d_{iF}/d_t = 100 A/μs (Note 2)	−	17	−	ns
Q_{rr}	Diode Reverse Recovery Charge		−	15	−	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 350 °C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

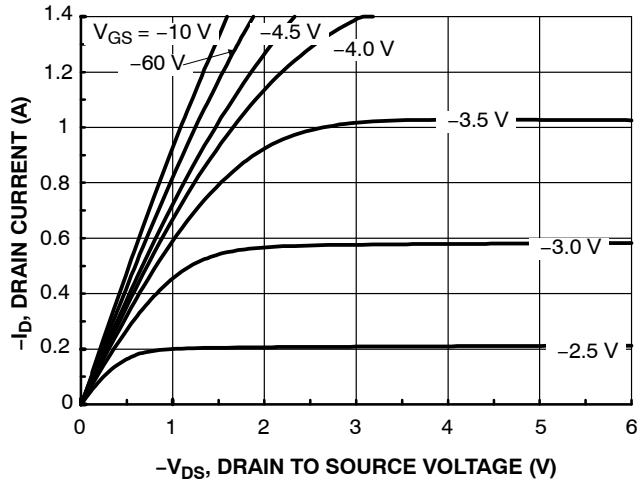


Figure 1. On−Region Characteristics

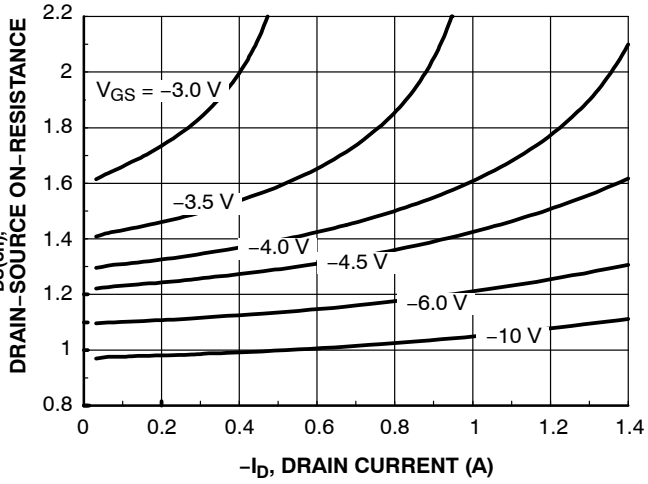


Figure 2. On−Resistance Variation With Drain Current and Gate Voltage

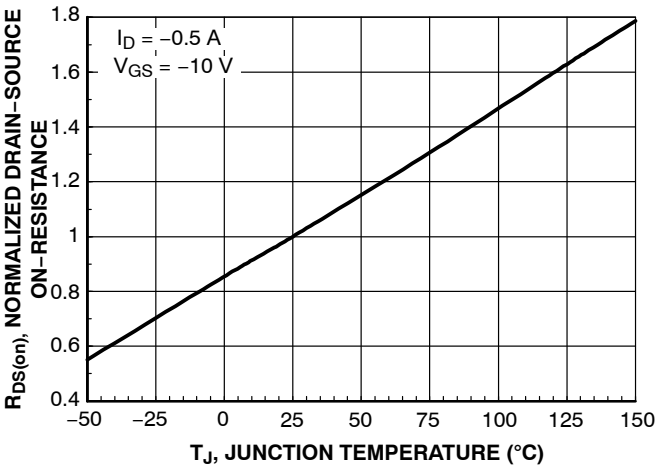


Figure 3. On−Resistance Variation with Temperature

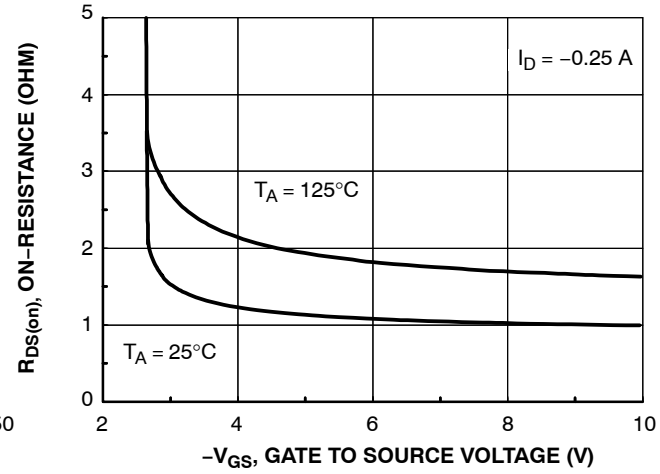


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

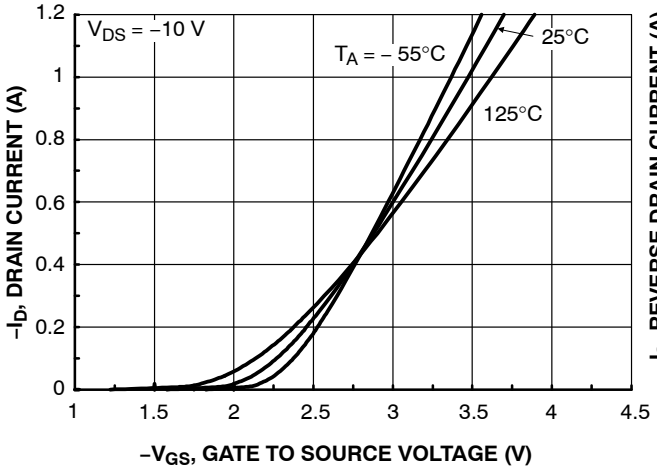


Figure 5. Transfer Characteristics

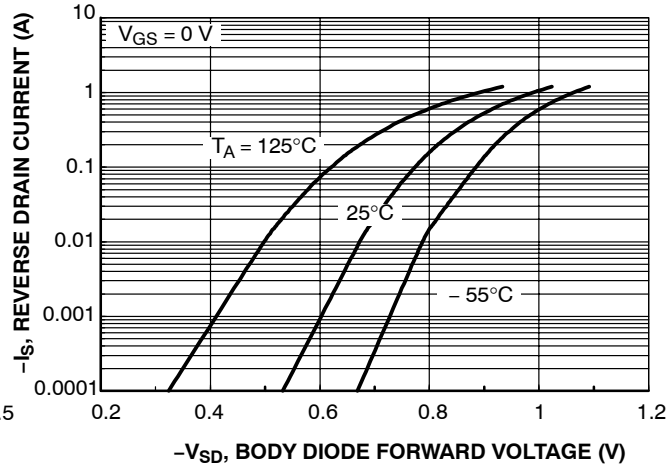


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

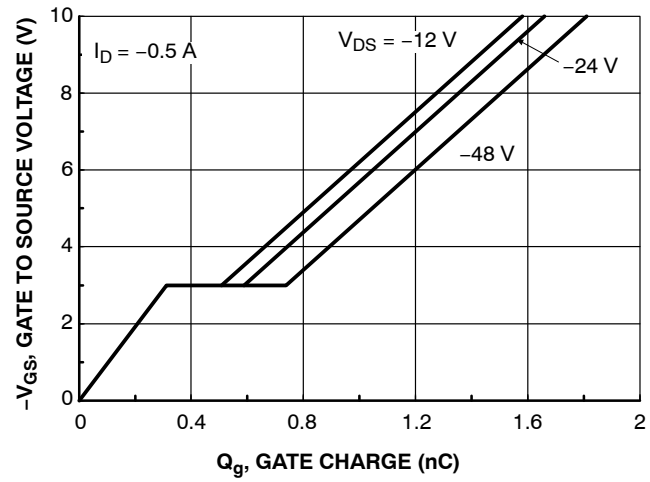


Figure 7. Gate Charge Characteristics

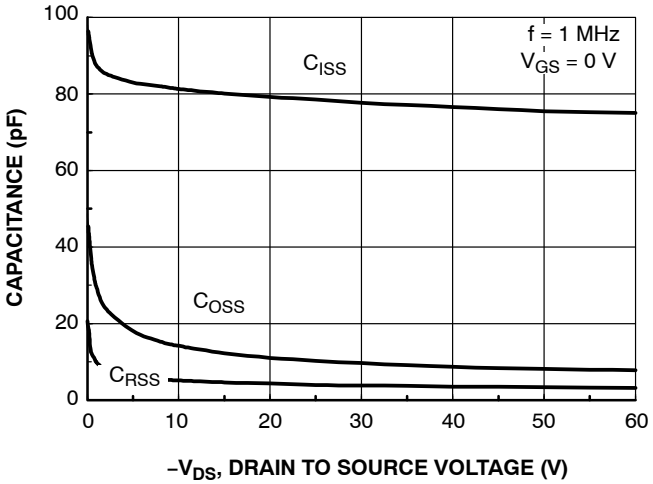


Figure 8. Capacitance Characteristics

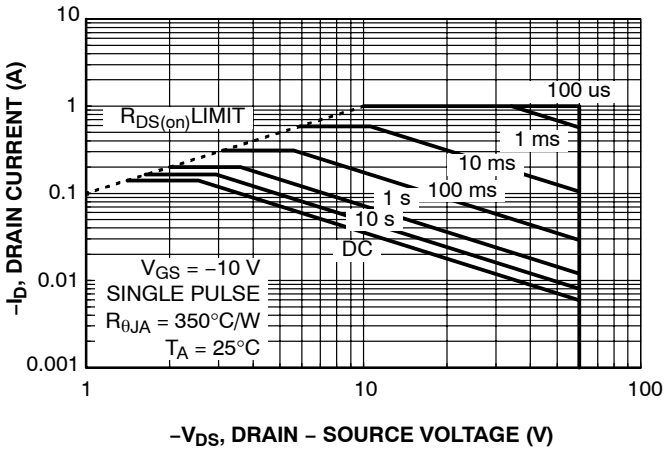


Figure 9. Maximum Safe Operating Area

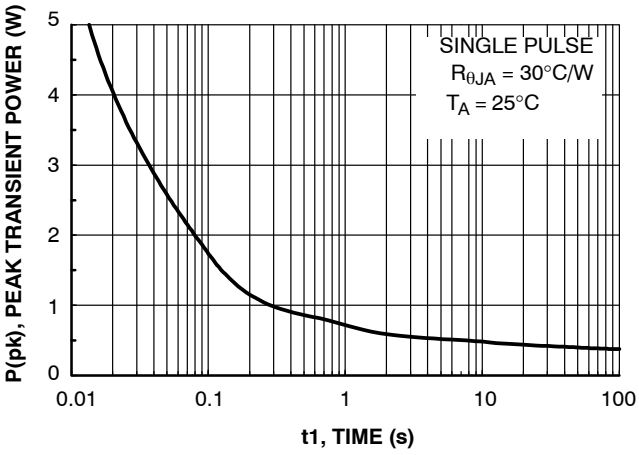


Figure 10. Single Pulse Maximum Power Dissipation

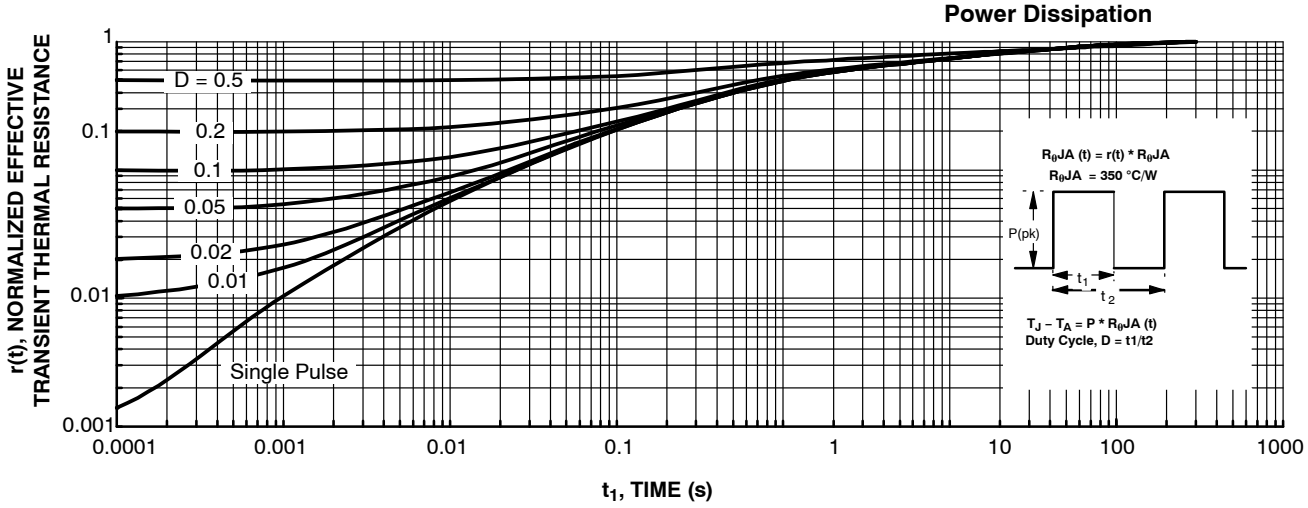
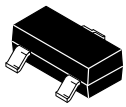


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1a.
Transient themal response will change depending on the circuit board design.

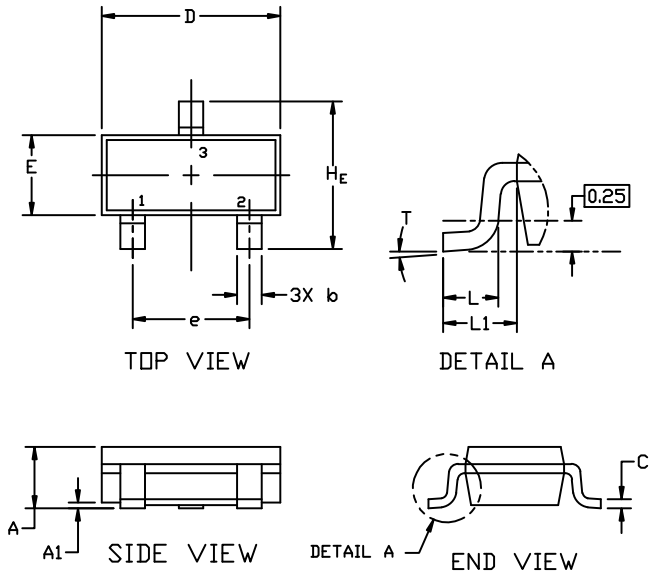
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

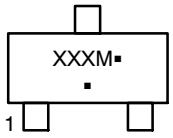


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

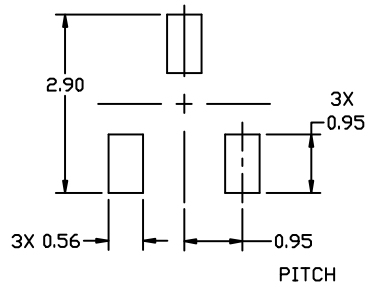
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

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