

# MOSFET – N-Channel QFET

900 V, 11.4 A, 960 mΩ

## FQA11N90-F109

### Description

This N-Channel Enhancement Mode Power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

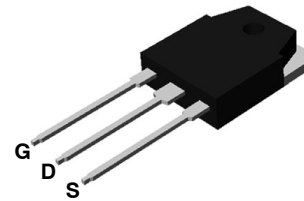
### Features

- 11.4 A, 900 V,  $R_{DS(on)} = 960 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 5.7 \text{ A}$
- Low Gate Charge (Typ. 72 nC)
- Low  $C_{rss}$  (Typ. 30 pF)
- 100% Avalanche Tested
- This Device is Pb-Free Halide, Free and RoHS Compliant

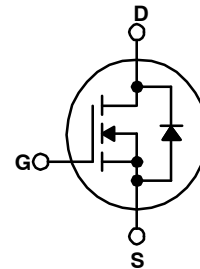
### MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain to Source Voltage	900	V
$I_D$	Drain Current – Continuous ( $T_C = 25^\circ\text{C}$ ) – Continuous ( $T_C = 100^\circ\text{C}$ )	11.4 7.2	A
$I_{DM}$	Drain Current – Pulsed (Note 1)	45.6	A
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	1000	mJ
$I_{AR}$	Avalanche Current (Note 1)	11.4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	30	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	4.0	V/ns
$P_D$	Power Dissipation – ( $T_C = 25^\circ\text{C}$ ) – Derate Above $25^\circ\text{C}$	300 2.38	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	$-55$ to $+150$	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



TO-3P-3LD  
CASE 340BZ



### MARKING DIAGRAM

&Z&3&K
FQA
11N90

&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= 2-Digit Lot Code
FQA11N90	= Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
FQA11N90-F109	TO-3P-3LD (Pb-Free)	450 Units / Tube

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

**THERMAL CHARACTERISTICS**

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.42	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	40	

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	900	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	1.0	–	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 900\text{ V}, V_{GS} = 0\text{ V}$	–	–	10	$\mu\text{A}$
	Zero Gate Voltage Drain Current	$V_{DS} = 720\text{ V}, T_C = 125^\circ\text{C}$	–	–	100	$\mu\text{A}$
$I_{GSSF}$	Gate to Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	–	–	100	nA
$I_{GSSR}$	Gate to Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	–	–	-100	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 5.7\text{ A}$	–	0.75	0.96	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 5.7\text{ A}$	–	12	–	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	2700	3500	pF
$C_{oss}$	Output Capacitance		–	260	340	pF
$C_{rss}$	Reverse Transfer Capacitance		–	30	40	pF

**Switching Characteristics**

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 450\text{ V}, I_D = 11.4\text{ A}, R_G = 25\text{ }\Omega$ (Note 4)	–	65	140	ns
$t_r$	Turn–On Rise Time		–	135	280	ns
$t_{d(off)}$	Turn–Off Delay Time		–	165	340	ns
$t_f$	Turn–Off Fall Time		–	90	190	ns
$Q_g$	Total Gate Charge	$V_{DS} = 720\text{ V}, I_D = 11.4\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	–	72	94	nC
$Q_{gs}$	Gate–Source Charge		–	16	–	nC
$Q_{gd}$	Gate–Drain Charge		–	35	–	nC

**Drain–Source Diode Characteristics and Maximum Ratings**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		–	–	11.4	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		–	–	45.6	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 11.4 A	–	–	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 11.4 A, dI <sub>F</sub> /dt = 100 A/μs	–	850	–	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	11.2	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**NOTES:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2.  $L = 15\text{ mH}, I_{AS} = 11.4\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$  starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 11.4\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature

## TYPICAL CHARACTERISTICS

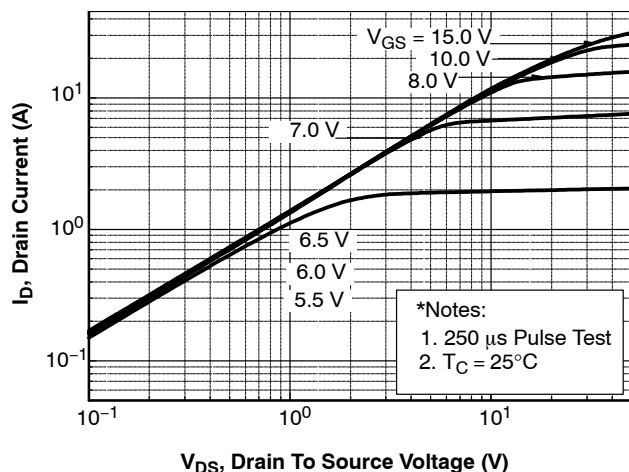


Figure 1. On-Region Characteristics

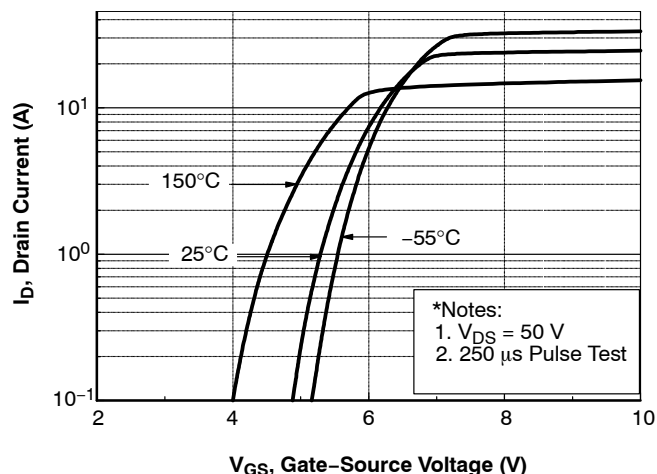


Figure 2. Transfer Characteristics

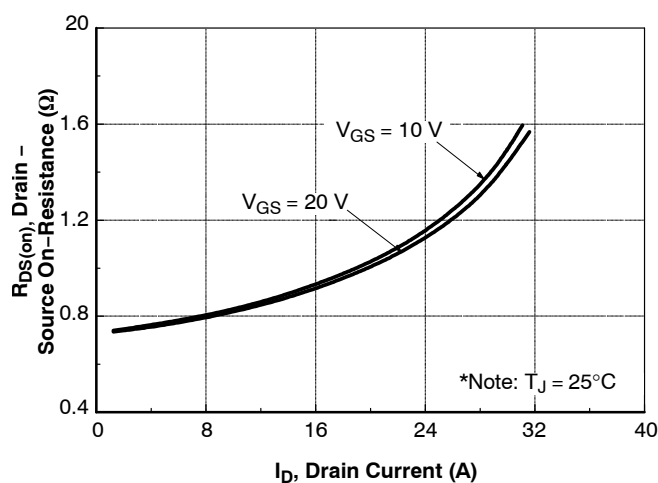


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

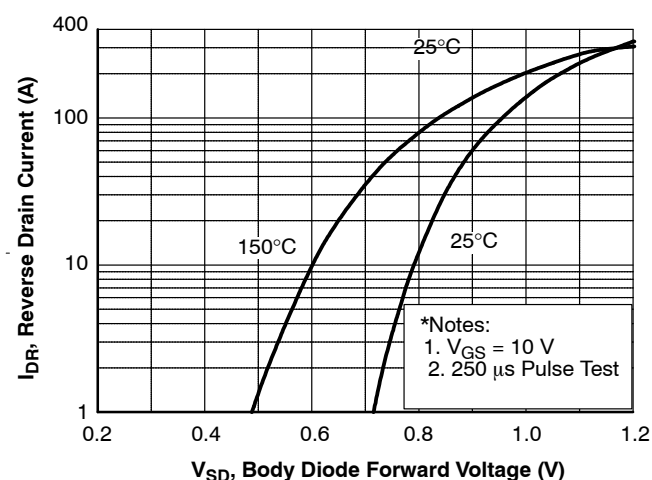


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

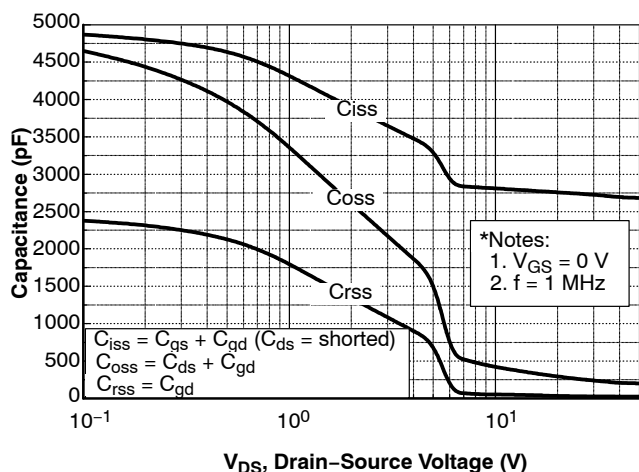


Figure 5. Capacitance Characteristics

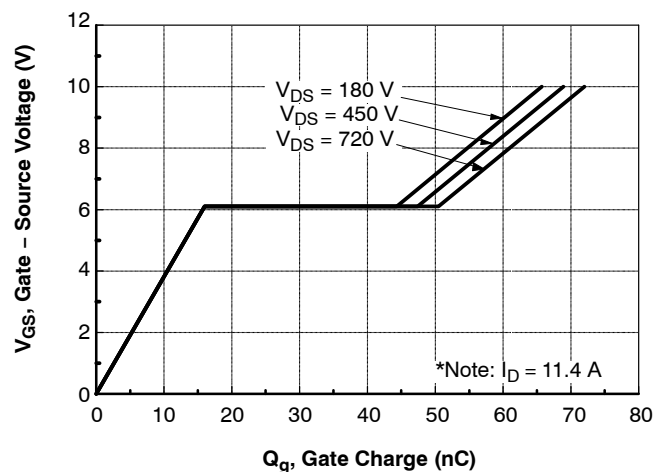


Figure 6. Gate Charge Characteristics

## TYPICAL CHARACTERISTICS (CONTINUED)

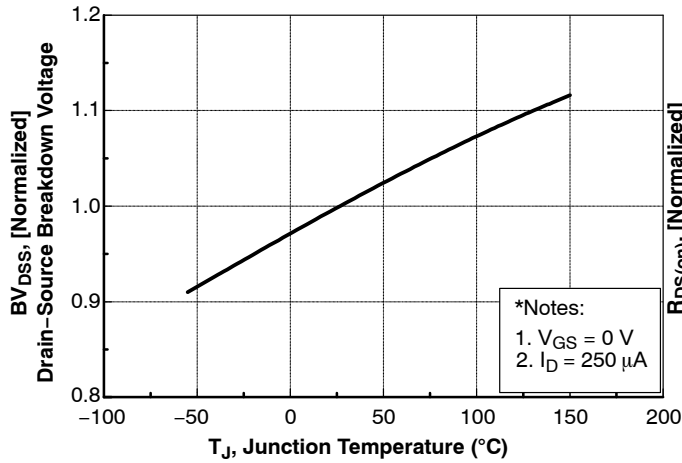


Figure 7. Breakdown Voltage Variation vs Temperature

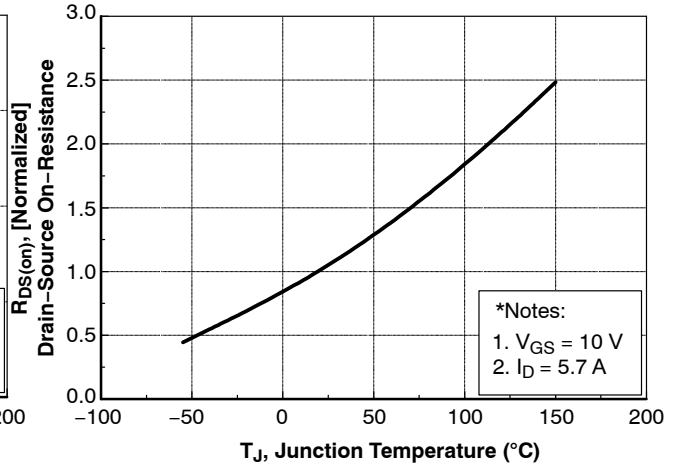


Figure 8. On-Resistance Variation vs Temperature

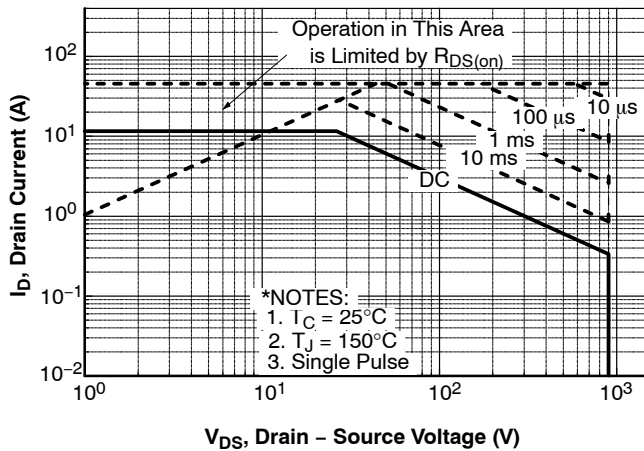


Figure 9. Maximum Safe Operating Area

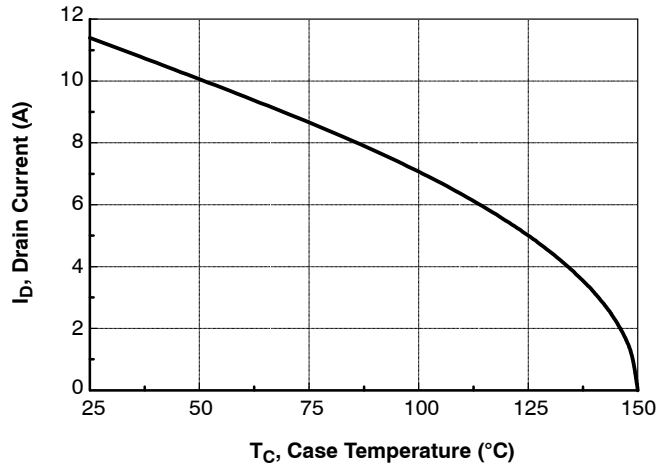


Figure 10. Maximum Drain Current vs. Case Temperature

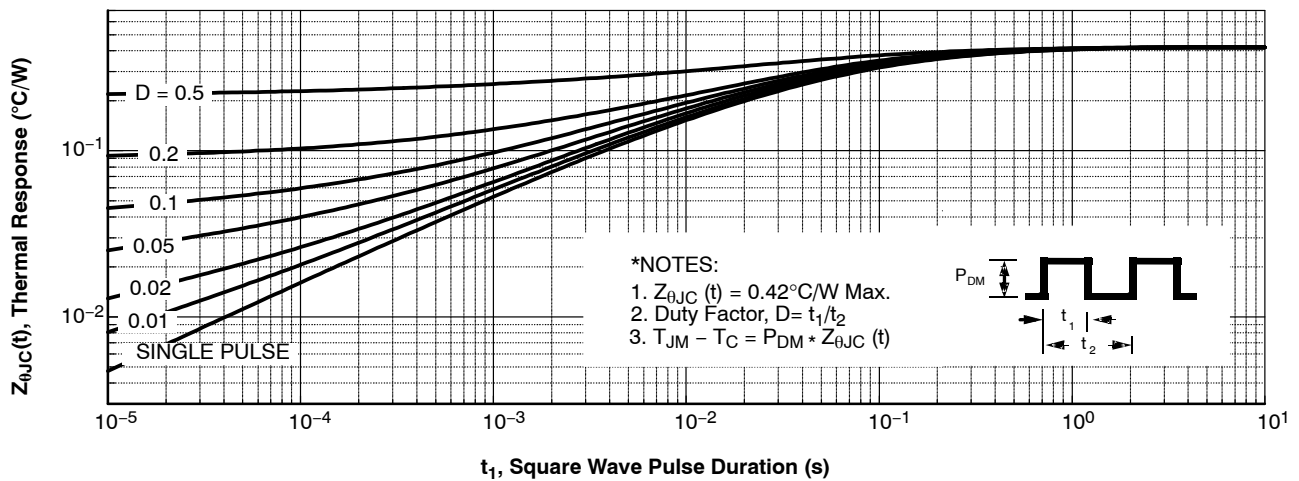


Figure 11. Transient Thermal Response Curve

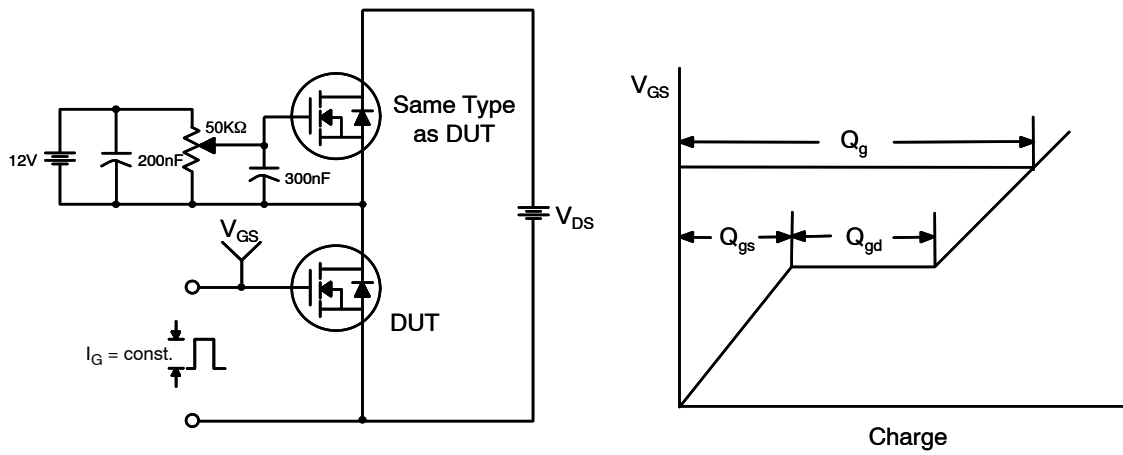


Figure 12. Gate Charge Test Circuit &amp; Waveform

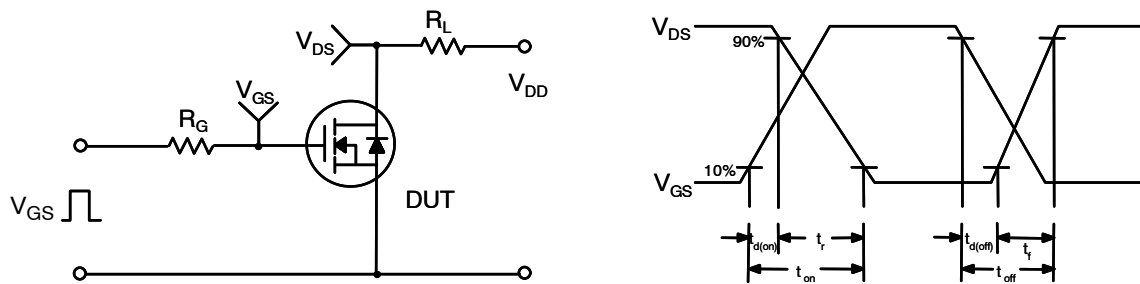


Figure 13. Resistive Switching Test Circuit &amp; Waveforms

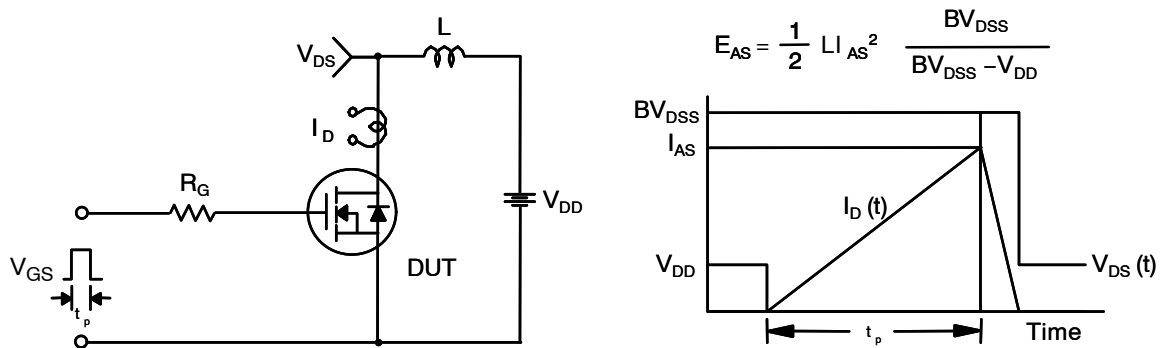
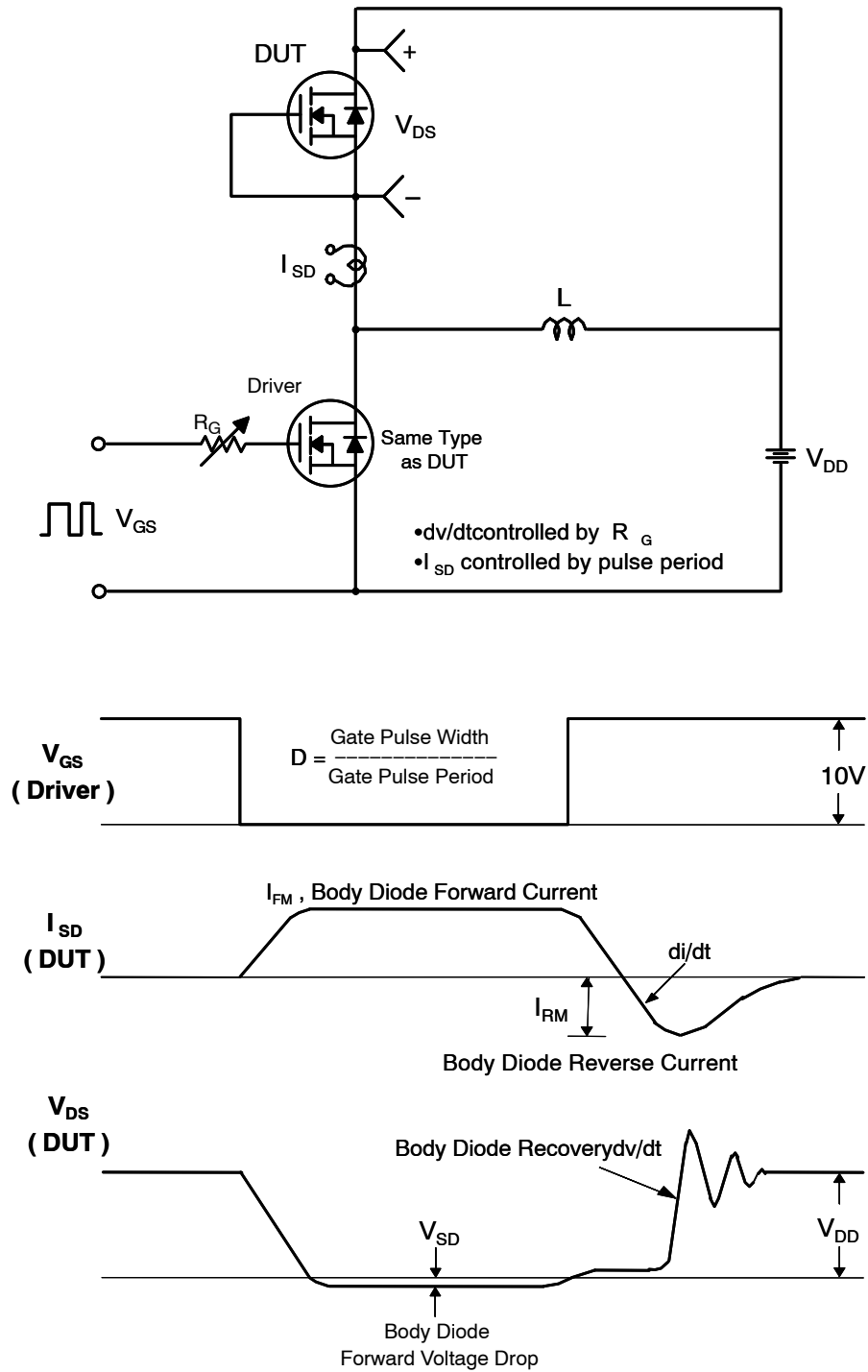


Figure 14. Unclamped Inductive Switching Test Circuit &amp; Waveforms

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**Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms**

# MECHANICAL CASE OUTLINE

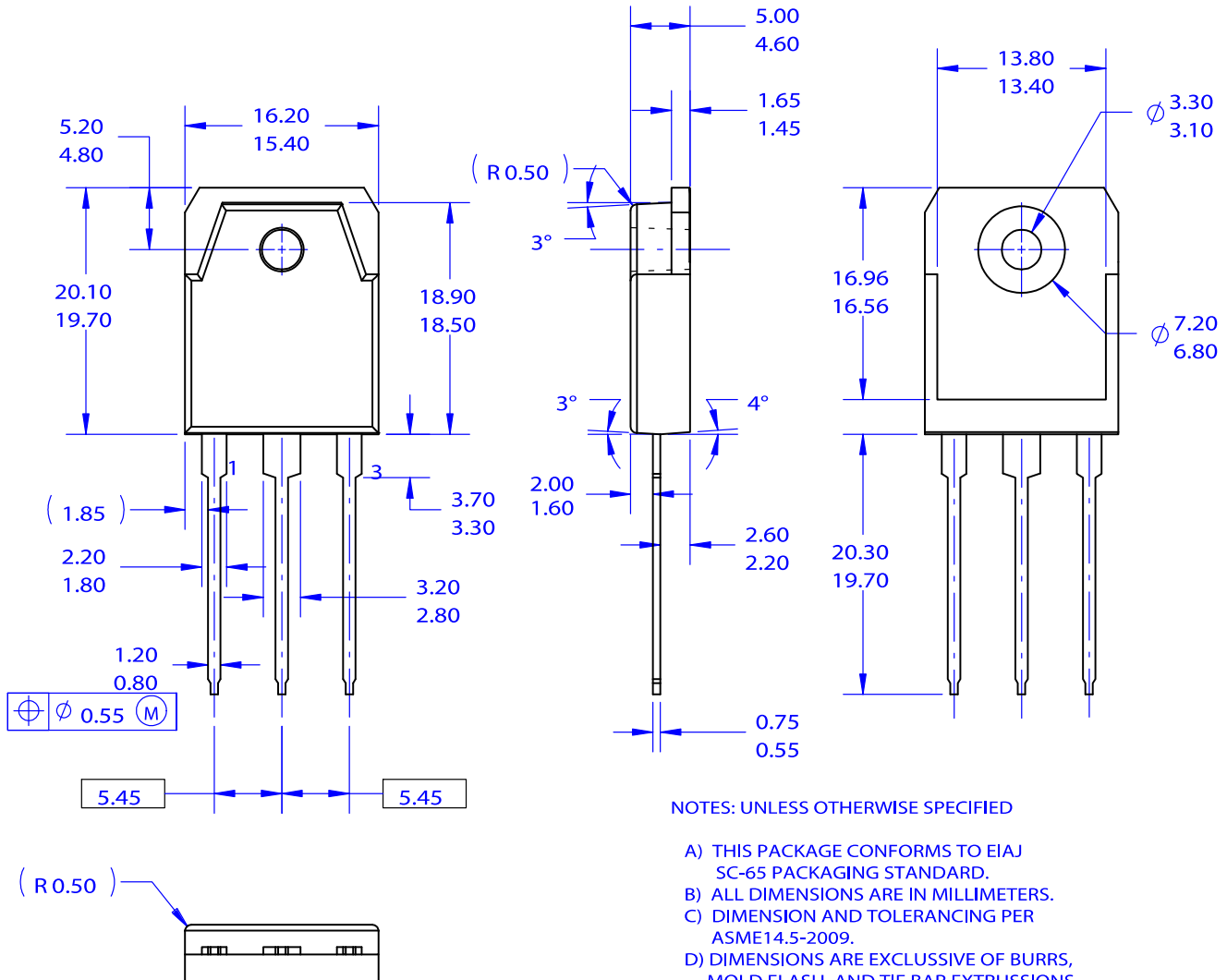
## PACKAGE DIMENSIONS

ON Semiconductor®

ON

TO-3P-3LD / EIAJ SC-65, ISOLATED  
CASE 340BZ  
ISSUE O

DATE 31 OCT 2016



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