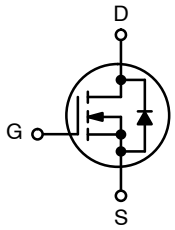
MOSFET – N-Channel, POWERTRENCH®

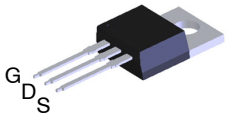
100 V, 74 A, 12 mΩ

FDP120N10

V_{DSS}	$R_{DS(on)}$ TYP	I_D MAX
100 V	9.7 mΩ @ 10 V	74 A



N−Channel MOSFET



TO−220−3LD
CASE 340AT

Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been tailored to minimize the on−state resistance while maintaining superior switching performance.

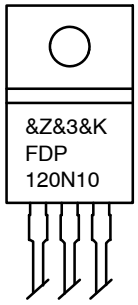
Features

- $R_{DS(on)}$ = 9.7 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 74 A
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability RoHS Compliant
- This Device is Pb−Free, Halide Free and RoHS Compliant

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micor Solar Inverter

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= 3−Digit Date Code Format
&K	= 3−Digit Lot Run Traceability Code
FDP120N10	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FDP120N10	TO−220 (Pb−Free)	800 Units / Tube

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FDP120N10	Unit
V_{DSS}	Drain to Source Voltage		100	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	– Continuous (T_C = 25°C, Silicon Limited)	74	A
		– Continuous (T_C = 100°C, Silicon Limited)	52	
I_{DM}	Drain Current	– Pulsed (Note 1)	296	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		198	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	170	W
		– Derate Above 25°C	1.14	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +175	°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. L = 0.11 mH, I_{AS} = 60 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 74 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP120N10	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.88	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V, T_C = 25°C	100	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.1	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 100 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 100 V, V_{GS} = 0 V, T_C = 150°C	–	–	500	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	–	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 74 A	–	9.7	12	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 74 A	–	105	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	4215	5605	pF
C_{oss}	Output Capacitance		–	405	540	pF
C_{rss}	Reverse Transfer Capacitance		–	170	255	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 80 V, I_D = 74 A, V_{GS} = 10 V (Note 4)	–	66	86	nC
Q_{gs}	Gate to Source Gate Charge		–	26	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	20	–	nC
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 50 V, I_D = 74 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	–	27	64	ns
t_r	Turn−On Rise Time		–	105	220	ns
$t_{d(off)}$	Turn−Off Delay Time		–	39	88	ns
t_f	Turn−Off Fall Time		–	15	40	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	74	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	296	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 74 A	–	–	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 74 A, dI_F/dt = 100 A/μs	–	44	–	ns
Q_{rr}	Reverse Recovery Charge		–	67	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Package limitation current is 120 A.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

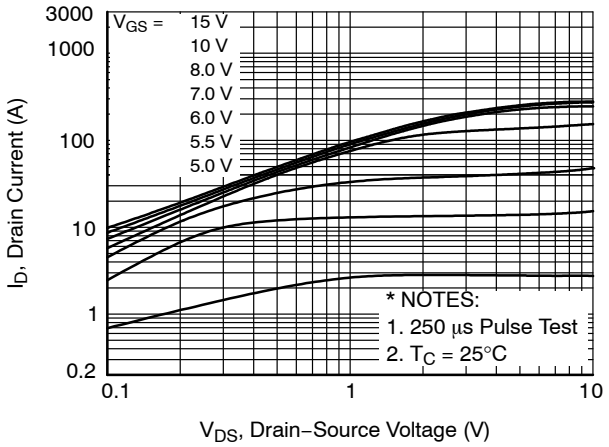


Figure 1. On−Region Characteristics

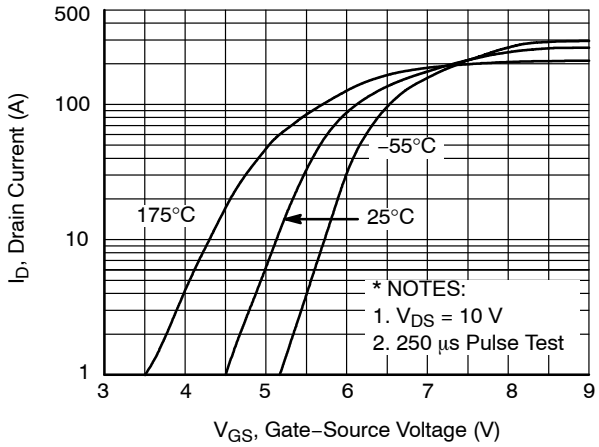


Figure 2. Transfer Characteristics

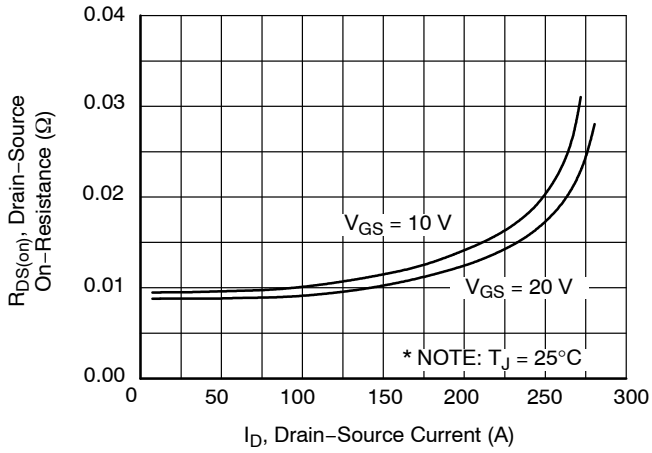


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

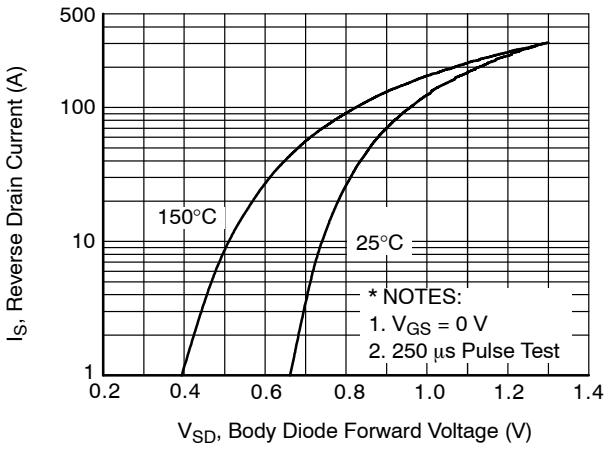


Figure 4. Body Diode Forward Voltage Variation vs. Source Current And Temperature

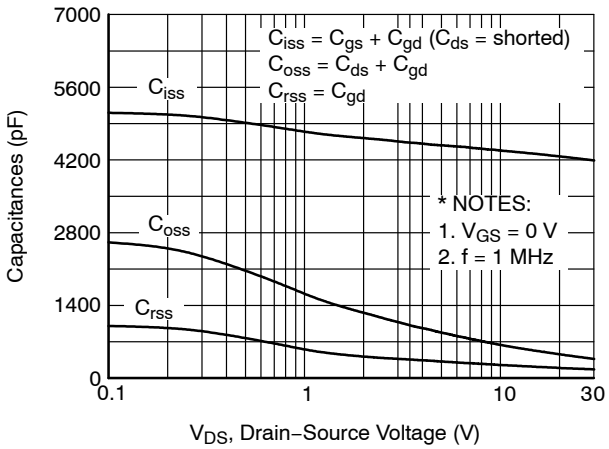


Figure 5. Capacitance Characteristics

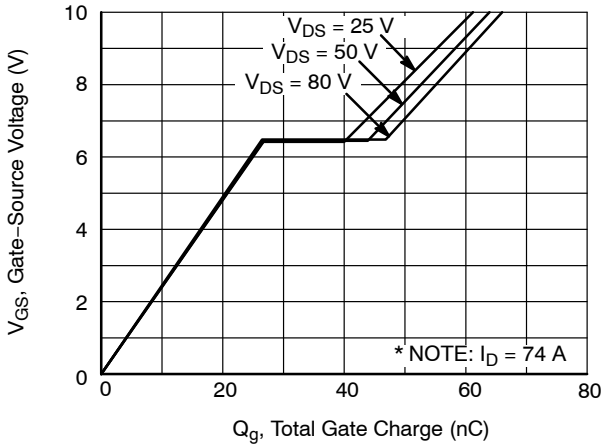


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

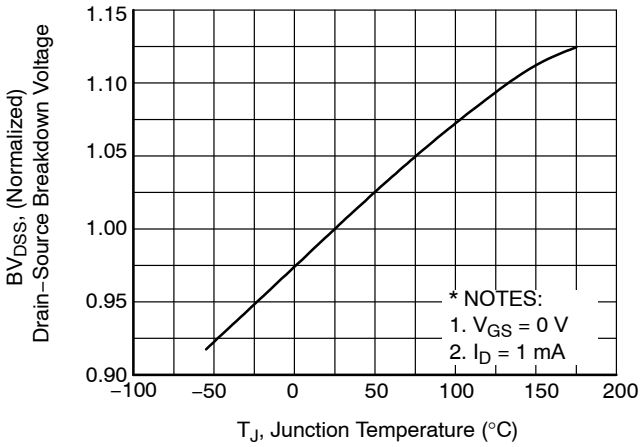


Figure 7. Breakdown Voltage Variation vs. Temperature

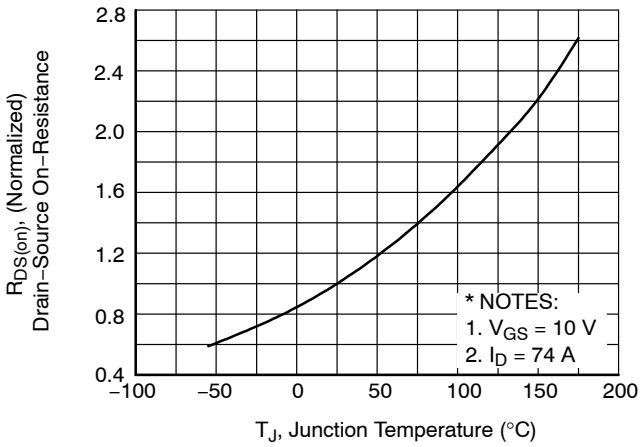


Figure 8. On−Resistance Variation vs. Temperature

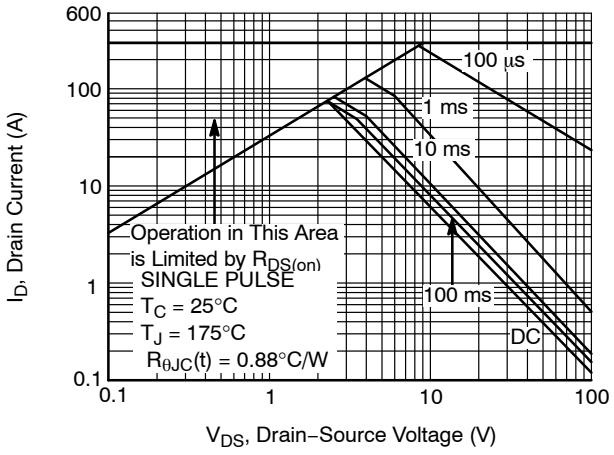


Figure 9. Maximum Safe Operating Area

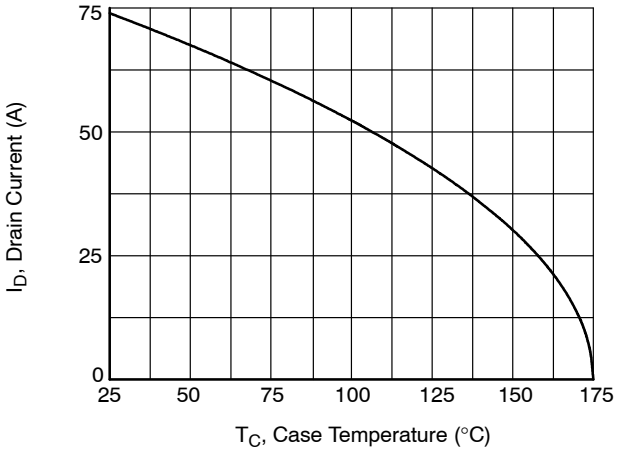


Figure 10. Maximum Drain Current vs. Case Temperature

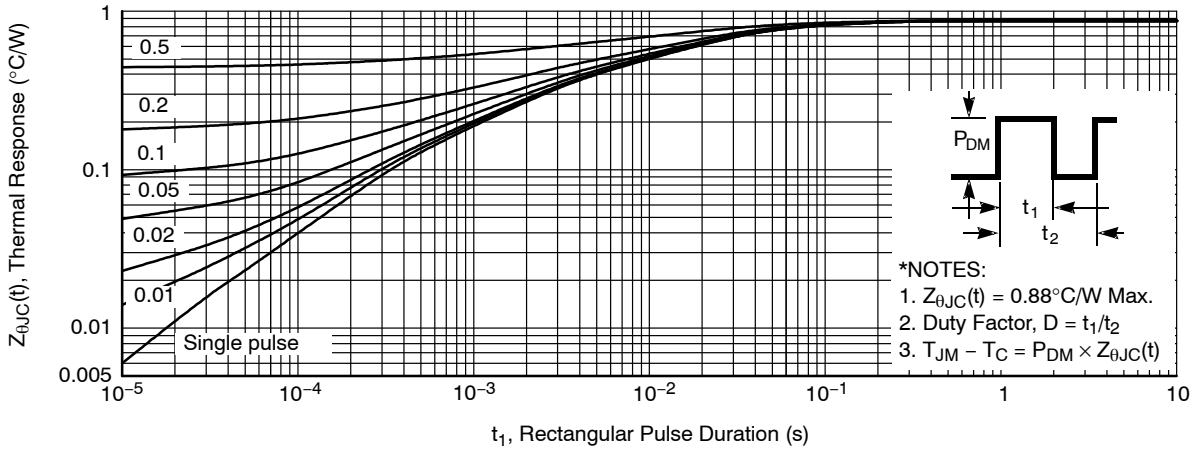


Figure 11. Transient Thermal Response Curve

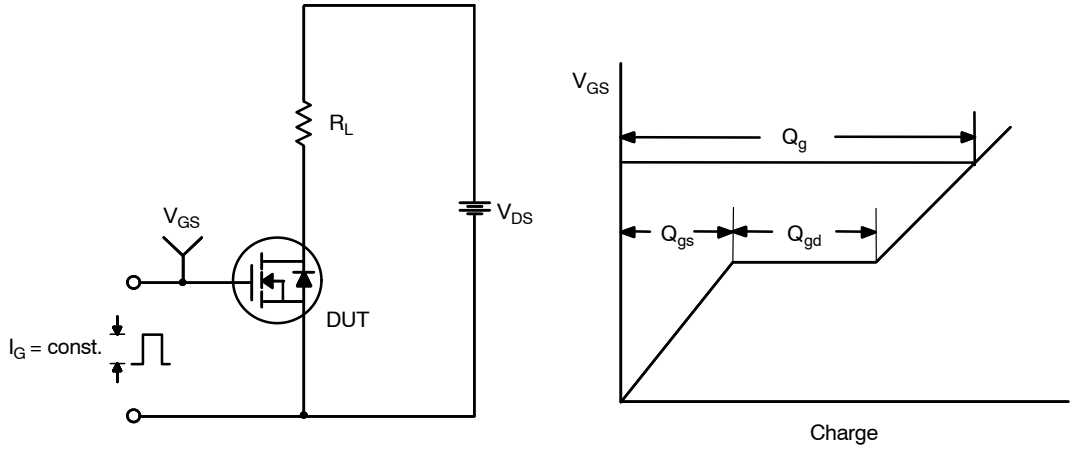


Figure 12. Gate Charge Test Circuit & Waveform

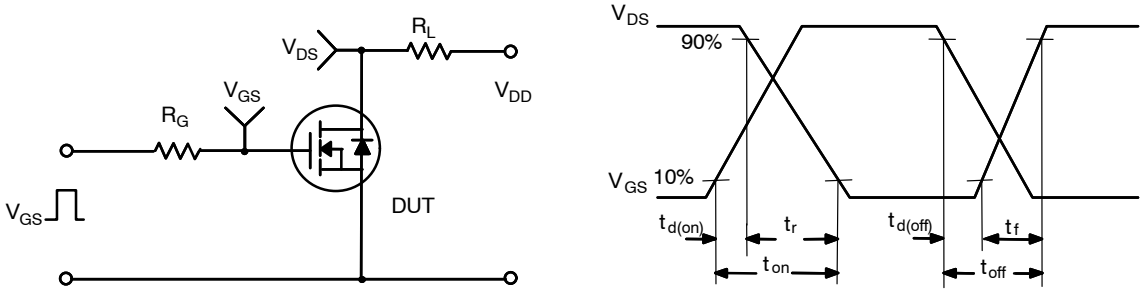


Figure 13. Resistive Switching Test Circuit & Waveforms

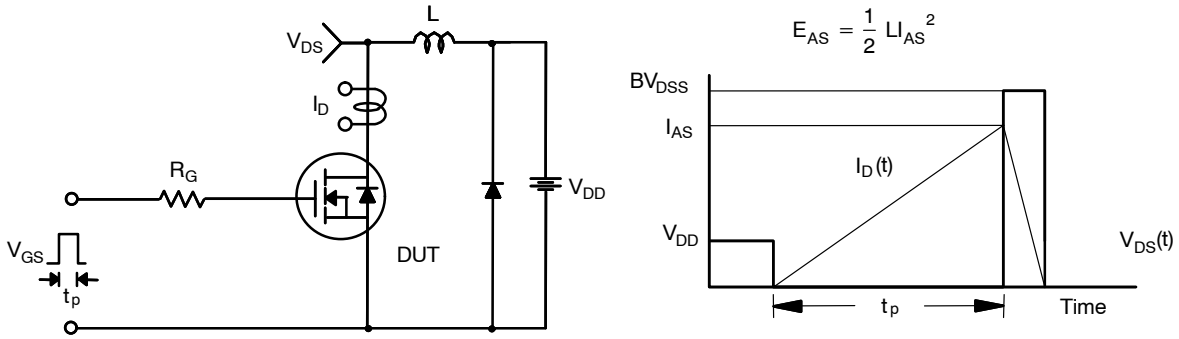


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

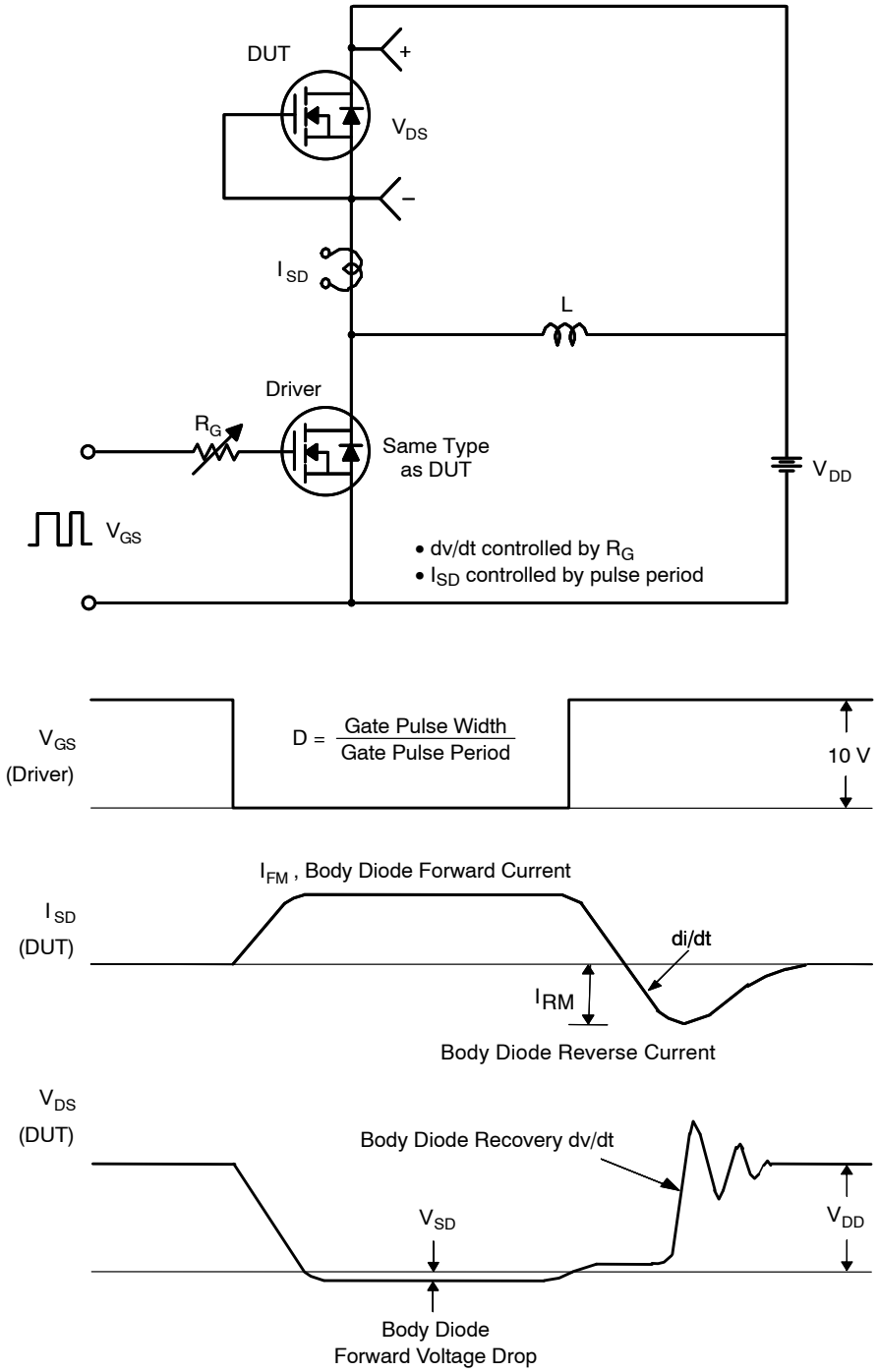


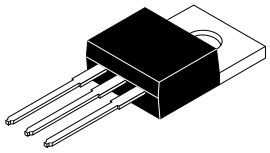
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



Scale 1:1

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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