

# MOSFET – N-Channel, POWERTRENCH®

**100 V, 74 A, 12 mΩ**

## FDP120N10

### Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

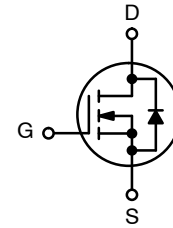
### Features

- $R_{DS(on)} = 9.7 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 74 \text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability RoHS Compliant
- This Device is Pb-Free, Halide Free and RoHS Compliant

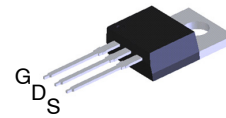
### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micor Solar Inverter

$V_{DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
100 V	9.7 mΩ @ 10 V	74 A

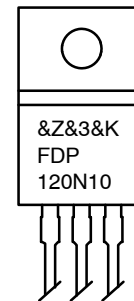


**N-Channel MOSFET**



**TO-220-3LD  
CASE 340AT**

### MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= 3-Digit Date Code Format
&K	= 3-Digit Lot Run Traceability Code
FDP120N10	= Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping
FDP120N10	TO-220 (Pb-Free)	800 Units / Tube

# FDP120N10

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		FDP120N10	Unit
$V_{DSS}$	Drain to Source Voltage		100	V
$V_{GSS}$	Gate to Source Voltage		$\pm 20$	V
$I_D$	Drain Current	– Continuous ( $T_C = 25^\circ\text{C}$ , Silicon Limited)	74	A
		– Continuous ( $T_C = 100^\circ\text{C}$ , Silicon Limited)	52	
$I_{DM}$	Drain Current	– Pulsed (Note 1)	296	A
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)		198	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)		6.0	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	170	W
		– Derate Above $25^\circ\text{C}$	1.14	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range		$-55$ to $+175$	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $L = 0.11$  mH,  $I_{AS} = 60$  A,  $V_{DD} = 50$  V,  $R_G = 25$   $\Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 74$  A,  $di/dt \leq 200$  A/ $\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .

## THERMAL CHARACTERISTICS

Symbol	Parameter	FDP120N10	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.88	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

# FDP120N10

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 $\mu$ A, V <sub>GS</sub> = 0 V, T <sub>C</sub> = 25°C	100	–	–	V
$\Delta$ BV <sub>DSS</sub> / $\Delta$ T <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 $\mu$ A, Referenced to 25°C	–	0.1	–	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V	–	–	1	$\mu$ A
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>C</sub> = 150°C	–	–	500	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = $\pm$ 20 V, V <sub>DS</sub> = 0 V	–	–	$\pm$ 100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 $\mu$ A	2.5	–	4.5	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 74 A	–	9.7	12	m $\Omega$
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 74 A	–	105	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	4215	5605	pF
C <sub>oss</sub>	Output Capacitance		–	405	540	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	170	255	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10 V	V <sub>DS</sub> = 80 V, I <sub>D</sub> = 74 A, V <sub>GS</sub> = 10 V (Note 4)	–	66	86	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		–	26	–	nC
Q <sub>gd</sub>	Gate to Drain “Miller” Charge		–	20	–	nC

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 74 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 4.7 $\Omega$ (Note 4)	–	27	64	ns
t <sub>r</sub>	Turn-On Rise Time		–	105	220	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	39	88	ns
t <sub>f</sub>	Turn-Off Fall Time		–	15	40	ns

### DRAIN-SOURCE DIODE CHARACTERISTICS

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		–	–	74	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		–	–	296	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 74 A	–	–	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 74 A, dI <sub>F</sub> /dt = 100 A/ $\mu$ s	–	44	–	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	67	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

\*Package limitation current is 120 A.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

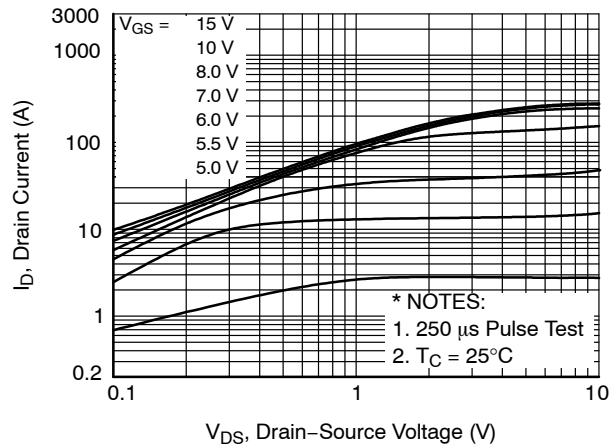


Figure 1. On-Region Characteristics

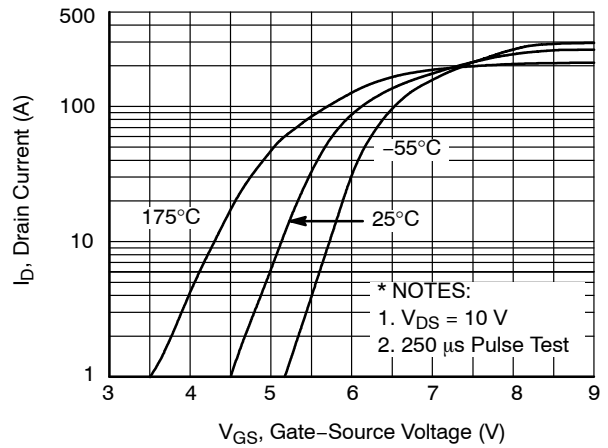


Figure 2. Transfer Characteristics

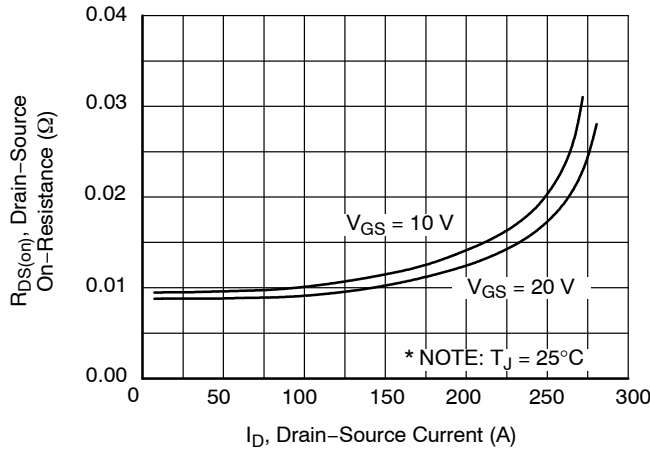


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

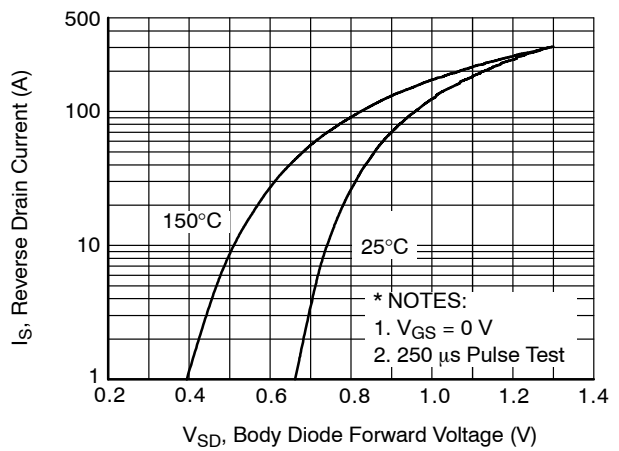


Figure 4. Body Diode Forward Voltage Variation vs. Source Current And Temperature

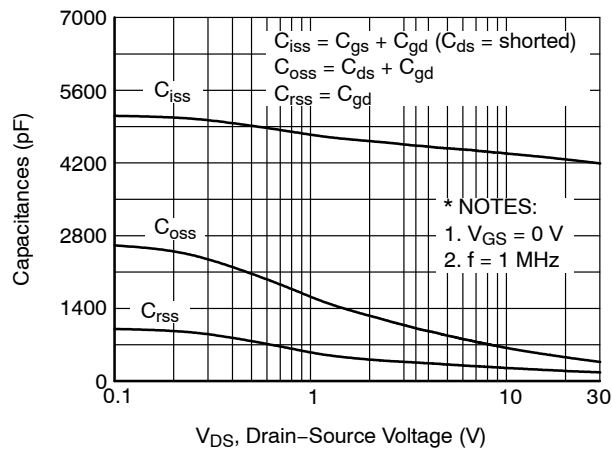


Figure 5. Capacitance Characteristics

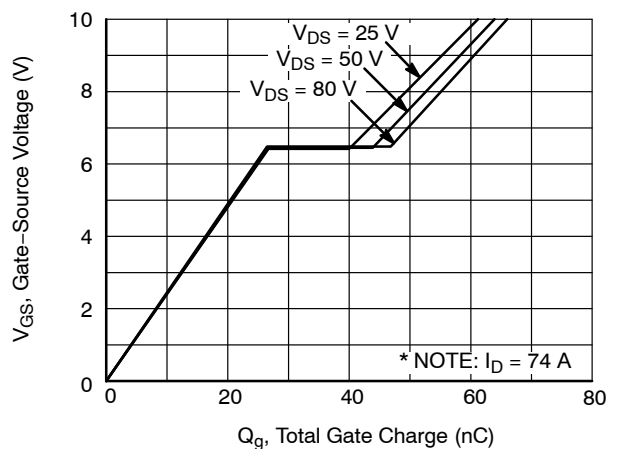


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

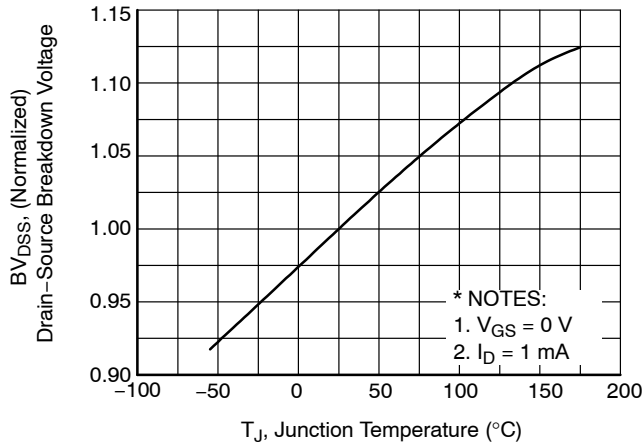


Figure 7. Breakdown Voltage Variation vs. Temperature

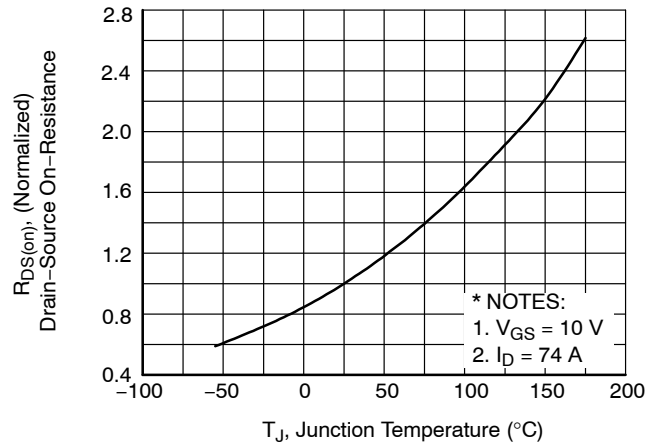


Figure 8. On-Resistance Variation vs. Temperature

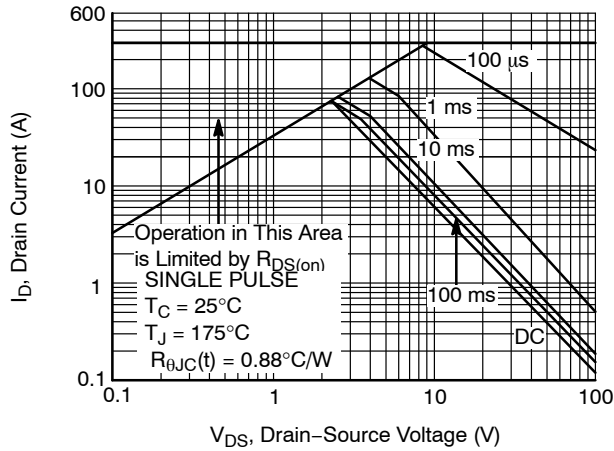


Figure 9. Maximum Safe Operating Area

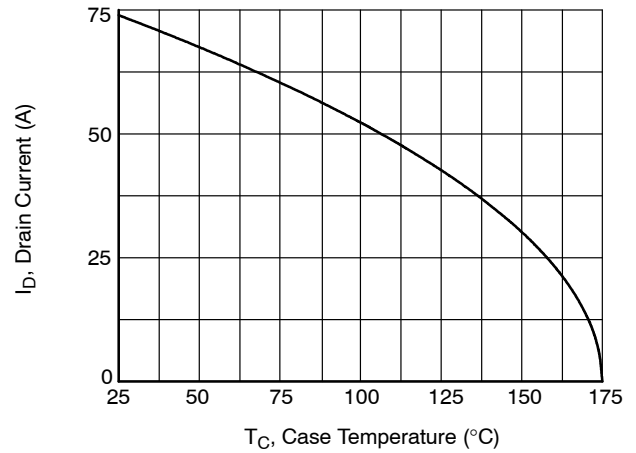


Figure 10. Maximum Drain Current vs. Case Temperature

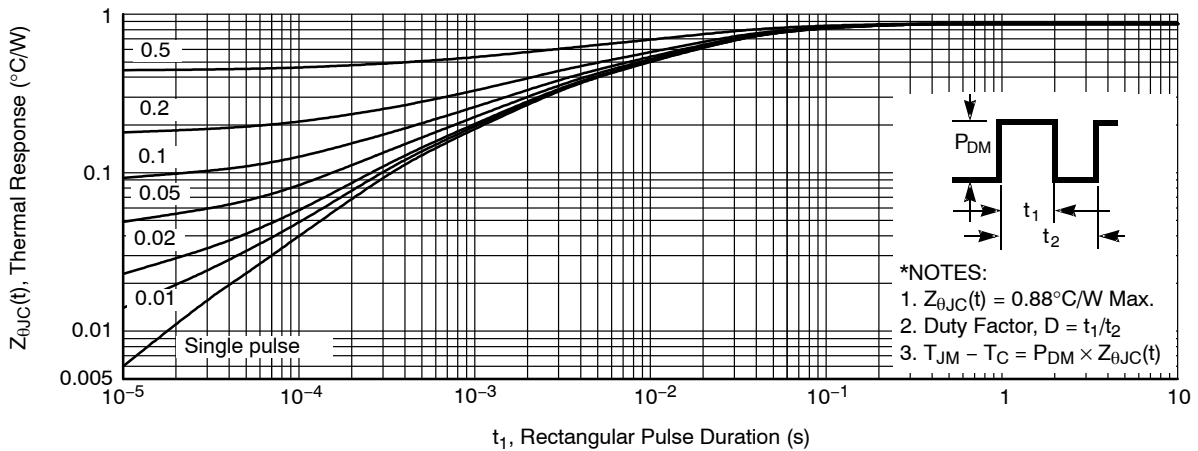


Figure 11. Transient Thermal Response Curve

# FDP120N10

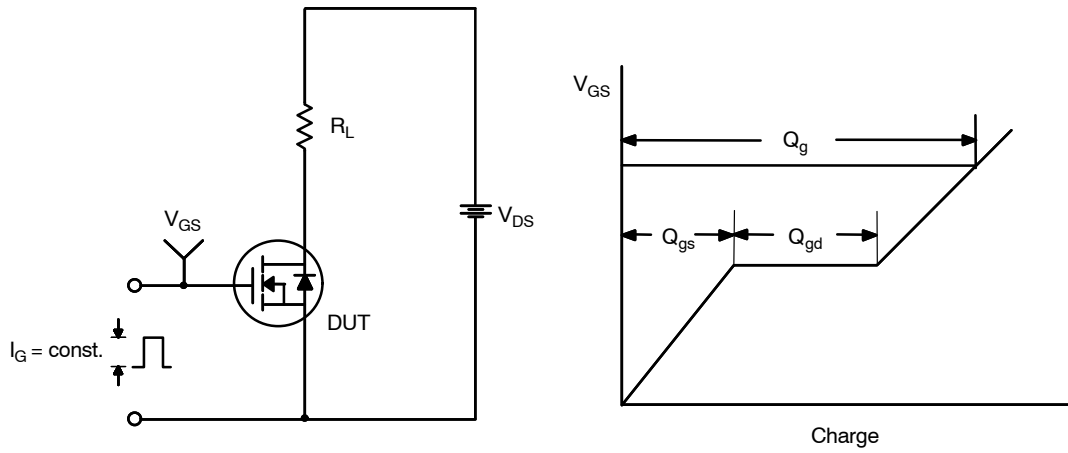


Figure 12. Gate Charge Test Circuit & Waveform

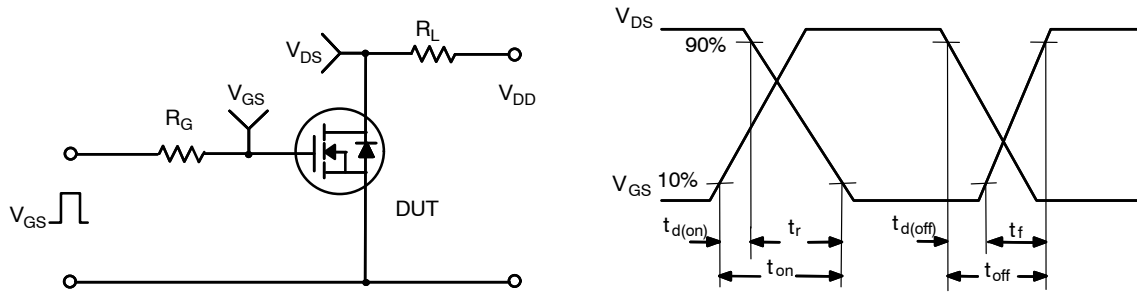


Figure 13. Resistive Switching Test Circuit & Waveforms

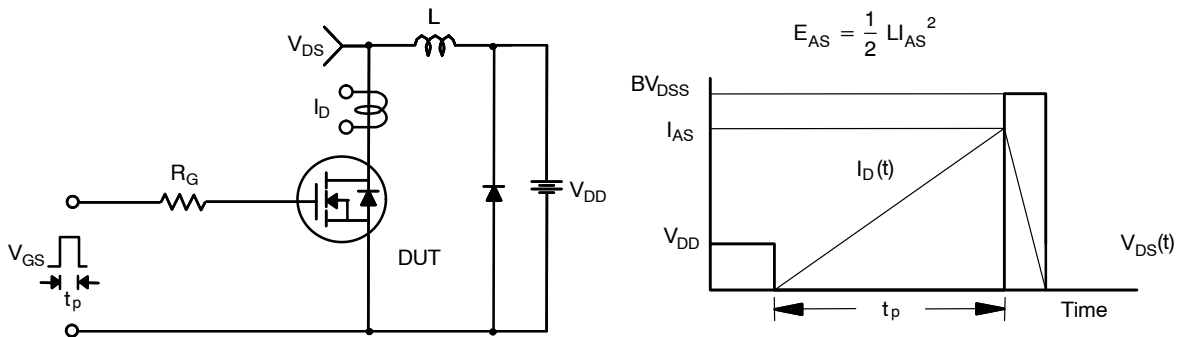
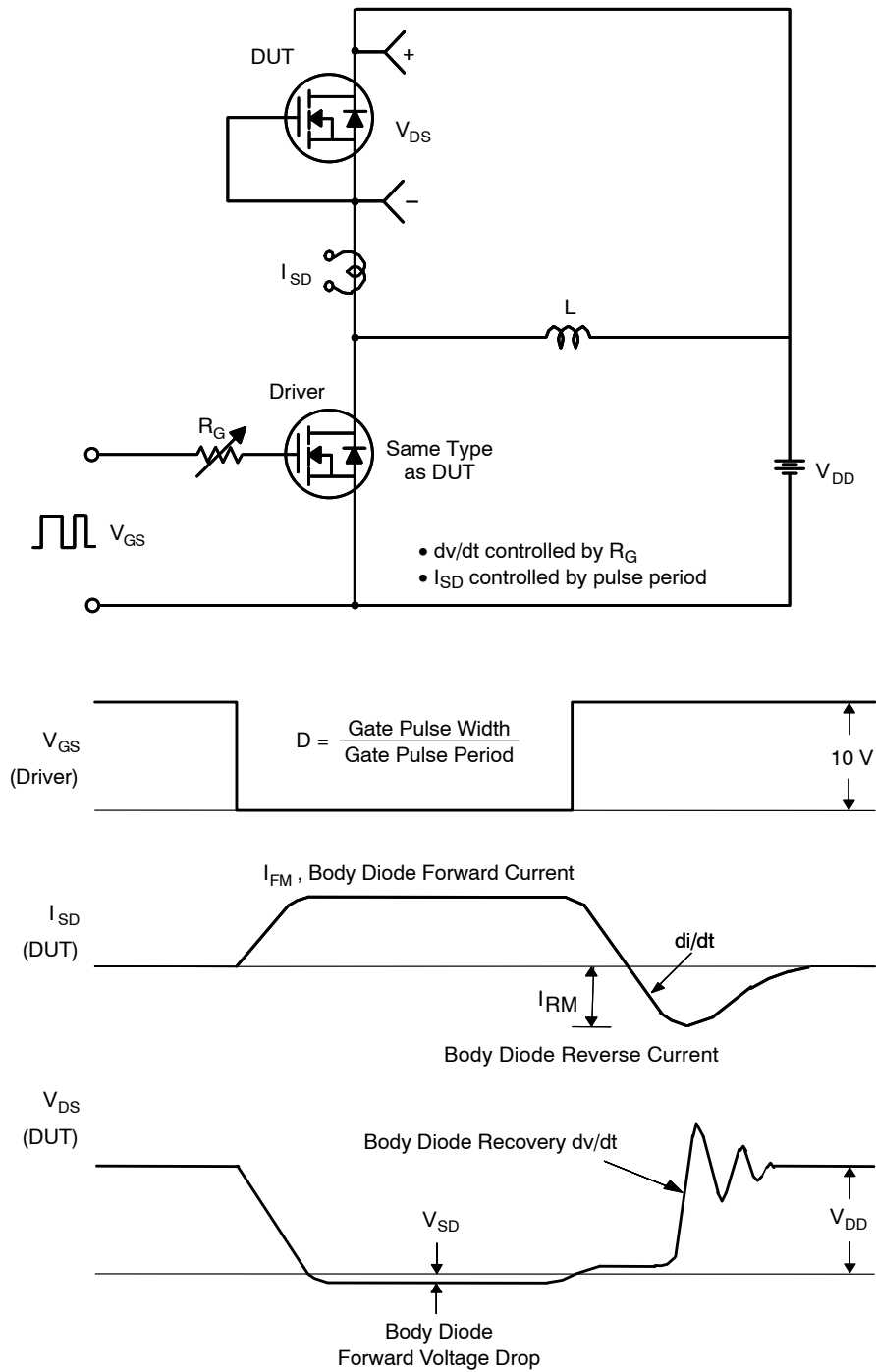


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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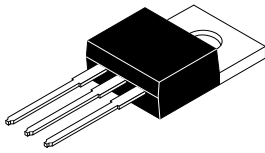


**Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

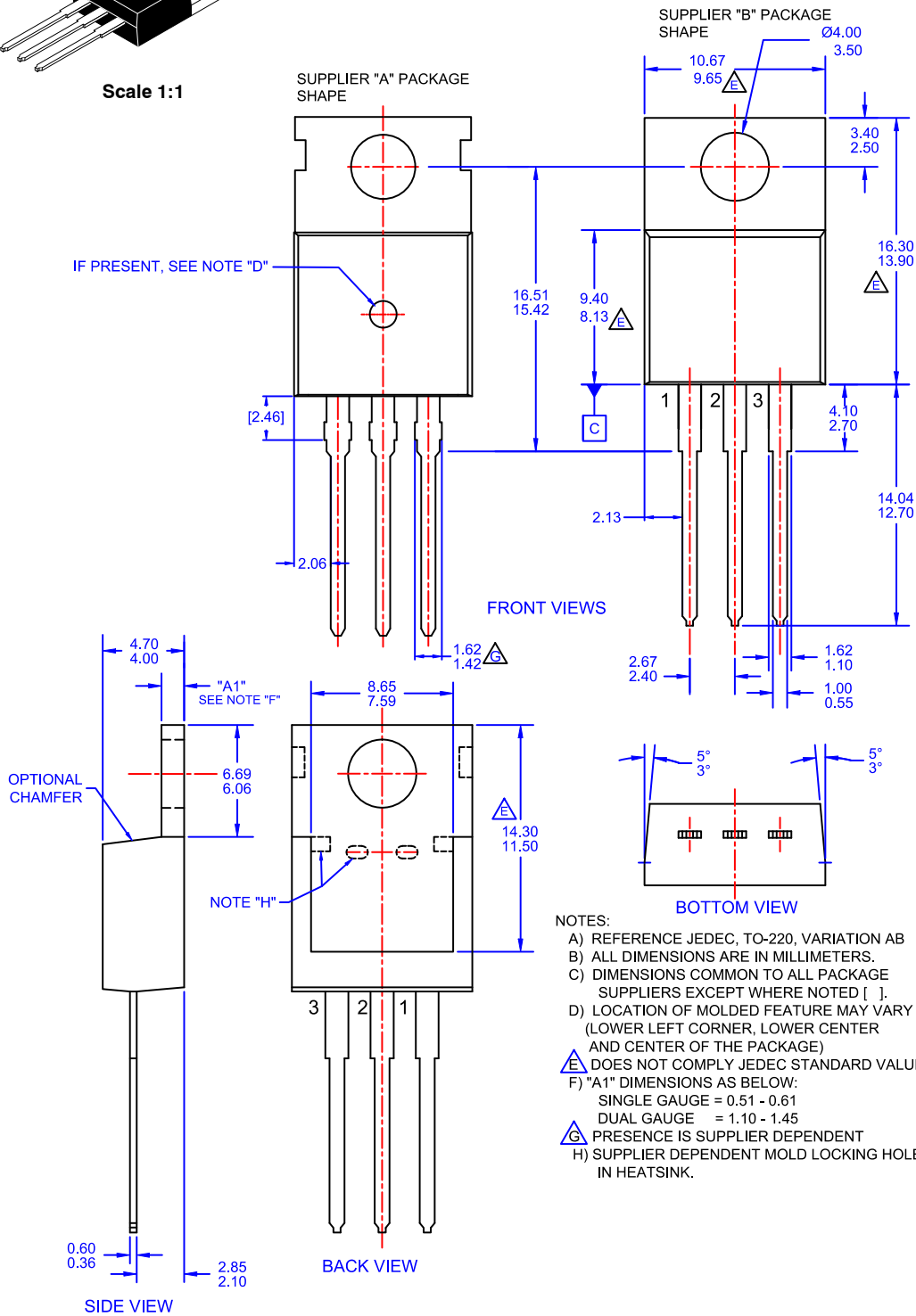
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Scale 1:1

## TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017



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