

MOSFET – P-Channel, POWERTRENCH®

-150 V, -0.8 A, 1.2 Ω

FDN86265P

General Description

This P-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been optimized for the on-state resistance and yet maintain superior switching performance.

Features

- Max $r_{DS(on)}$ = 1.2 Ω at $V_{GS} = -10$ V, $I_D = -0.8$ A
Max $r_{DS(on)}$ = 1.4 Ω at $V_{GS} = -6$ V, $I_D = -0.7$ A
- Very Low R_{DS-on} Mid Voltage P-Channel Silicon Technology Optimised for Low Q_g
- This Product is Optimised for Fast Switching Applications as Well as Load Switch Applications
- 100% UIL Tested
- Pb-Free, Halide Free and RoHS Compliant

Applications

- Active Clamp Switch
- Load Switch

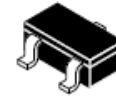
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	-150	V
V_{GS}	Gate to Source Voltage	± 25	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	-0.8 -5	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	6	mJ
P_D	Power Dissipation (Note 1a) (Note 1b)	1.5 0.6	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

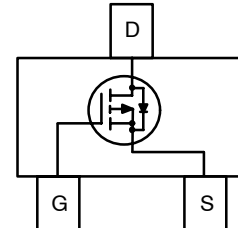
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

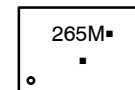
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	75	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	80	$^\circ\text{C/W}$



SOT-23/SUPERSOT™ -23, 3 LEAD,
1.4x2.9
CASE 527AG



MARKING DIAGRAM



265 = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
FDN86265P	SOT-23 (Pb-Free/ Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDN86265P

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-150	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	-129	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -120 V, V _{GS} = 0 V	-	-	-1	μA
I _{GSS}	Gate-Body Leakage	V _{GS} = ±25 V, V _{DS} = 0 V	-	-	±100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-2	-3.3	-4	V
ΔV _{GS(th)} / ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	5	-	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = -10 V, I _D = -0.8 A V _{GS} = -6 V, I _D = -0.7 A V _{GS} = -10 V, I _D = -0.8 A, T _J = 125°C	-	0.85 0.96 1.54	1.2 1.4 2.2	Ω
g _{FS}	Forward Transconductance	V _{DS} = -10 V, I _D = -0.8 A	-	1.5	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -75 V, V _{GS} = 0 V, f = 1 MHz	-	158	210	pF
C _{oss}	Output Capacitance		-	17	25	pF
C _{rss}	Reverse Transfer Capacitance		-	1.6	5	pF
R _g	Gate Resistance		0.1	3.3	6.7	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = -75 V, I _D = -0.8 A, V _{GS} = -10 V, R _{GEN} = 6 Ω	-	5.7	12	ns
t _r	Rise Time		-	2.2	10	ns
t _{d(off)}	Turn-Off Delay Time		-	7.9	16	ns
t _f	Fall Time		-	9.9	20	ns
Q _g	Total Gate Charge		-	2.9	4.1	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = -75 V, I _D = -0.8 A	-	0.8	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	0.8	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -0.8 A (Note 2)	-	-0.86	-1.3	V
t _{rr}	Reverse Recovery Time	I _F = -0.8 A, di/dt = 100 A/μs	-	49	78	ns
Q _{rr}	Reverse Recovery Charge		-	70	112	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a) 80°C/W when mounted on a 1 in² pad of 2 oz. copper.



b) 180°C/W when mounted on a minimum pad.

- Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.
- Starting T_J = 25°C; N-ch: L = 3 mH, I_{AS} = -2 A, V_{DD} = -150 V, V_{GS} = -10 V. 100% test at L = 0.1 mH, I_{AS} = -9 A.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

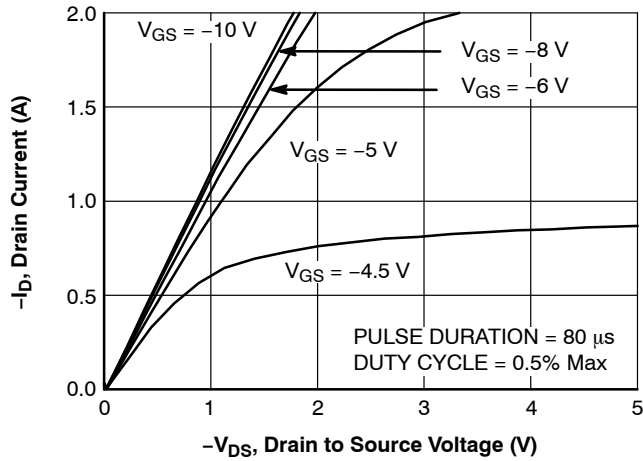


Figure 1. On Region Characteristics

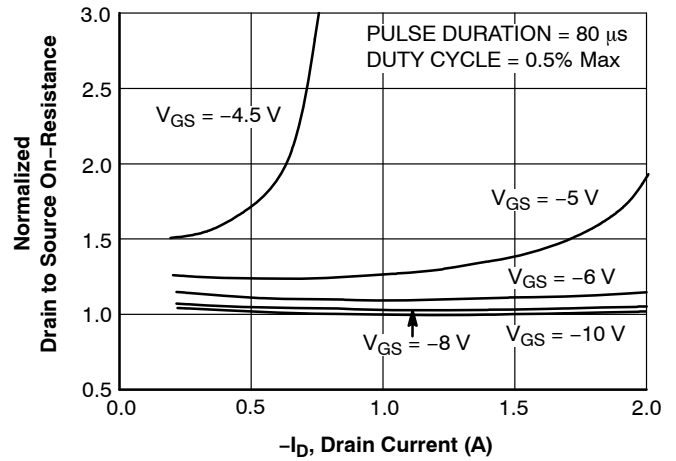


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

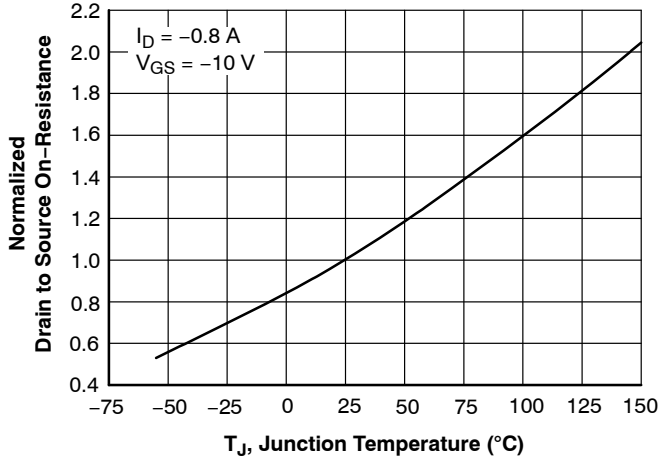


Figure 3. Normalized On Resistance vs. Junction Temperature

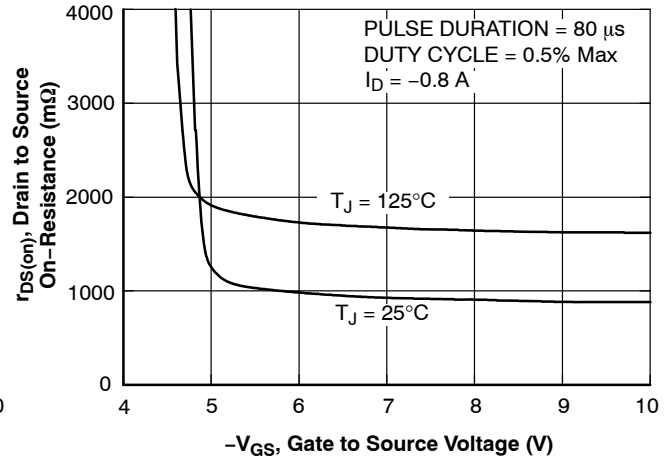


Figure 4. On-Resistance vs. Gate to Source Voltage

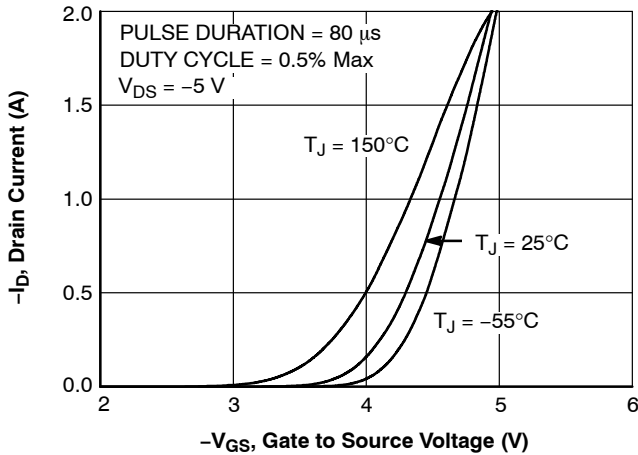


Figure 5. Transfer Characteristics

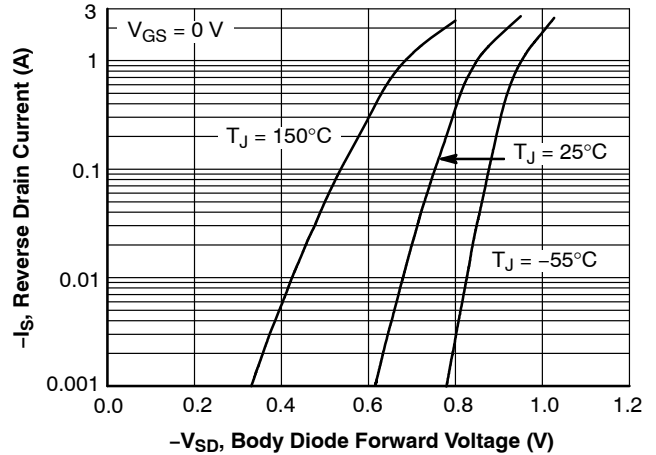


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (CONTINUED)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

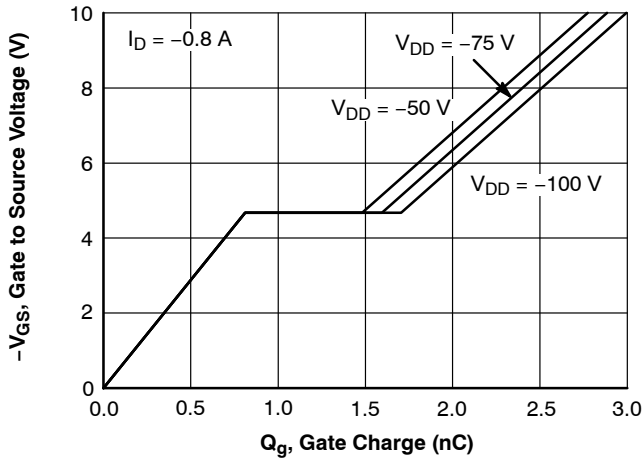


Figure 7. Gate Charge Characteristics

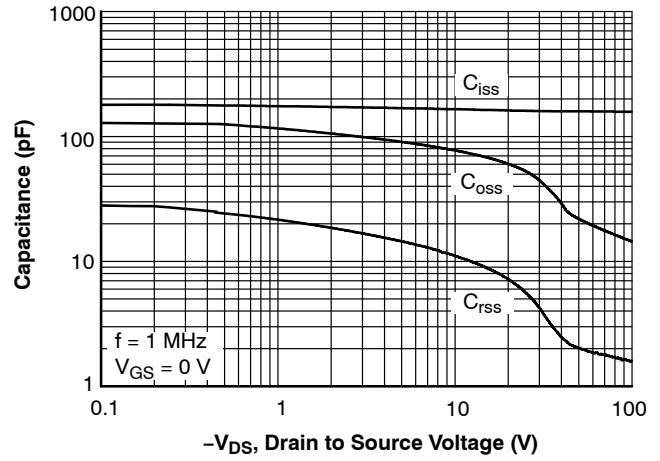


Figure 8. Capacitance vs. Drain to Source Voltage

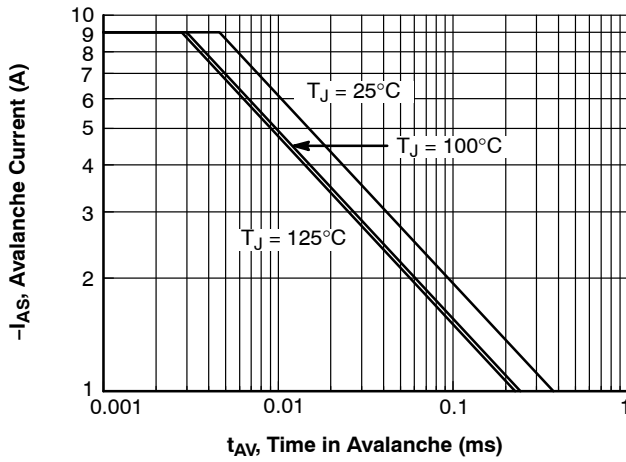


Figure 9. Unclamped Inductive Switching Capability

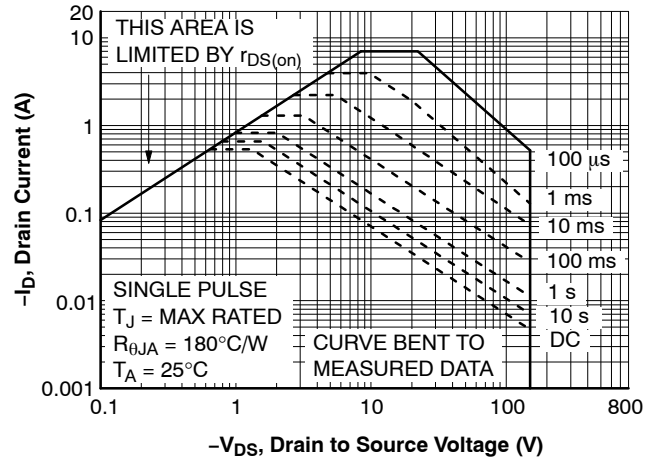


Figure 10. Forward Bias Safe Operating Area

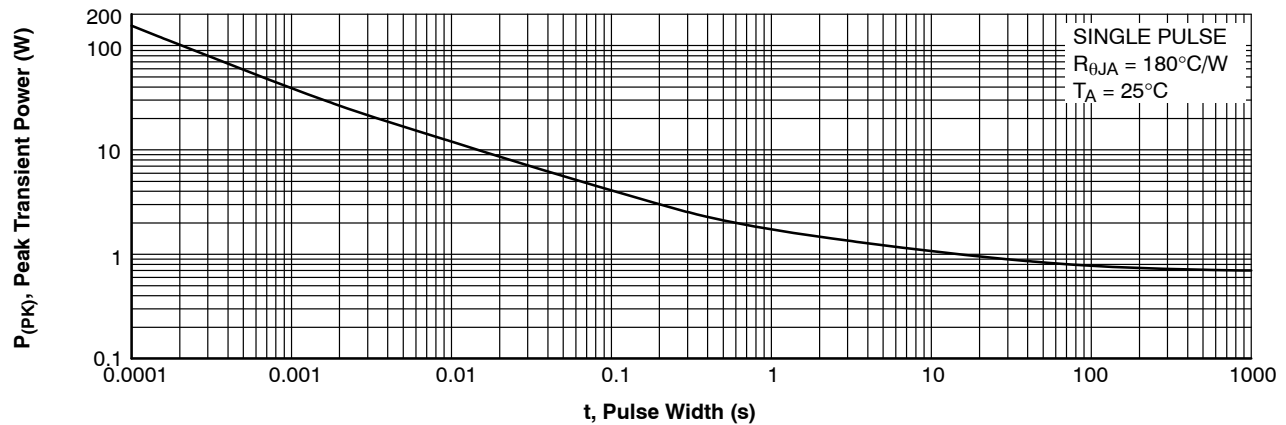


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (CONTINUED)

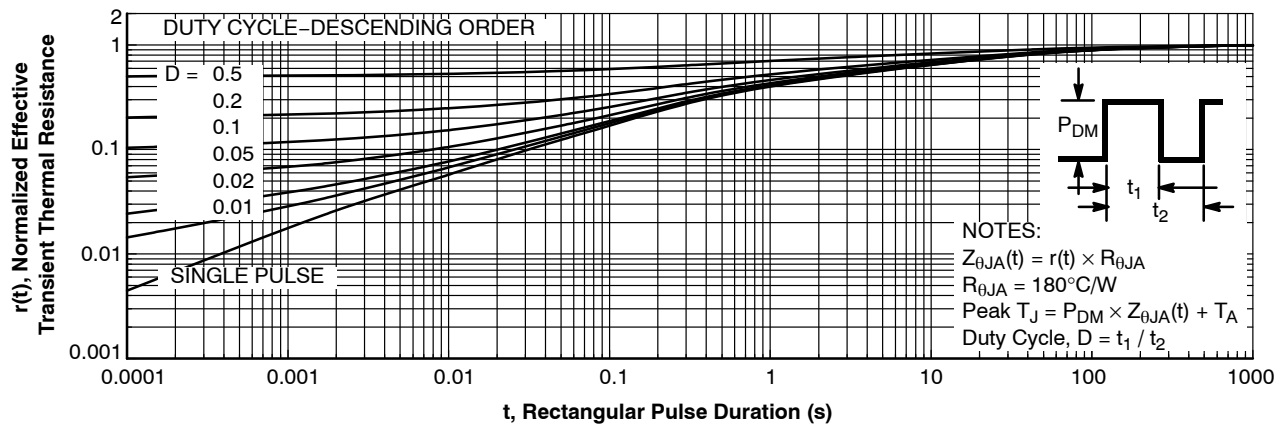
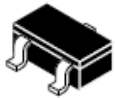
(T_J = 25°C unless otherwise noted)

Figure 12. Junction-to-Ambient Transient Thermal Response Curve

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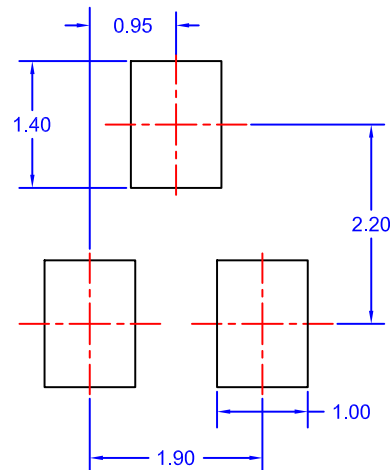
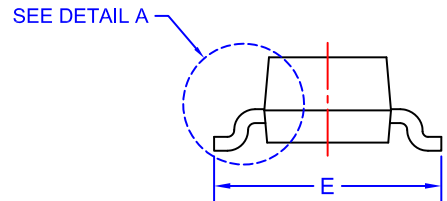
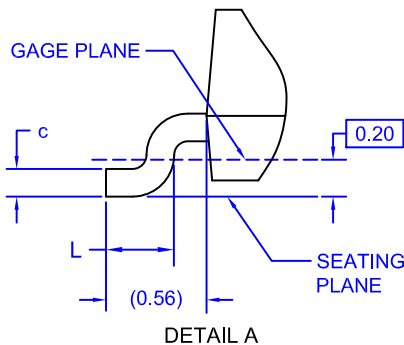
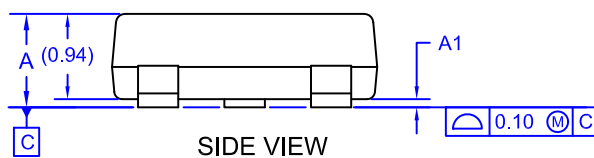
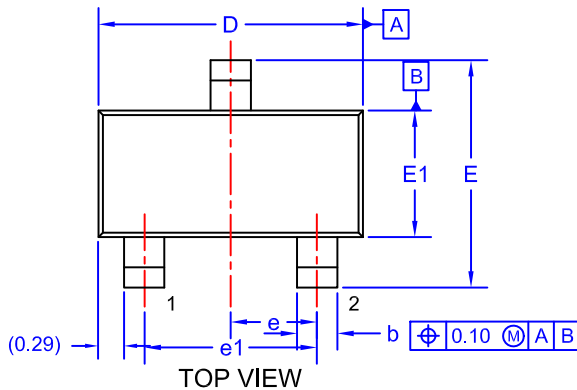
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23/SUPERSOT™ –23, 3 LEAD, 1.4x2.9 CASE 527AG ISSUE A

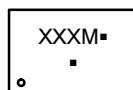
DATE 09 DEC 2019



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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