

MOSFET – N-Channel, POWER TRENCH®

60 V

FDN5630

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of dc-dc converters using either synchronous or conventional switching PWM controllers.

This MOSFET features very low $R_{DS(on)}$ in a small SOT23 footprint. onsemi's POWER TRENCH technology provides faster switching than other MOSFETs with comparable $R_{DS(on)}$ specifications. The result is higher overall efficiency with less board space.

Features

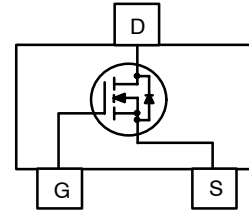
- -1.7 A, 60 V
 - ♦ $R_{DS(on)} = 0.100 \Omega @ V_{GS} = 10 V$
 - ♦ $R_{DS(on)} = 0.120 \Omega @ V_{GS} = 6 V$
- Optimized for Use in High Frequency DC-DC Converters
- Low Gate Charge
- Very Fast Switching
- SUPERSOT™-3 Provides Low $R_{DS(on)}$ in SOT23 Footprint
- This Device is Pb-Free and Halogen Free

Applications

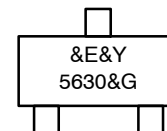
- DC-DC Converters
- Motor Drives



SOT-23-3
CASE 527AG



MARKING DIAGRAM



&E	= Designates Space
&Y	= Binary Calendar Year Coding Scheme
5630	= Specific Device Code
&G	= Date Code

ORDERING INFORMATION

Device	Package	Shipping†
FDN5630	SOT-23-3 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDN5630

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V _{DSS}	Drain–Source Voltage	60	V
V _{GSS}	Gate–Source Voltage	±20	V
I _D	Drain Current – Continuous (Note 1a)	1.7	A
	Drain Current – Pulsed	10	
P _D	Power Dissipation for Single Operation (Note 1a)	0.5	W
	Power Dissipation for Single Operation (Note 1b)	0.46	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R _{θJA}	Thermal Resistance, Junction–to–Ambient (Note 1a)	250	°C/W
R _{θJC}	Thermal Resistance, Junction–to–Case (Note 1)	75	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	60	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	63	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 48 V, V _{GS} = 0 V	–	–	1	μA
I _{GSSF}	Gate–Body Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	–	–	100	nA
I _{GSSR}	Gate–Body Leakage Current, Reverse	V _{GS} = –20 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	2.4	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	–6.9	–	mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 1.7 A	–	0.073	0.100	Ω
		V _{GS} = 10 V, I _D = 1.7 A T _J = 125°C	–	0.127	0.180	
		V _{GS} = 6 V, I _D = 1.6 A	–	0.083	0.120	
I _{D(on)}	On–State Drain Current	V _{GS} = 10 V, V _{DS} = 1.7 V	5	–	–	A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 1.7 A	–	6	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	–	400	560	pF
C _{oss}	Output Capacitance		–	65	95	
C _{rss}	Reverse Transfer Capacitance		–	27	40	

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\ \Omega$	–	10	20	ns
t_r	Turn-On Rise Time		–	6	15	
$t_{d(off)}$	Turn-Off Delay Time		–	15	28	
t_f	Turn-Off Fall Time		–	5	15	
Q_g	Total Gate Charge	$V_{DS} = 20\text{ V}$, $I_D = 1.7\text{ A}$, $V_{GS} = 10\text{ V}$	–	7	10	nC
Q_{gs}	Gate-Source Charge		–	1.6	–	
Q_{gd}	Gate-Drain Charge		–	1.2	–	

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	0.42	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.42 A (Note 2)	–	0.72	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in^2 pad of 2 oz. copper.



b) 270°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

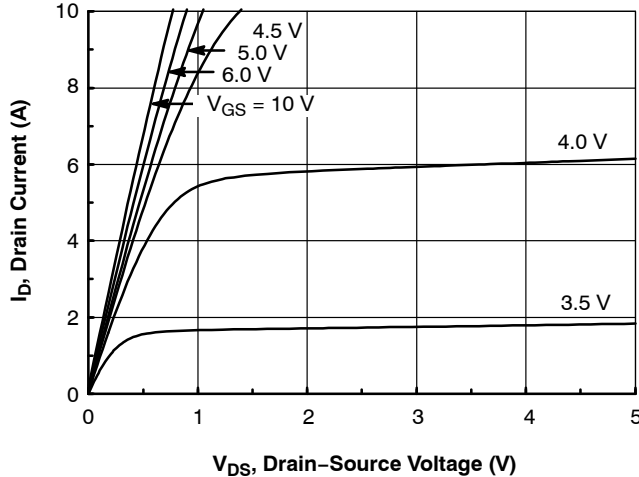
TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

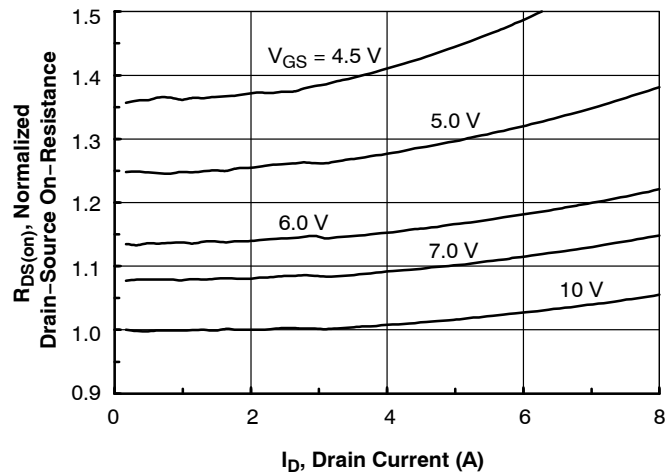


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS (CONTINUED)

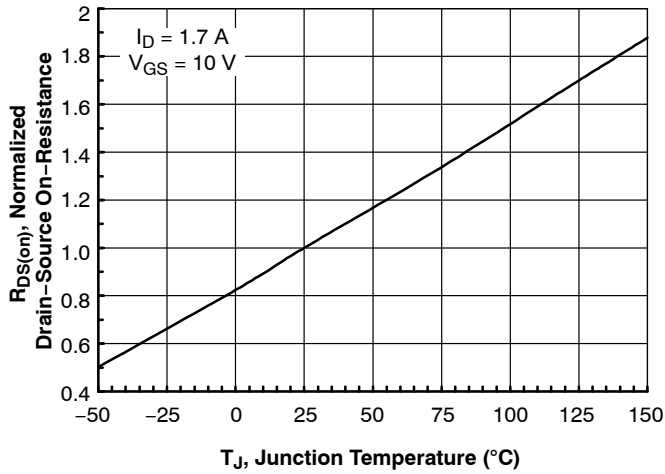


Figure 3. On-Resistance Variation with Temperature

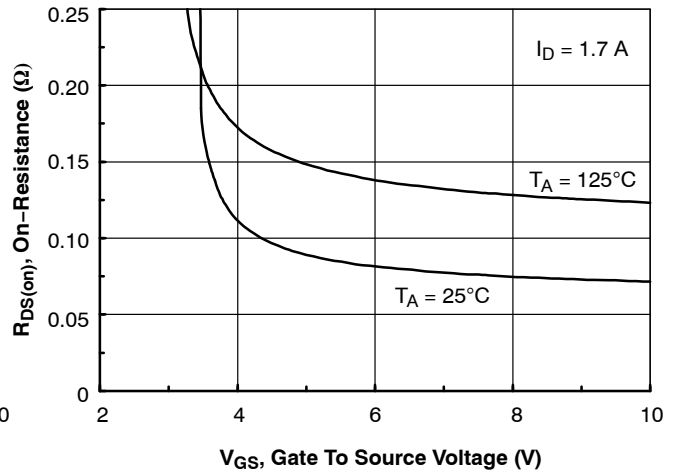


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

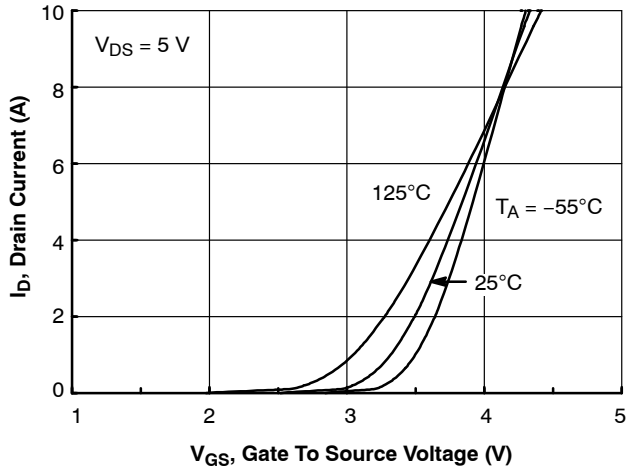


Figure 5. Transfer Characteristics

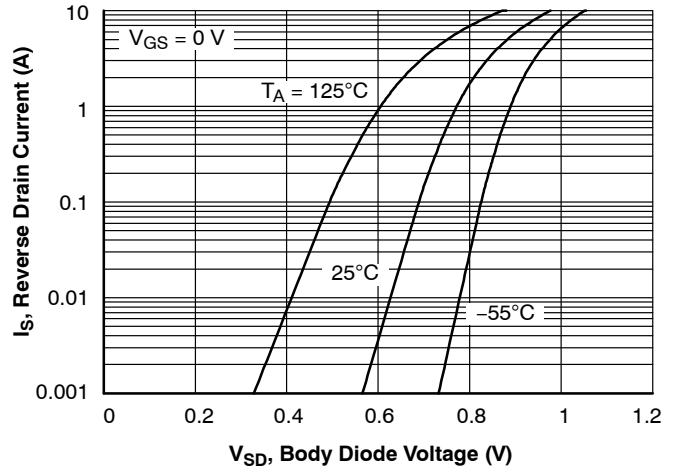


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

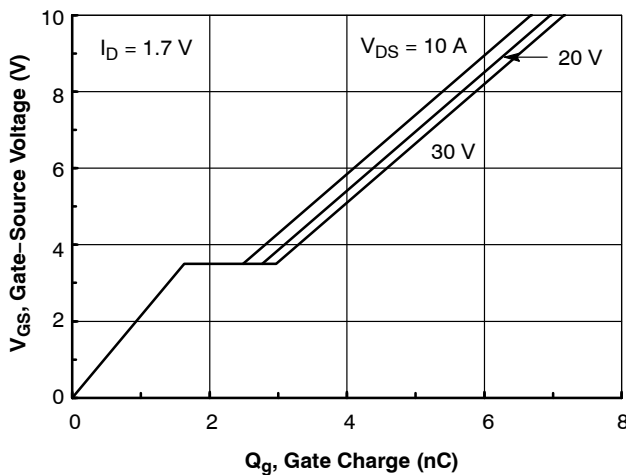


Figure 7. Gate Charge Characteristics

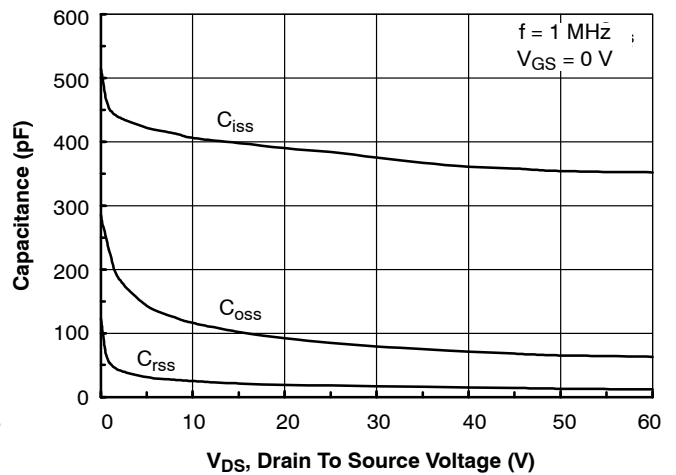


Figure 8. Capacitance Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

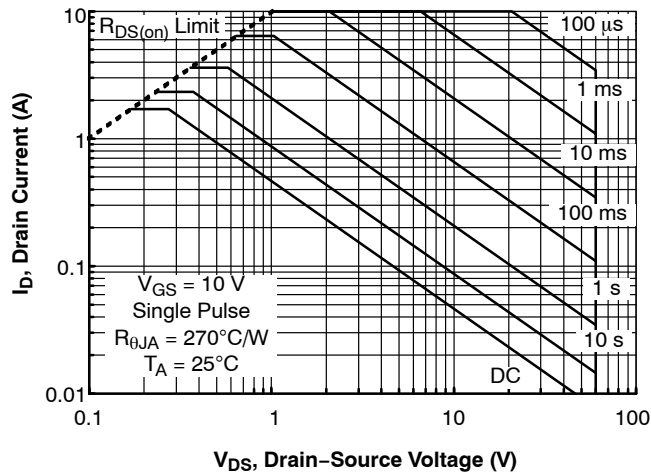


Figure 9. Maximum Safe Operating Area

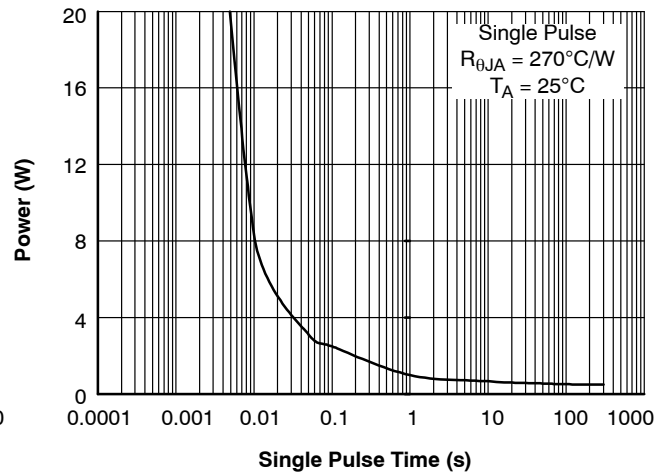


Figure 10. Single Pulse Maximum Power Dissipation

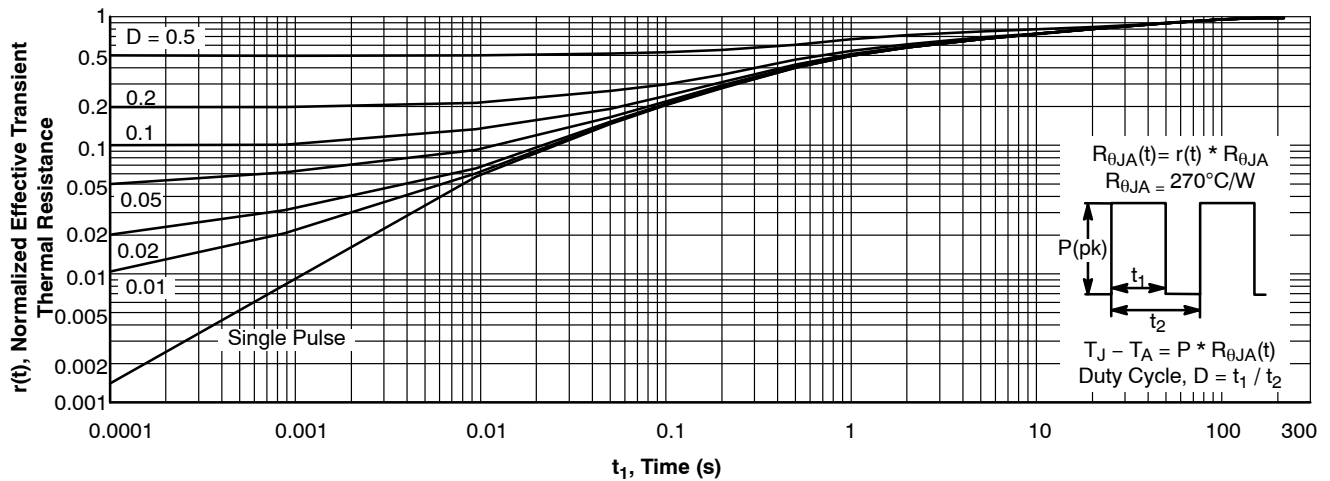


Figure 11. Transient Thermal Response Curve

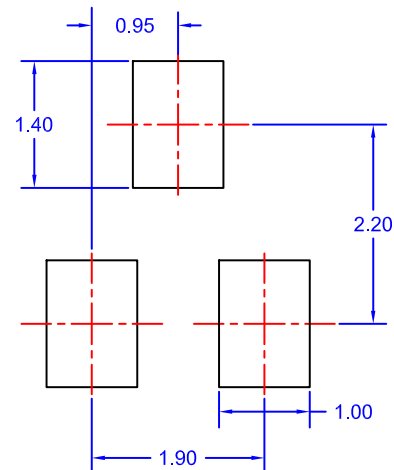
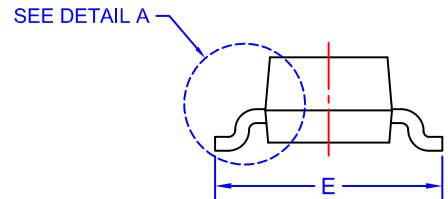
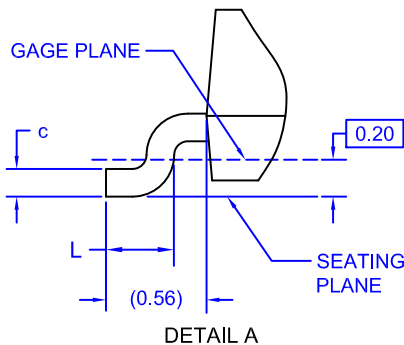
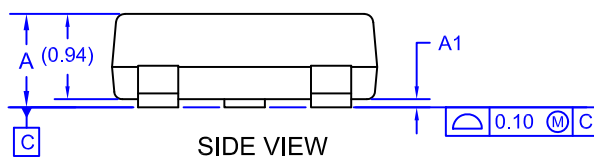
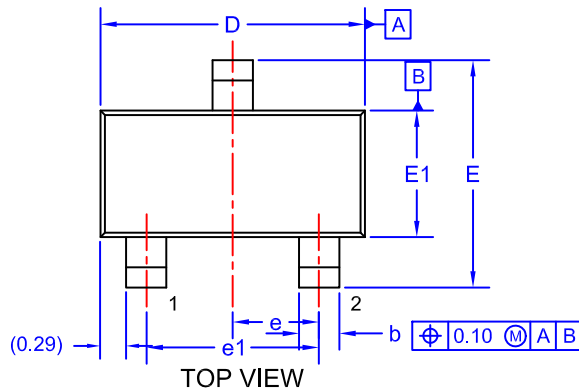
Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23/SUPERSOT™ –23, 3 LEAD, 1.4x2.9 CASE 527AG ISSUE A

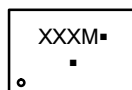
DATE 09 DEC 2019



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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