

# MOSFET – POWERTRENCH®

## N-Channel

80 V, 240 A, 2.0 mΩ

## FDBL86363-F085

### Features

- Typical  $R_{DS(on)} = 1.5 \text{ mΩ}$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 80 \text{ A}$
- Typical  $Q_{g(\text{tot})} = 130 \text{ nC}$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 80 \text{ A}$
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

### MOSFET MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	80	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous ( $V_{GS} = 10 \text{ V}$ , $T_C = 25^\circ\text{C}$ (Note 1))	240	A
	Pulsed Drain Current, $T_C = 25^\circ\text{C}$	See Figure 4	
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	512	mJ
$P_D$	Power Dissipation	357	W
	Derate Above $25^\circ\text{C}$	2.38	W/ $^\circ\text{C}$
$T_J$ , $T_{STG}$	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.42	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C}/\text{W}$

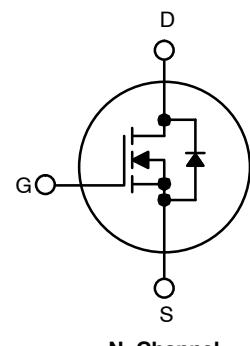
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.25 \text{ mH}$ ,  $I_{AS} = 64 \text{ A}$ ,  $V_{DD} = 80 \text{ V}$  during inductor charging and  $V_{DD} = 0 \text{ V}$  during time in avalanche.
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.



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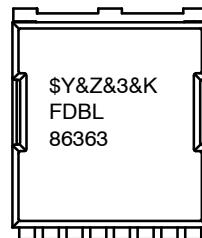


N-Channel



H-PSOF8L  
CASE 100CU

### MARKING DIAGRAM



\$Y = ON Semiconductor Logo  
&Z = Assembly Plant Code  
&3 = Numeric Date Code  
&K = Lot Code  
FDBL86363 = Specific Device Code

### ORDERING INFORMATION

Device	Top Mark	Package	Shipping <sup>†</sup>
FDBL86363-F085	FDBL86363	H-PSOF8L	2000 Units/ Tape&Reel

<sup>†</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# FDBL86363-F085

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
<b>OFF CHARACTERISTICS</b>							
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V		80	—	—	V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C	—	—	1	μA
			T <sub>J</sub> = 175°C (Note 4)	—	—	1	mA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>GS</sub> = ±20 V		—	—	±100	nA

## ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.0	3.0	4.0	V	
R <sub>DS(on)</sub>	Drain to Source on Resistance	I <sub>D</sub> = 80 A, V <sub>GS</sub> = 10 V	T <sub>J</sub> = 25°C	—	1.5	2.0	mΩ
			T <sub>J</sub> = 175°C (Note 4)	—	3.1	4.1	mΩ

## DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz	—	10000	—	pF	
C <sub>oss</sub>	Output Capacitance		—	1540	—	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance		—	70	—	pF	
R <sub>g</sub>	Gate Resistance	f = 1 MHz	—	2.8	—	Ω	
Q <sub>g(ToT)</sub>	Total Gate Charge at 10 V	V <sub>GS</sub> = 0 to 10 V	V <sub>DD</sub> = 64 V, I <sub>D</sub> = 80 A	—	130	169	nC
	Threshold Gate Charge		V <sub>GS</sub> = 0 to 2 V	—	18	27	nC
Q <sub>gs</sub>	Gate-to-Source Gate Charge	V <sub>DD</sub> = 64 V, I <sub>D</sub> = 80 A	—	47	—	nC	
Q <sub>gd</sub>	Gate-to-Drain "Miller" Charge		—	24	—	nC	

## SWITCHING CHARACTERISTICS

t <sub>on</sub>	Turn-On Time	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 80 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	—	—	133	ns
t <sub>d(on)</sub>	Turn-On Delay		—	39	—	ns
t <sub>r</sub>	Rise Time		—	63	—	ns
t <sub>d(off)</sub>	Turn-Off Delay		—	61	—	ns
t <sub>f</sub>	Fall Time		—	33	—	ns
t <sub>off</sub>	Turn-Off Time		—	—	140	ns

## DRAIN-SOURCE DIODE CHARACTERISTIC

V <sub>SD</sub>	Source-to-Drain Diode Voltage	I <sub>SD</sub> = 80 A, V <sub>GS</sub> = 0 V	—	—	1.25	V
		I <sub>SD</sub> = 40 A, V <sub>GS</sub> = 0 V	—	—	1.2	V
t <sub>rr</sub>	Reverse-Recovery Time	I <sub>F</sub> = 80 A, dI <sub>SD</sub> /dt = 100 A/μs, V <sub>DD</sub> = 64 V	—	83	108	ns
			—	118	153	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T<sub>J</sub> = 175°C. Product is not tested to this condition in production.

## TYPICAL CHARACTERISTICS

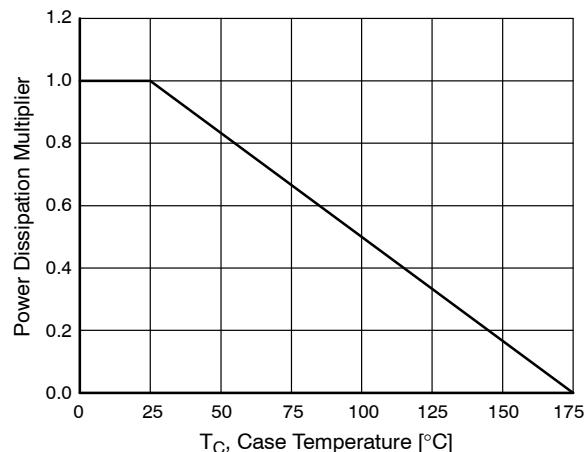


Figure 1. Normalized Power Dissipation  
vs. Case Temperature

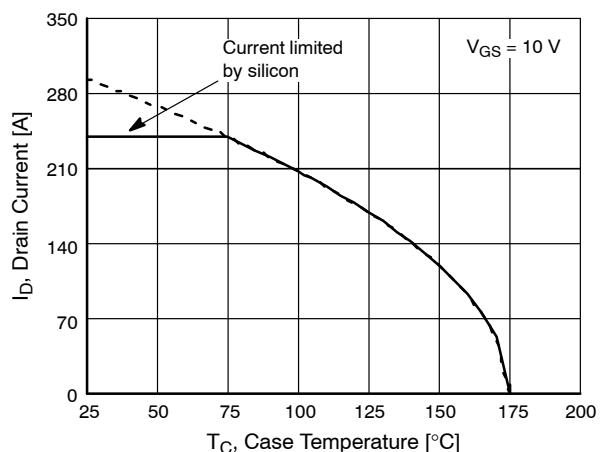


Figure 2. Maximum Continuous Drain Current  
vs. Case Temperature

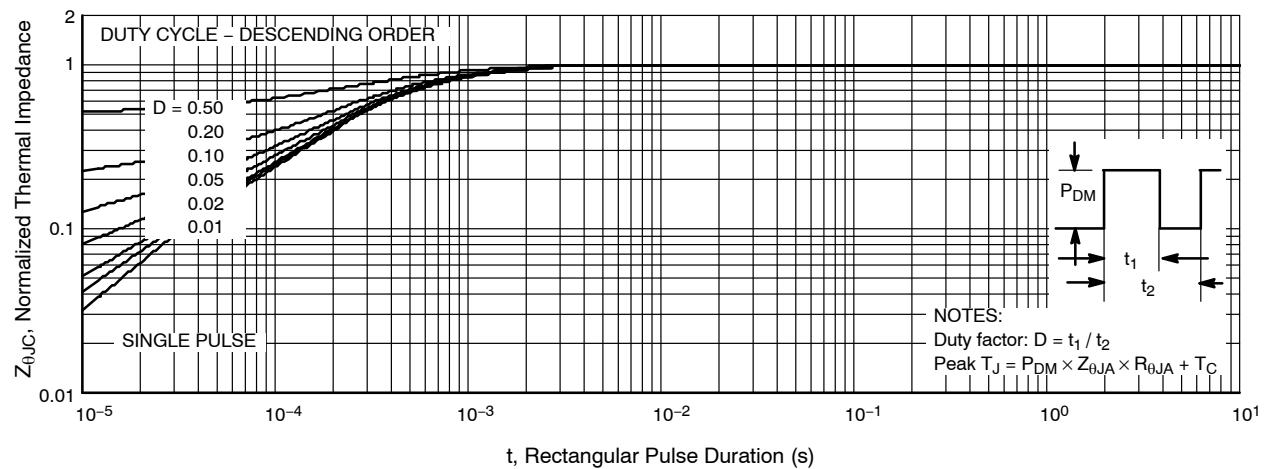


Figure 3. Normalized Maximum Transient Thermal Impedance

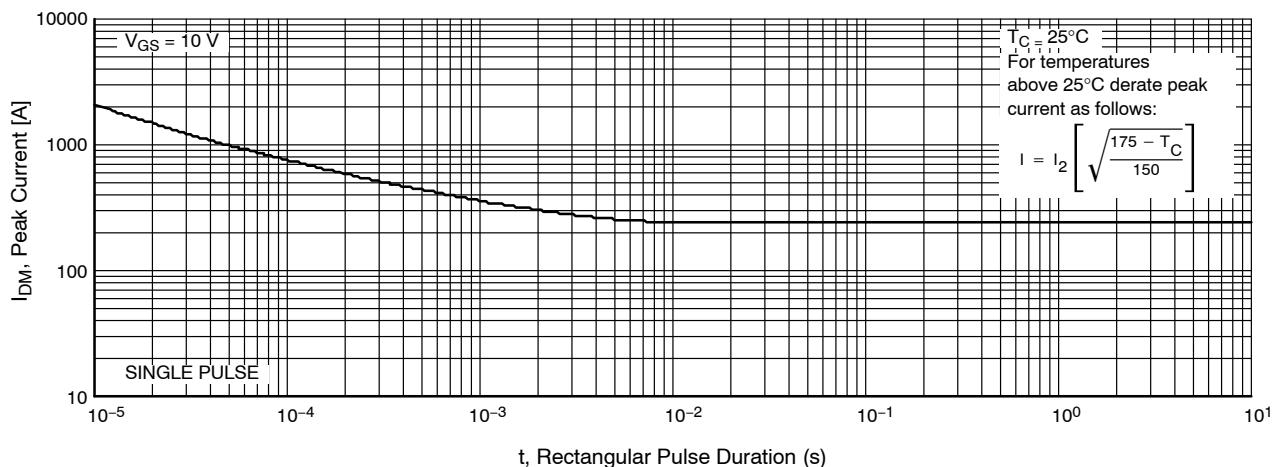
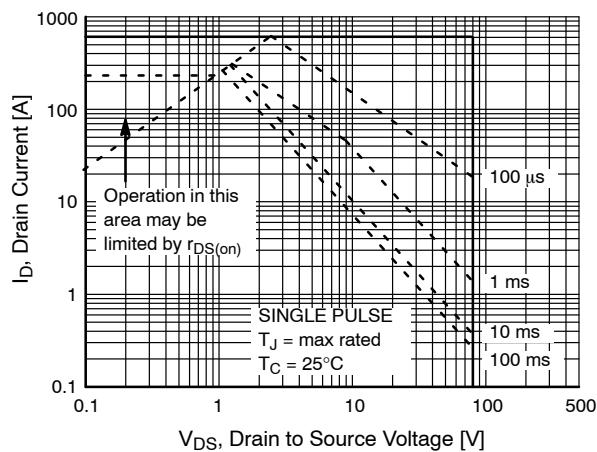
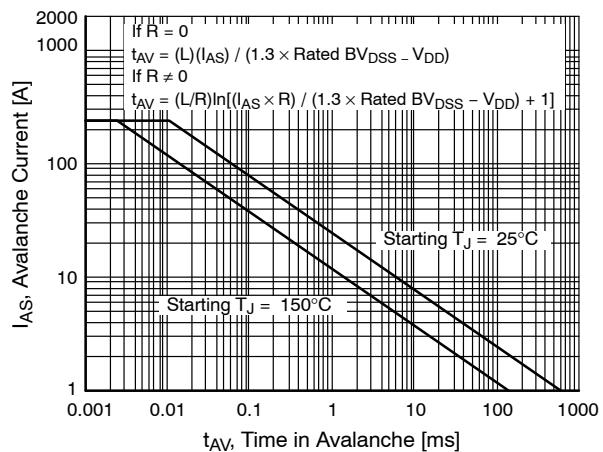


Figure 4. Peak Current Capability

**TYPICAL CHARACTERISTICS (continued)**

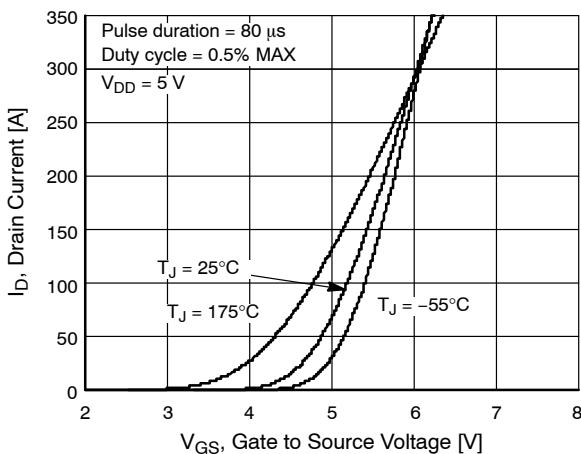


**Figure 5. Forward Bias Safe Operating Area**

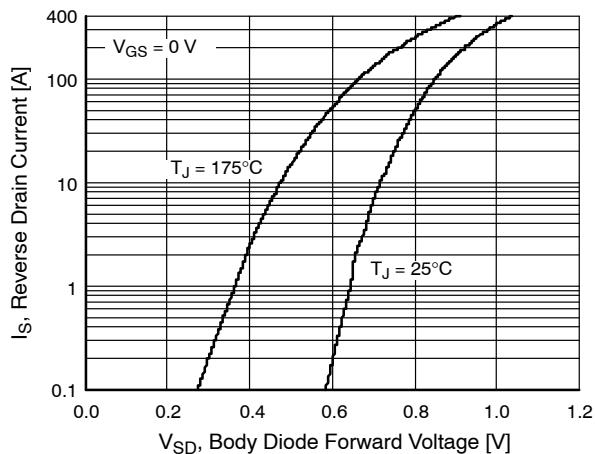


NOTE: Refer to ON Semiconductor Application Notes [AN7514](#) and [AN7515](#).

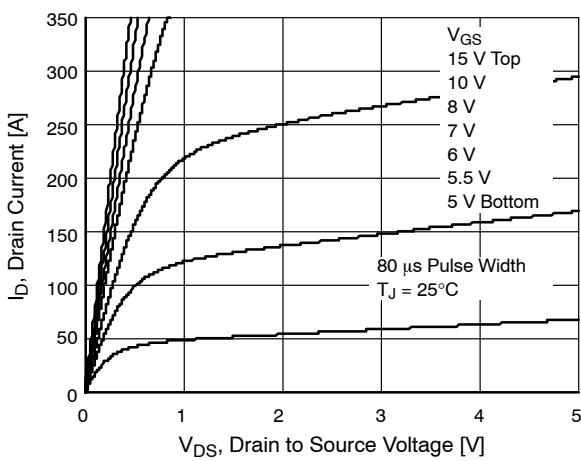
**Figure 6. Unclamped Inductive Switching Capability**



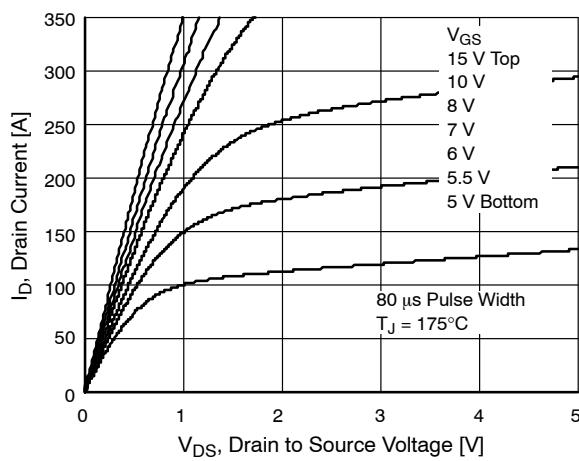
**Figure 7. Transfer Characteristics**



**Figure 8. Forward Diode Characteristics**

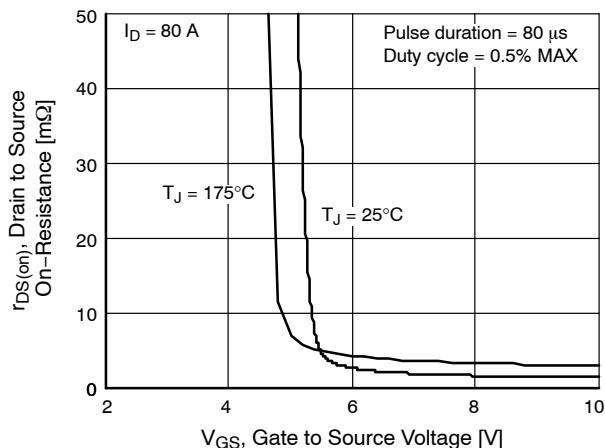


**Figure 9. Saturation Characteristics**

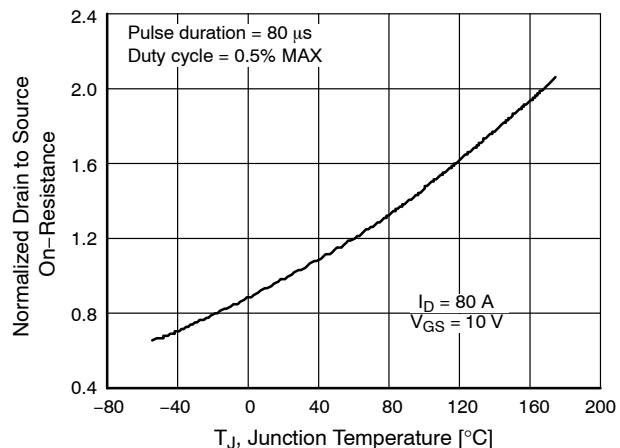


**Figure 10. Saturation Characteristics**

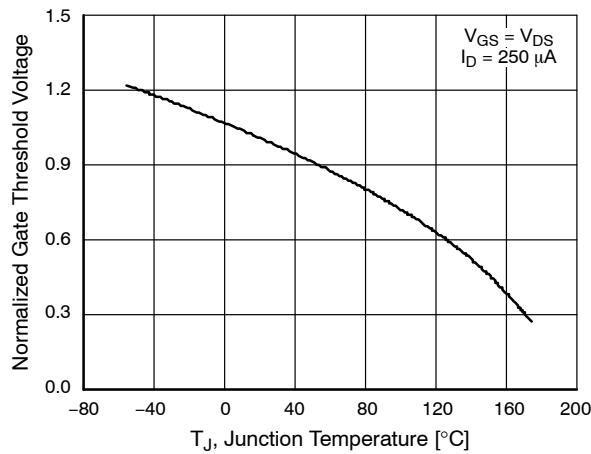
**TYPICAL CHARACTERISTICS (continued)**



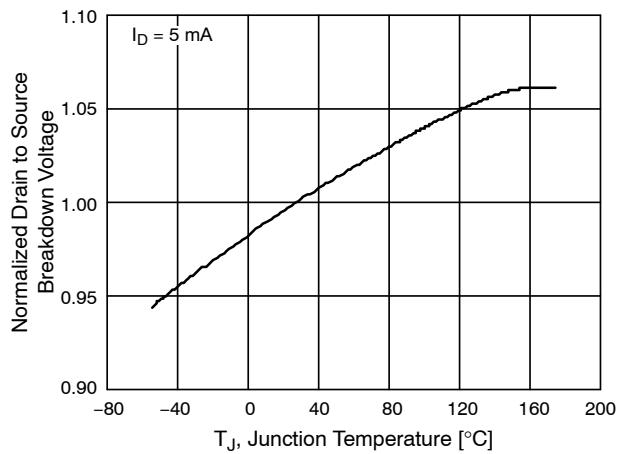
**Figure 11.  $R_{DS(on)}$  vs. Gate Voltage**



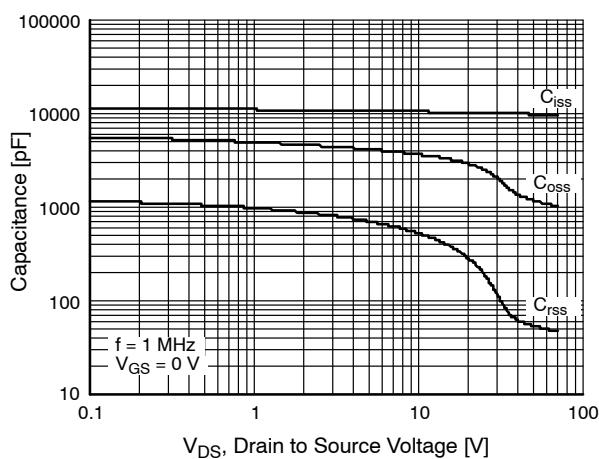
**Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature**



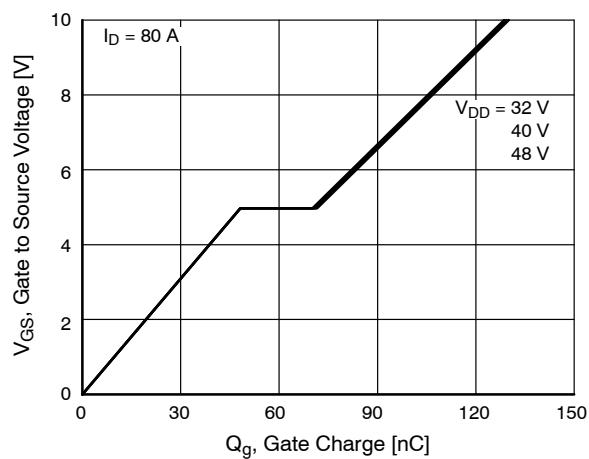
**Figure 13. Normalized Gate Threshold Voltage vs. Temperature**



**Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature**



**Figure 15. Capacitance vs. Drain to Source Voltage**



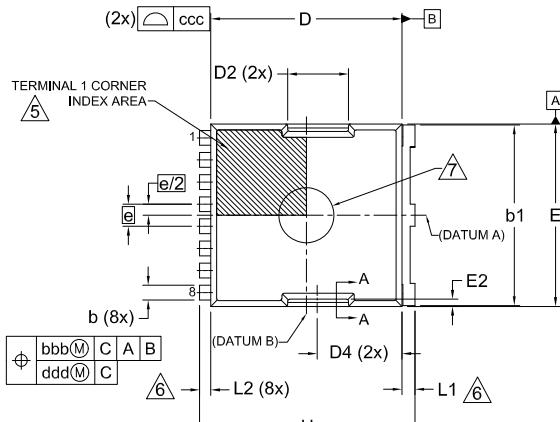
**Figure 16. Gate Charge vs. Gate to Source Voltage**

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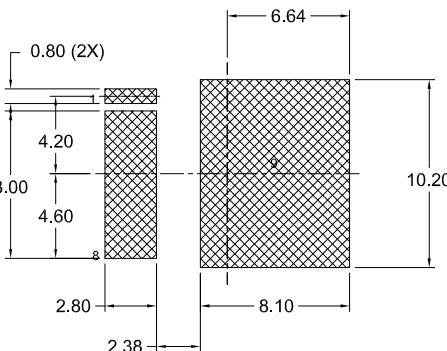
**H-PSOF8L 11.68x9.80x2.30, 1.20P**  
CASE 100CU  
ISSUE E

DATE 31 MAY 2024



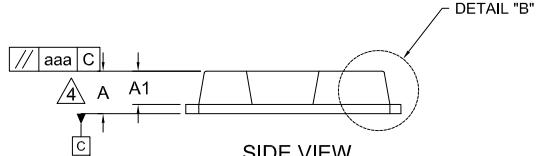
TOP VIEW

SECTION "A-A"  
SCALE: 2X

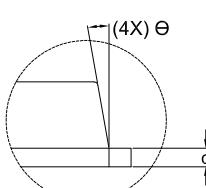


LAND PATTERN  
RECOMMENDATION

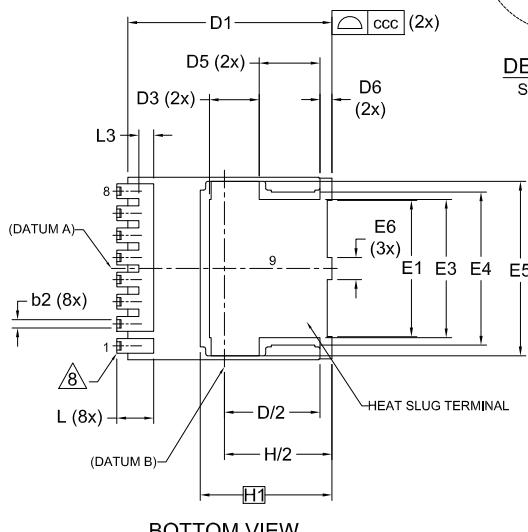
\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SODERRM/D.



SIDE VIEW

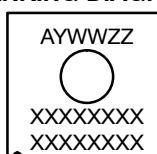


DETAIL "B"  
SCALE: 2X



BOTTOM VIEW

**GENERIC  
MARKING DIAGRAM\***



**A** = Assembly Location  
**Y** = Year  
**WW** = Work Week  
**ZZ** = Assembly Lot Code  
**XXXX** = Specific Device Code

**NOTES:**

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1, L1, L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

DIM	MILLIMETERS			DIM	MILLIMETERS		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	2.20	2.30	2.40	E5	9.36	9.46	9.47
A1	1.70	1.80	1.90	E6	1.10	1.20	1.30
b	0.70	0.80	0.90	E7	0.15	0.18	0.21
b1	9.70	9.80	9.90	e	1.20 BSC		
b2	0.35	0.45	0.55	e/2	0.60 BSC		
c	0.40	0.50	0.60	H	11.58	11.68	11.78
D	10.28	10.38	10.48	H/2	5.74	5.84	5.94
D/2	5.09	5.19	5.29	H1	7.15 BSC		
D1	10.98	11.08	11.18	L	1.90	2.00	2.10
D2	3.20	3.30	3.40	L1	0.60	0.70	0.80
D3	2.60	2.70	2.80	L2	0.50	0.60	0.70
D4	4.45	4.55	4.65	L3	0.70	0.80	0.90
D5	3.20	3.30	3.40	Θ	10° REF		
D6	0.55	0.65	0.75	Θ1	10° REF		
E	9.80	9.90	10.00	aaa	0.20		
E1	7.30	7.40	7.50	bbb	0.25		
E2	0.30	0.40	0.50	ccc	0.20		
E3	7.40	7.50	7.60	ddd	0.20		
E4	8.20	8.30	8.40	eee	0.10		

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	H-PSOF8L 11.68x9.80x2.30, 1.20P	PAGE 1 OF 1

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