

MOSFET – N-Channel, UniFET™

300 V, 38 A, 85 mΩ

FDA38N30

Description

UniFET MOSFET is onsemi's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

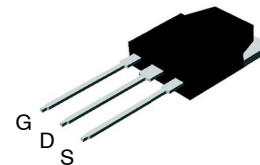
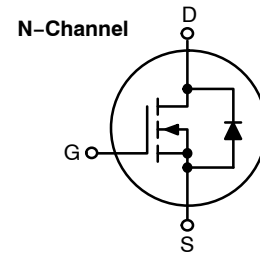
Features

- $R_{DS(on)} = 70 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 19 \text{ A}$
- Low Gate Charge (Typ. 60 nC)
- Low C_{rss} (Typ. 60 pF)
- 100% Avalanche Tested
- ESD Improved Capability
- RoHS Compliant

Applications

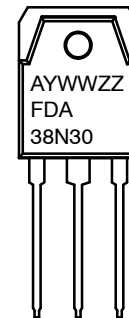
- PDP TV
- Uninterruptible Power Supply
- AC-DC Power Supply

V_{DS}	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
300 V	85 mΩ @ 10 V	38 A



TO-3P-3LD / EIAJ SC-65, ISOLATED
 CASE 340BZ

MARKING DIAGRAM



- A = Assembly Site
- YWW = Date Code (Year & Work Week)
- ZZ = Assembly Lot Number
- FDA38N30 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FDA38N30	TO-3P-3LD	450 Units / Tube

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MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	300	V
V_{GSS}	Gate to Source Voltage	± 30	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	38
		- Continuous ($T_C = 100^\circ\text{C}$)	22
		- Pulsed (Note 1)	150
I_{DM}			A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	1200	mJ
I_{AR}	Avalanche Current (Note 1)	38	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	31	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	312
		-Derate above = 25°C	2.5
			W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 1.7\text{ mH}$, $I_{AS} = 38\text{ A}$, $V_{DD} = 50\text{ V}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 38\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$, $T_C = 25^\circ\text{C}$	300	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C	–	0.3	–	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 300 \text{ V}$, $V_{GS} = 0 \text{ V}$	–	–	1	μA
		$V_{DS} = 240 \text{ V}$, $T_C = 125^\circ\text{C}$	–	–	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0 \text{ V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 19 \text{ A}$	–	0.070	0.085	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}$, $I_D = 19 \text{ A}$	–	6.3	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	–	2600	–	pF
C_{oss}	Output Capacitance		–	500	–	pF
C_{rss}	Reverse Transfer Capacitance		–	60	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 240 \text{ V}$, $I_D = 38 \text{ A}$, $V_{GS} = 10 \text{ V}$ (Note 4)	–	60	–	nC
Q_{gs}	Gate to Source Gate Charge		–	17	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	28	–	nC

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 150 \text{ V}$, $I_D = 38 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_G = 25 \Omega$ (Note 4)	–	53	69	ns
t_r	Turn–On Rise Time		–	110	143	ns
$t_{d(off)}$	Turn–Off Delay Time		–	118	153	ns
t_f	Turn–Off Fall Time		–	54	70	ns

DRAIN–SOURCE DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain to Source Diode Forward Current	–	–	38	A	
I_{SM}	Maximum Pulsed Drain–Source Diode Forward Current	–	–	150	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 38 \text{ A}$	–	–	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$, $I_{SD} = 38 \text{ A}$, $dI_F/dt = 100 \text{ A}/\mu\text{s}$	–	315	–	ns
Q_{rr}	Reverse Recovery Charge		–	4.0	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

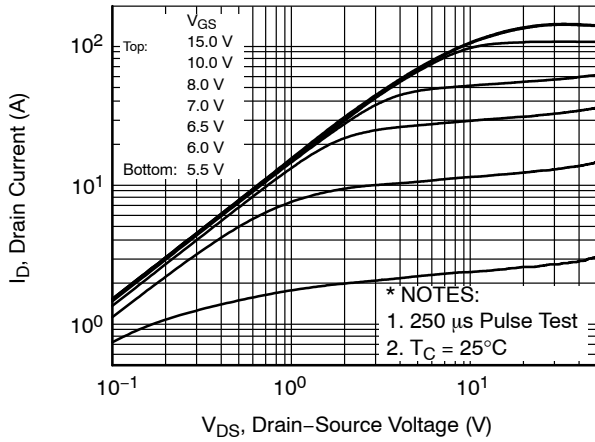


Figure 1. On-Region Characteristics

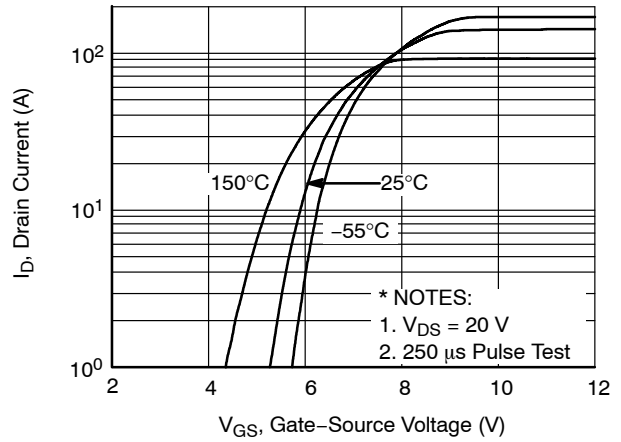


Figure 2. Transfer Characteristics

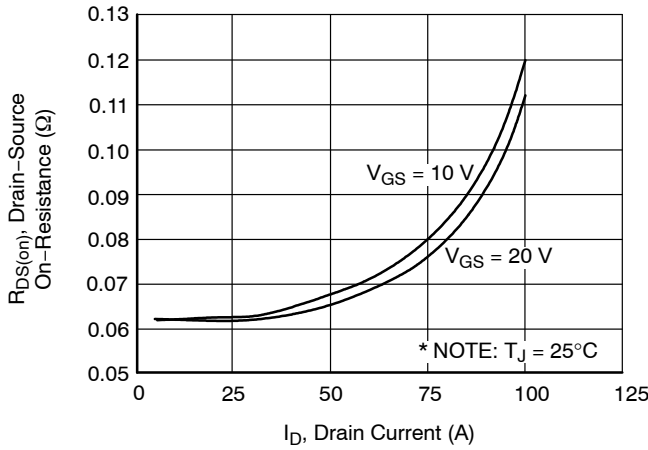


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

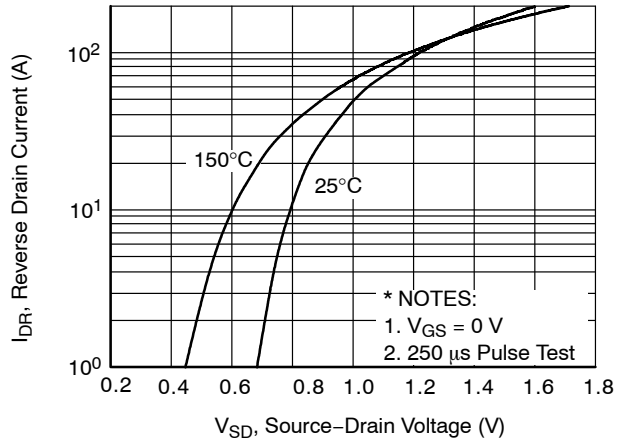


Figure 4. Body Diode Forward Voltage Variation vs. Source Current And Temperature

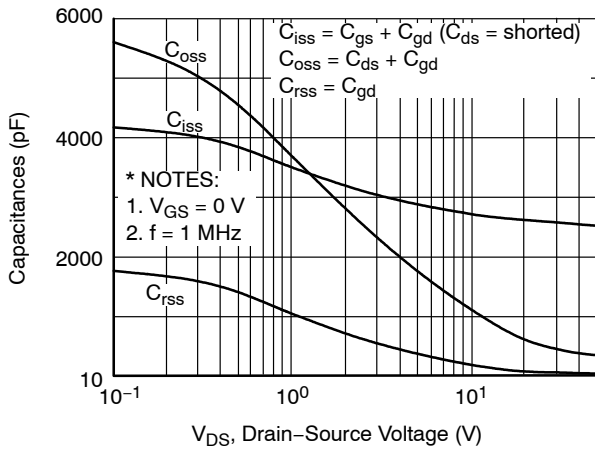


Figure 5. Capacitance Characteristics

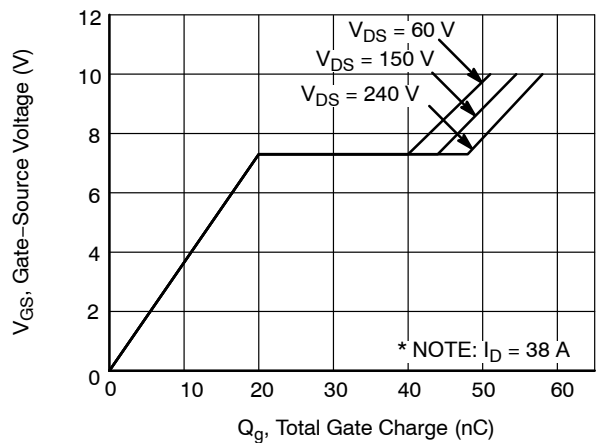


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

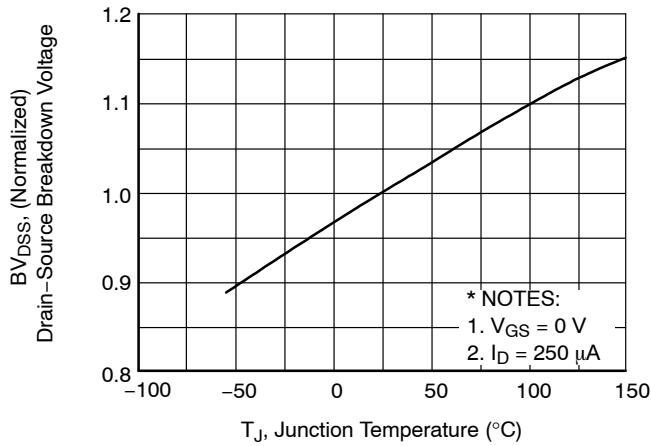


Figure 7. Breakdown Voltage Variation vs. Temperature

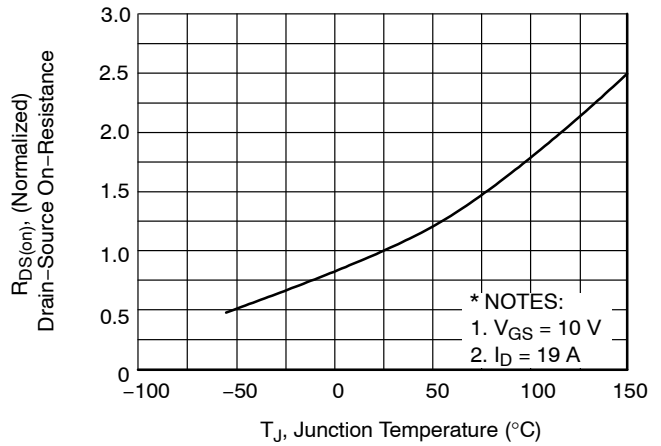


Figure 8. On-Resistance Variation vs. Temperature

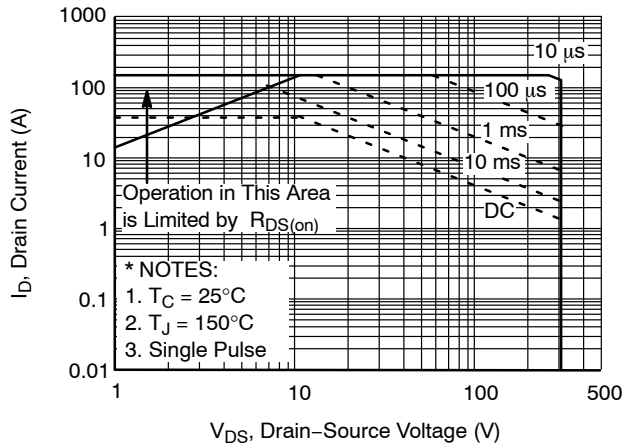


Figure 9. Maximum Safe Operating Area

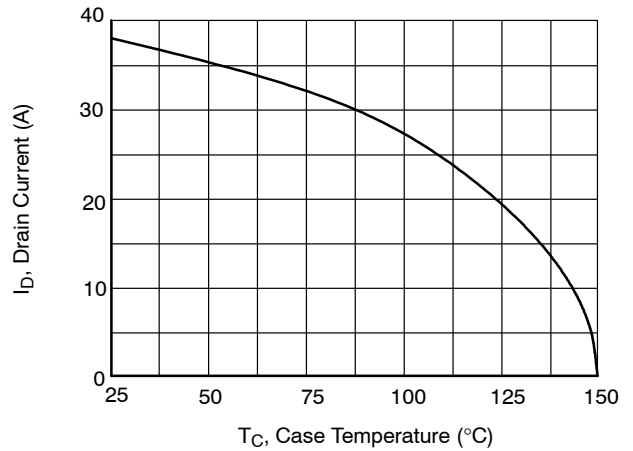


Figure 10. Maximum Drain Current vs. Case Temperature

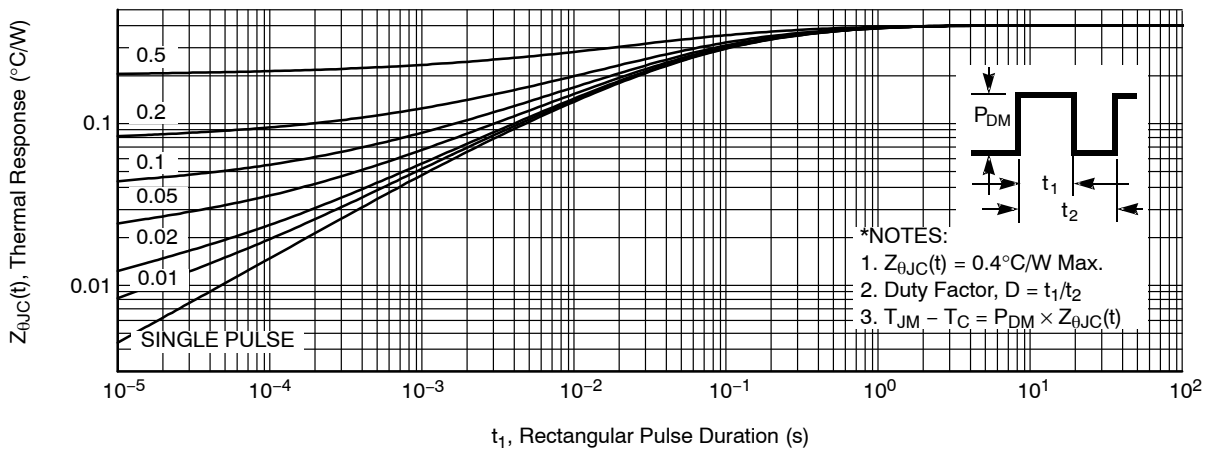


Figure 11. Transient Thermal Response Curve

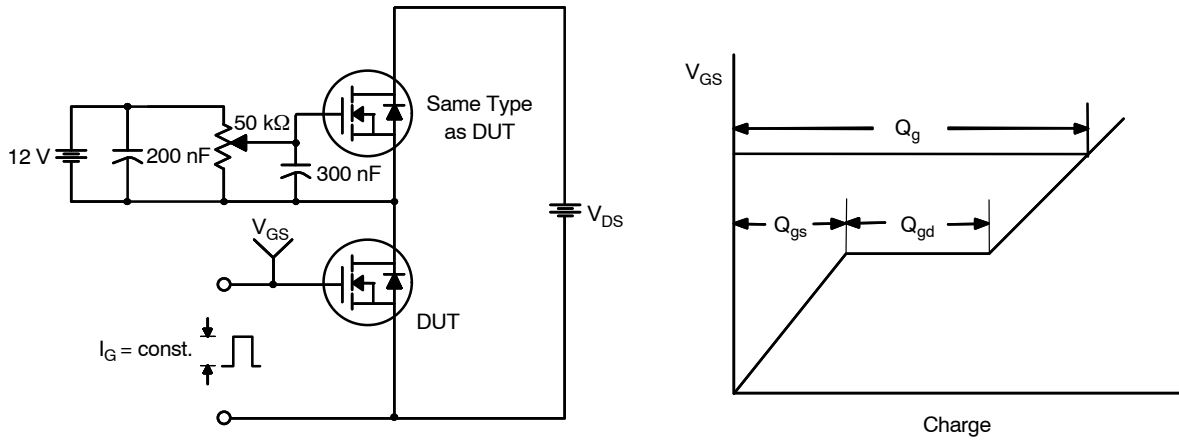


Figure 12. Gate Charge Test Circuit & Waveform

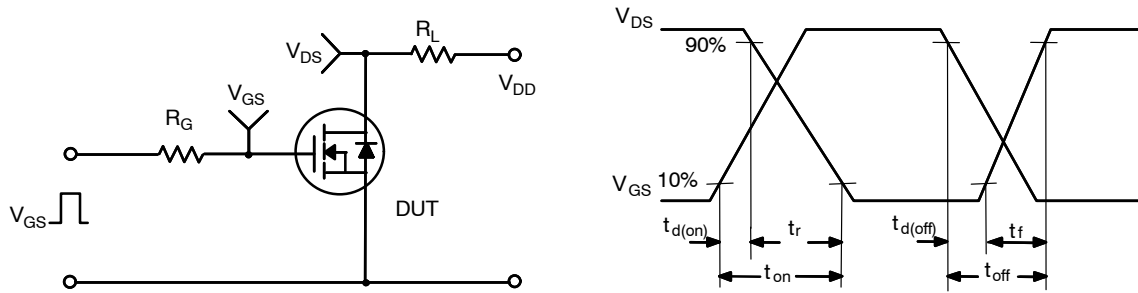


Figure 13. Resistive Switching Test Circuit & Waveforms

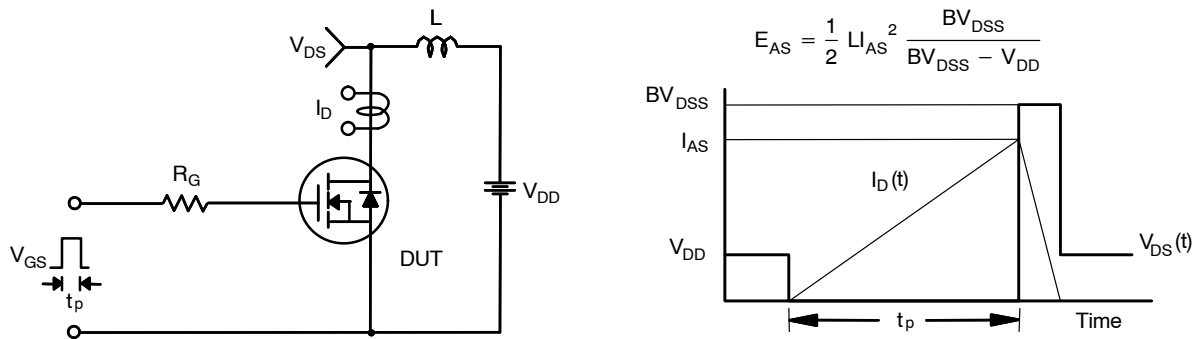


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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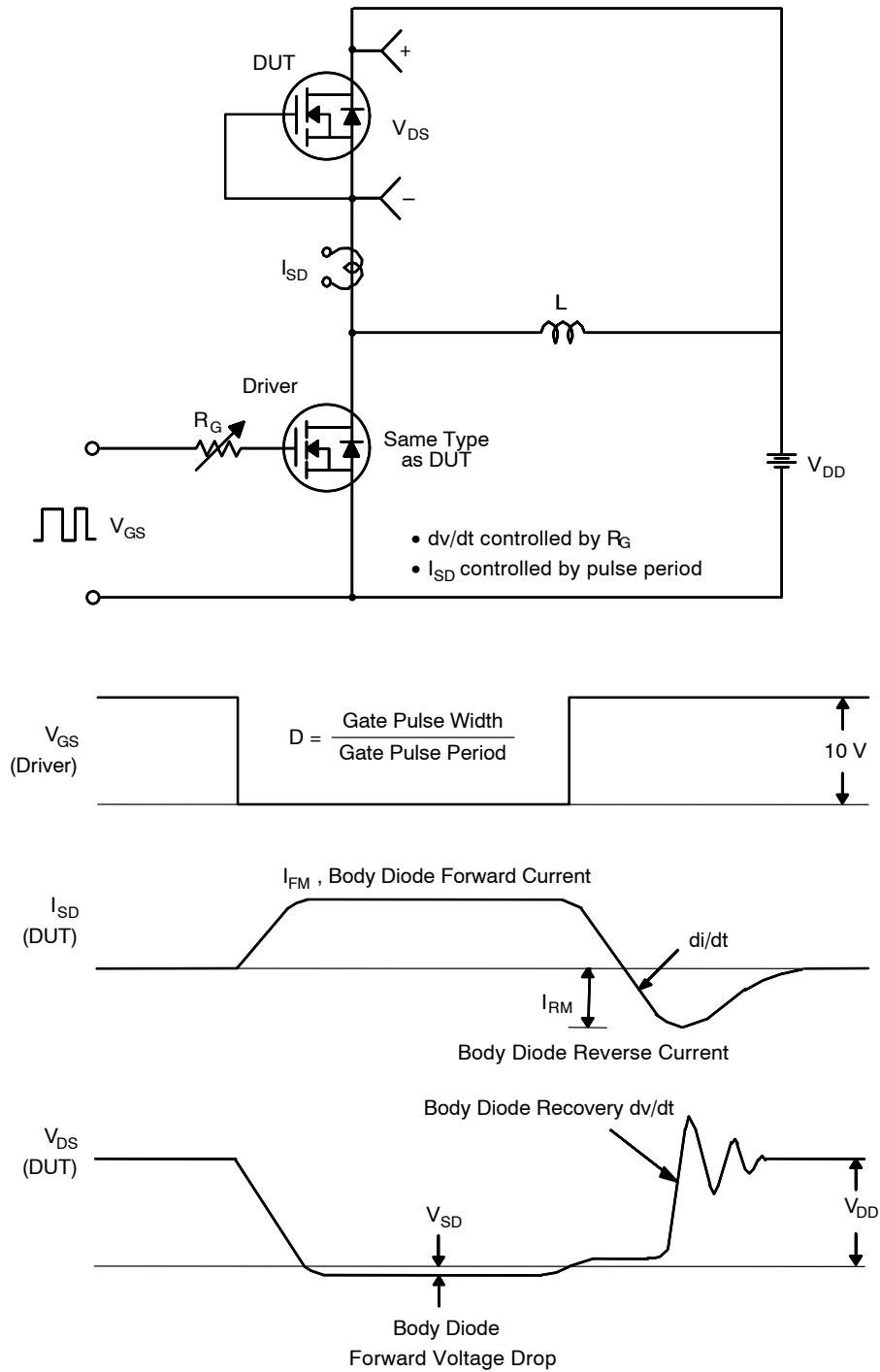


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

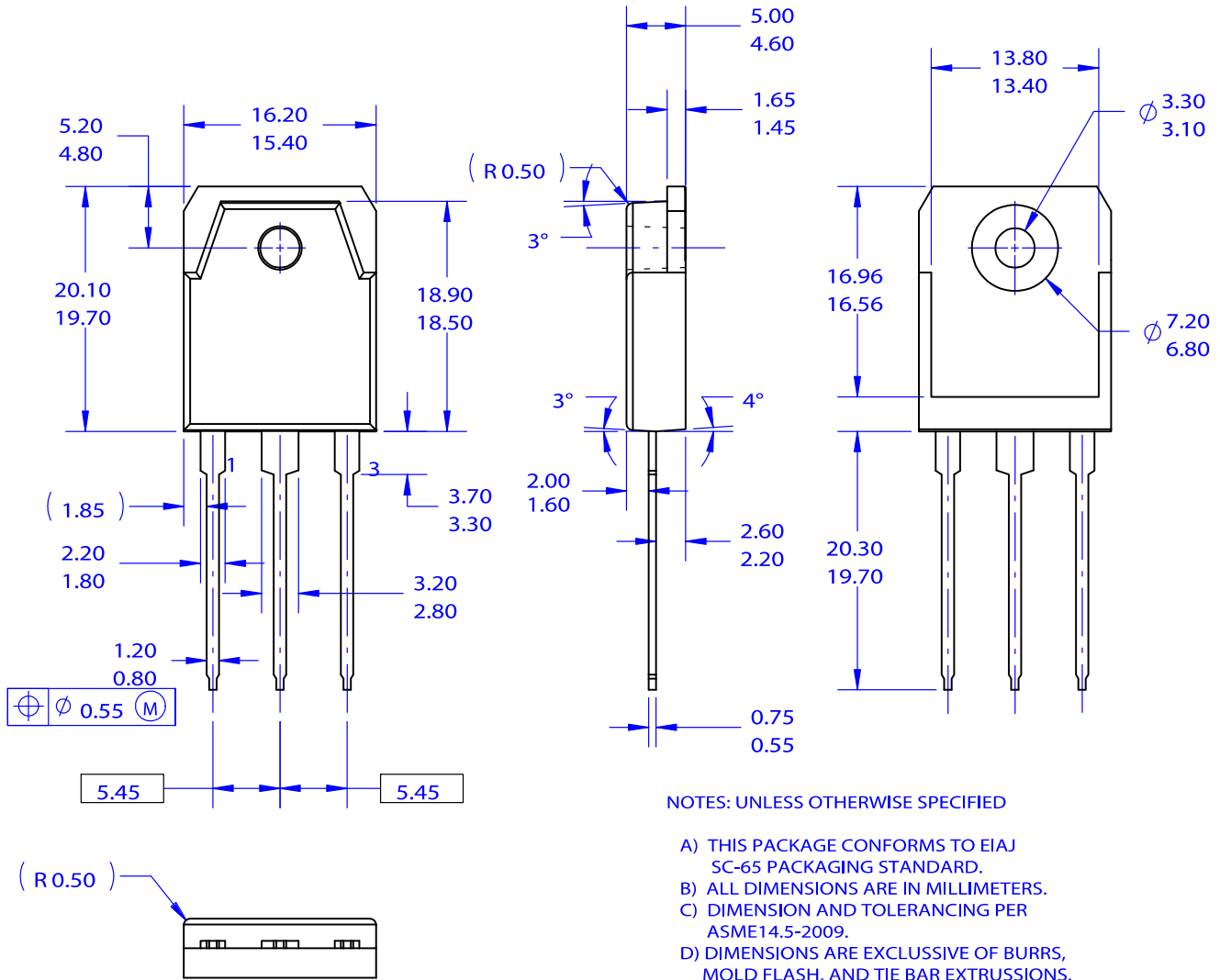
PACKAGE DIMENSIONS

ON Semiconductor®



TO-3P-3LD / EIAJ SC-65, ISOLATED CASE 340BZ ISSUE O

DATE 31 OCT 2016



NOTES: UNLESS OTHERWISE SPECIFIED

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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
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- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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