

MOSFET – N-Channel, SUPERFET II

600 V, 28 A, 130 mΩ

FCH130N60

Description

SUPERFET® II MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SUPERFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.

Features

- 650 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 112\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 54\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 240\text{ pF}$)
- 100% Avalanche Tested
- This Device is Pb-Free and is RoHS Compliant

Applications

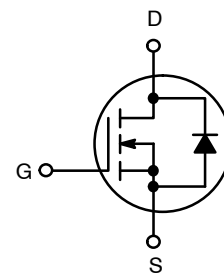
- Telecom / Server Power Supplies
- Industrial Power Supplies
- AC-DC Power Supply



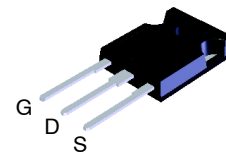
ON Semiconductor®

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V_{DS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
600 V	130 mΩ	28 A

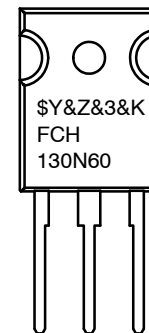


N-Channel MOSFET



TO-247
CASE 340CK

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot Code
FCH130N60	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCH130N60

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		FCH130N60	Unit
V _{DSS}	Drain to Source Voltage		600	V
V _{GSS}	Gate to Source Voltage	– DC	±20	V
		– AC (f > 1 Hz)	±30	
I _D	Drain Current	– Continuous (T _C = 25°C)	28	A
		– Continuous (T _C = 100°C)	18	
I _{DM}	Drain Current	– Pulsed (Note 1)	84	A
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		720	mJ
I _{AR}	Avalanche Current (Note 1)		6	A
E _{AR}	Repetitive Avalanche Energy (Note 1)		2.78	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P _D	Power Dissipation	(T _C = 25°C)	278	W
		– Derate Above 25°C	2.2	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		–55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.

2. I_{AS} = 6 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.

3. I_{SD} ≤ 14 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FCH130N60	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.45	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH130N60	FCH130N60	TO-247	Tube	N/A	N/A	30 Units

FCH130N60

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 10 mA, T _J = 25°C	600	–	–	V
		V _{GS} = 0 V, I _D = 10 mA, T _J = 150°C	650	–	–	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	–	0.67	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 480 V, V _{GS} = 0 V, T _C = 125°C	–	2.5	–	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.5	–	3.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 14 A	–	112	130	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 14 A	–	26	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz	–	2700	3590	pF
C _{oss}	Output Capacitance		–	65	85	pF
C _{rss}	Reverse Transfer Capacitance		–	2.85	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	–	240	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 380 V, I _D = 14 A, V _{GS} = 10 V (Note 4)	–	54	70	nC
Q _{gs}	Gate to Source Gate Charge		–	12	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	14	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 380 V, I _D = 14 A, V _{GS} = 10 V, R _G = 4.7 Ω (Note 4)	–	25	60	ns
t _r	Turn-On Rise Time		–	16	42	ns
t _{d(off)}	Turn-Off Delay Time		–	65	140	ns
t _f	Turn-Off Fall Time		–	4	18	ns

DRAIN-SOURCE- DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain to Source Diode Forward Current		–	–	28	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	84	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 14 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 14 A, dI _F /dt = 100 A/μs	–	376	–	ns
Q _{rr}	Reverse Recovery Charge		–	7.6	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

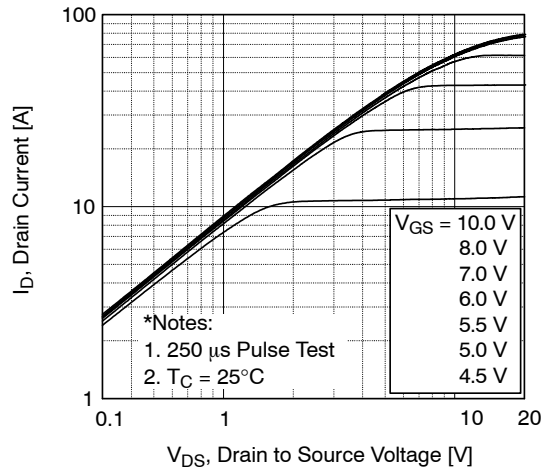


Figure 1. On-Region Characteristics

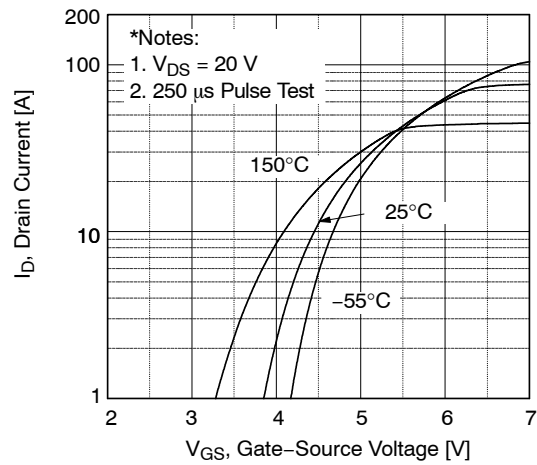


Figure 2. Transfer Characteristics

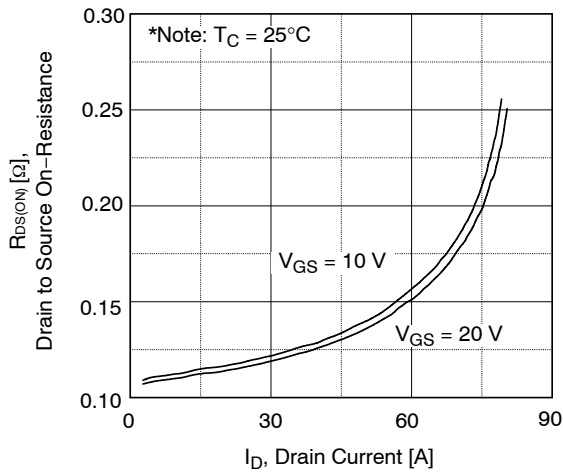


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

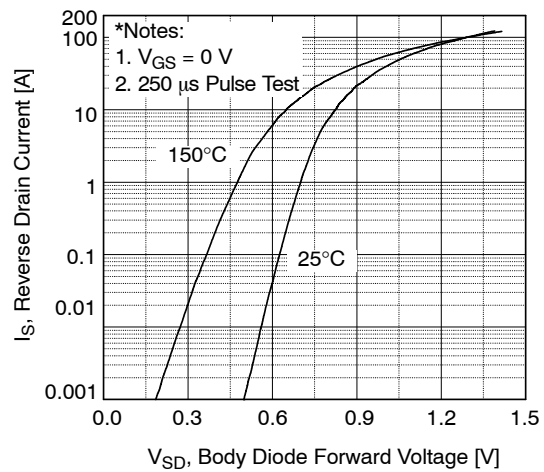


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

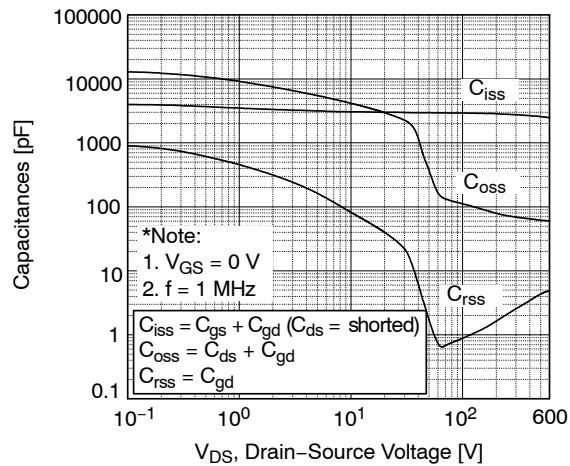


Figure 5. Capacitance Characteristics

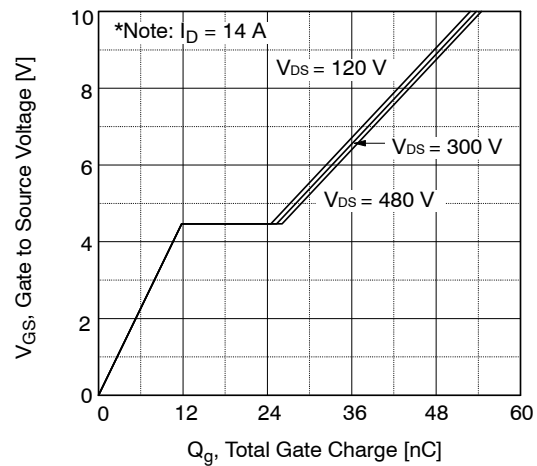


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

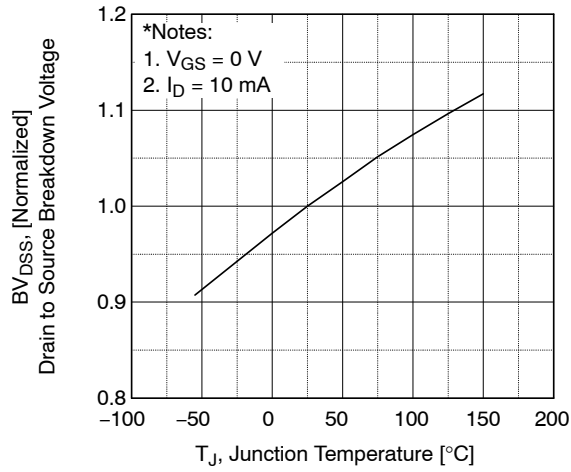


Figure 7. Breakdown Voltage Variation vs. Temperature

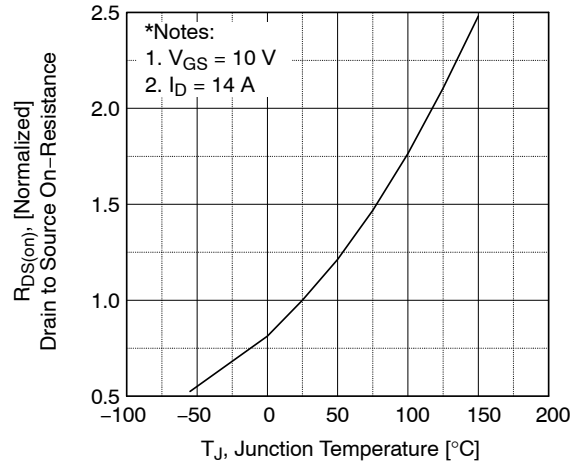


Figure 8. On-Resistance Variation vs. Temperature

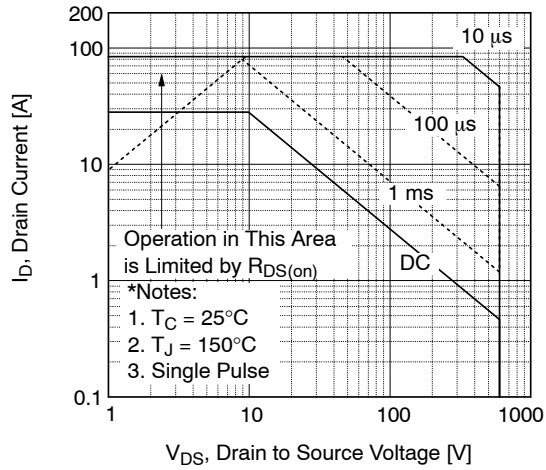


Figure 9. Maximum Safe Operation Area

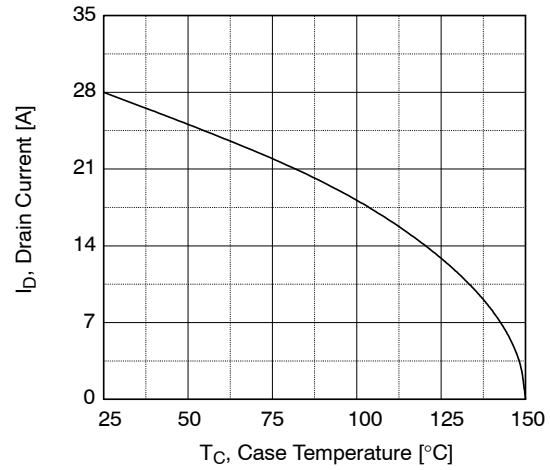


Figure 10. Maximum Drain Current vs. Case Temperature

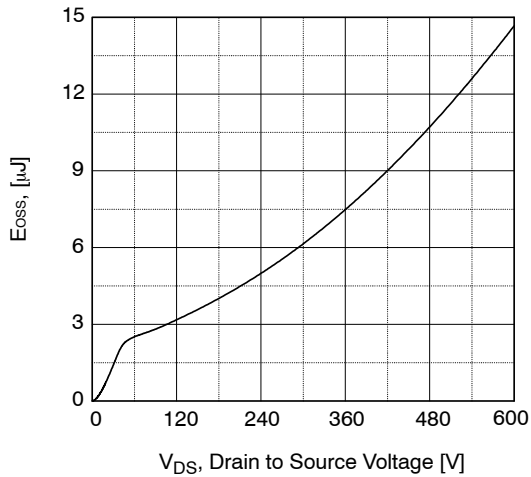


Figure 11. E_{OSS} vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

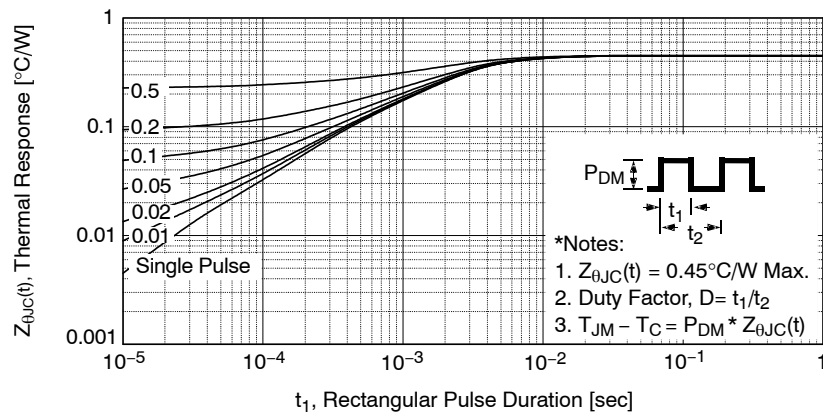


Figure 12. Transient Thermal Response Curve

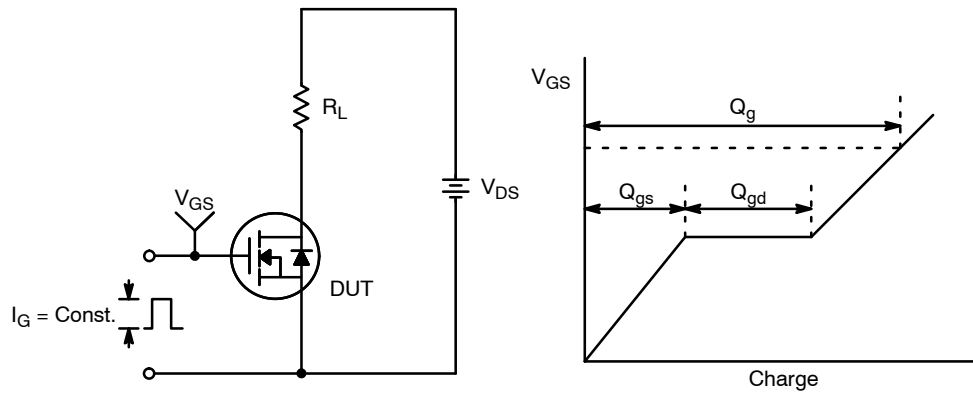


Figure 13. Gate Charge Test Circuit & Waveform

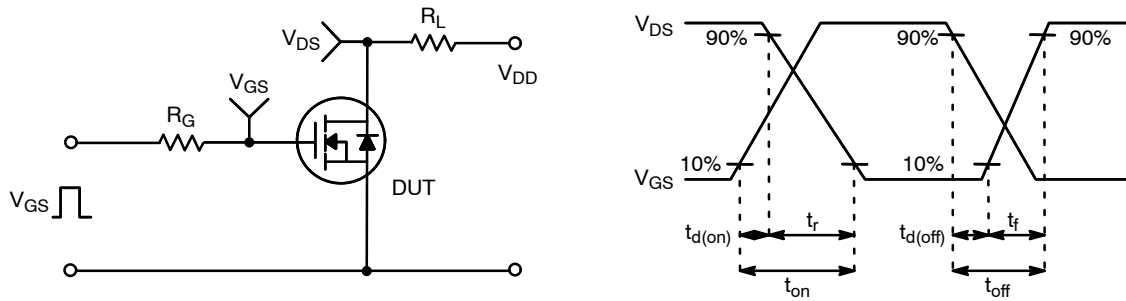


Figure 14. Resistive Switching Test Circuit & Waveforms

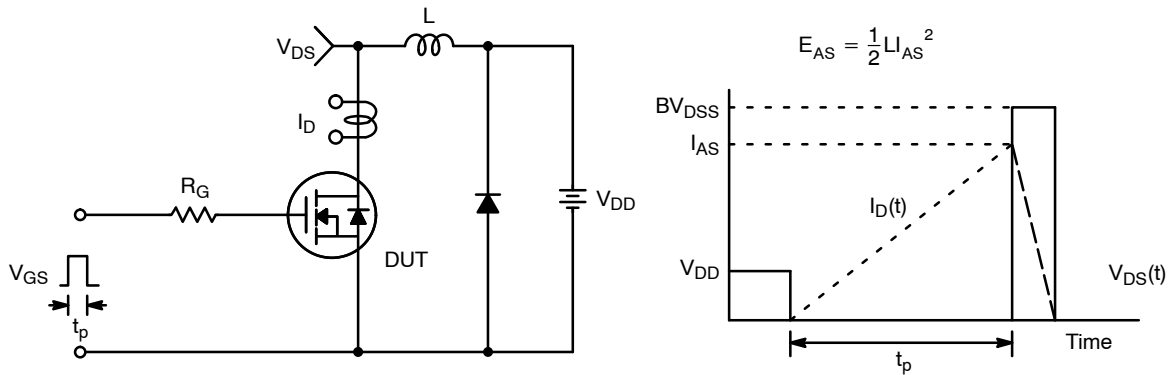


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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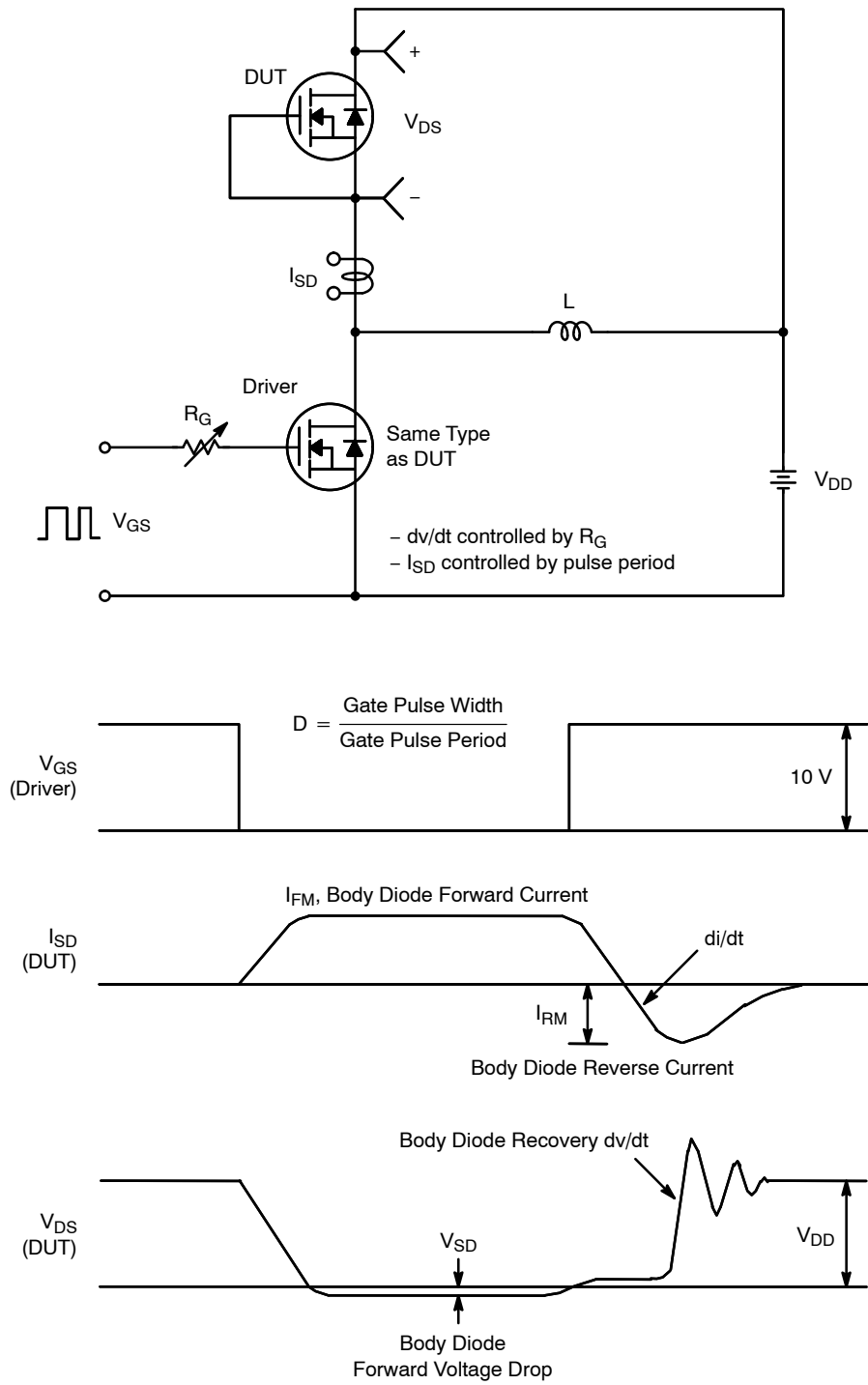


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO-247-3LD SHORT LEAD CASE 340CK ISSUE A

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ϕP	3.51	3.58	3.65
$\phi P1$	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

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