



*Quality Through Innovation Since 1987*

**HIGH-SPEED DMOS  
FET ANALOG SWITCHES  
AND SWITCH ARRAYS**

## Introduction

This Application Note describes in detail the principle of operation of the SD210/5000 series of high-speed analog switches and switch arrays. It contains an explanation of the most important switch characteristics, application examples, test data, and other application hints.

## Description

The Linear Systems [SD210](#) and SD5000 series are discretes and quad monolithic arrays, respectively, of single-pole single-throw analog switches. These switches are n-channel enhancement-mode silicon field effect transistors built using double-diffusion MOS (DMOS) silicon gate technology. Surface mount versions ([SST211](#), [SD5400](#) Series) are also available.

This family of devices is designed to handle a wide variety of video, fast ATE, and telecom analog switching applications. They are capable of ultrafast switching speeds ( $t_r = 1$  ns,  $t_{OFF} = 3$  ns) and excellent transient response. Thanks to the reduced parasitic capacitances, DMOS can handle wideband signals with high off-isolation and minimum crosstalk.

The [SD210](#) series of single-channel FETs is produced without Zener protection to reduce leakage and in Zener protected versions to reduce electrostatic discharge hazards. The SD5000 series is available in 16-lead dual inline surface mount or sidebrazed ceramic packages. Analog signal voltage ranges up to  $\pm 10$  V and frequencies up to 1 GHz can be controlled.

For surface-mount applications the [SST211](#) series is offered in the TO-253 (SOT-143) package. The [SD5400](#) series comes in the narrow body gull-wing SO-14 package.

## Applications

Fast switching speeds, low on-state resistance, high channel-to-channel isolation, low capacitance, and low charge injection make these DMOS devices especially well suited for a variety of applications.

A few of the many possible application areas for DMOS analog switches are as follows:

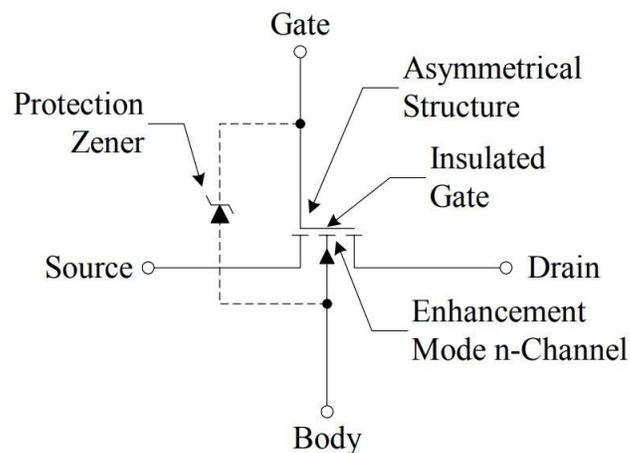
1. Video and RF switching (high speed, high offisolation, low crosstalk):
  - Multiple video distribution networks
  - Sampling scanners for RF systems
2. Audio routing (glitch- and noise-free):
  - High-speed switching
  - Audio switching systems using digitized remote control
3. Data acquisition (highspeed, low charge injection, low leakage):
  - High-speed sample-and-holds
  - Audio and communication A/D converters

## 4. Other:

- Digital switching
- PCM distribution networks
- UHF Amplifiers
- VHF Modulators and Double
- Balanced Mixers
- High-speed inverters/drivers
- Switched capacitor filters
- Choppers

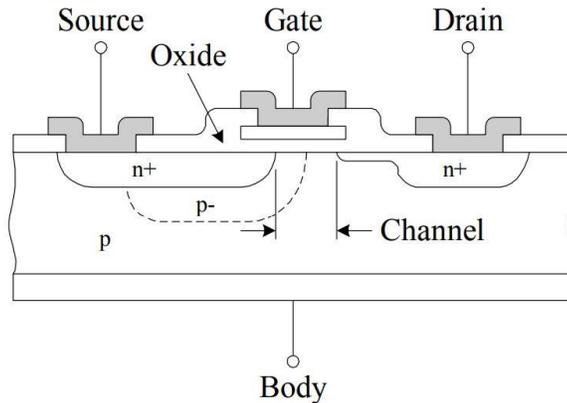
**Principle of Operation**

Figure 1 depicts an n-channel enhancement mode device with an insulated gate and asymmetrical structure. The gate protection Zener is shown with broken lines to indicate that, although it is present on the chip, it is not a main constituent of the fundamental switch structure.



**Figure 1. DMOS Electrical System**

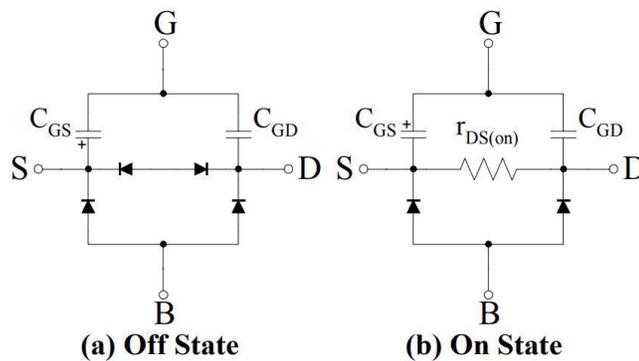
The DMOS field-effect transistor (FET) is normally off when the gate-to-source voltage ( $V_{GS}$ ) is 0 V. The lateral DMOS transistor, shown in cross-section in Figure 2, has three terminals (source, gate, and drain) on the top surface and one (the body or substrate) on the bottom. A Zener diode with a breakdown voltage of approximately 40 V is added to protect the gate against overvoltage and electrostatic discharges.



**Figure 2. Cross Sectional View of an Idealized DMOS Structure**

The double-diffusion process creates a thin self-aligning region of p-type material, isolating the source from the drain region. The very short channel length that results between the two junction depths produces extremely low source-to-drain and gate-to-drain capacitances at the same time that it provides good breakdown voltages.

When the gate potential is equal to or negative with respect to the source, the switch is off. In this state, the p-type material in the channel forms two back-to-back diodes and prevents channel conduction (Figure 3a). If a voltage is applied between the S and D regions, only a small junction leakage current will flow.



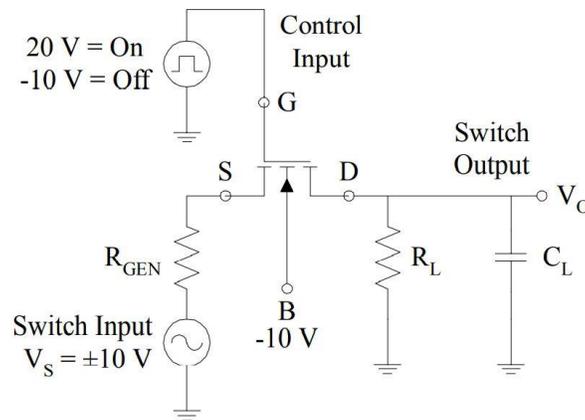
**Figure 3. Equivalent Circuits**

The silicon oxide insulation present between gate and source forms a small capacitor that accumulates charge.

If the gate-to-source potential ( $V_{GS}$ ) is made positive, the capacitive effect attracts electrons to the channel area immediately adjacent to gate oxide. As  $V_{GS}$  increases, the electron density in the channel will exceed the hole density, and the channel will become an n-type region. As the channel conductivity is enhanced, the n-n-n structure becomes a simple silicon resistor through which current can easily flow in either direction.

Figure 4 shows typical biasing for  $\pm 10$  V analog signal processing. Note that the drain is recommended for the output. Since  $CGD < CGS$  this causes less charge injection noise on the load.

As can be seen from Figures 3a and 3b, the body-source and body-drain pn junctions should be kept reverse biased at all times—otherwise, signal clipping and even device damage may occur if unlimited currents are allowed to flow. Body biasing is conveniently set, in most cases, by connecting the substrate to  $V_-$ .



**Figure 4. Normal Switch Configuration for a  $\pm 10$  V Analog Switch**

### Main Switch Characteristics

#### $r_{DS(on)}$

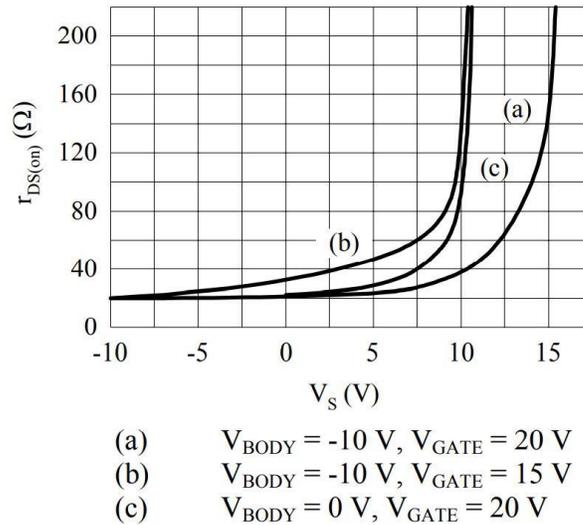
Channel on-resistance is controlled by the electric field present across and along the channel. Channel resistance is mainly determined by the gate-to-source voltage difference. When  $V_{GS}$  exceeds the threshold voltage ( $V_{GS(th)}$ ), the FET starts to turn on.

Numerous applications call for switching a point to ground. In these cases the source and substrate are connected to ground and a gate voltage of 3 to 4 V is sufficient to ensure switching action.

With a  $V_{GS}$  in excess of +5 V, a low resistance path exists between the source and the drain.

The circuit shown in Figure 4 exhibits the  $r_{DS(on)}$  vs. analog signal voltage relationship shown in Figure 5.

When the analog signal excursion is large (for example  $\pm 10$  V) the channel on-resistance changes as a function of signal level. To achieve minimum distortion, this channel on-resistance modulation should be kept in mind, and the amount of resistance in series with the switch should be properly sized. For instance, if the switch resistance varies between  $20 \Omega$  and  $30 \Omega$  over the signal range and the switch is in series with a  $200 \Omega$  load, the result will be a total  $\Delta R = 4.5\%$ . Whereas, if the load is  $100 \text{ k}\Omega$ ,  $\Delta R$  will only be  $0.01\%$ .



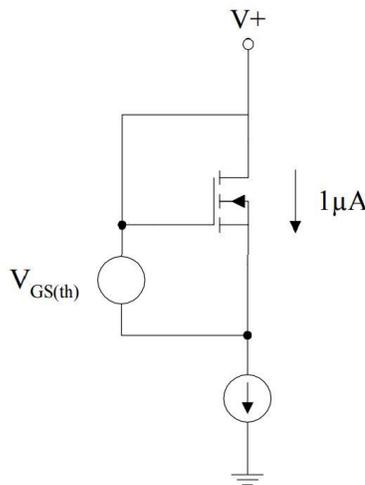
**Figure 5. On Resistance Characteristics**

Figure 4 shows typical biasing for  $\pm 10\text{ V}$  analog signal processing. Note that the drain is recommended for the output. Since  $CGD < CGS$  this causes less charge injection noise on the load. As can be seen from Figures 3a and 3b, the body-source and body-drain pn junctions should be kept reverse biased at all times-otherwise, signal clipping and even device damage may occur if unlimited currents are allowed to flow. Body biasing is conveniently set, in most cases, by connecting the substrate to  $V_-$ .

**Threshold Voltage**

The threshold voltage ( $V_{GS(th)}$ ) is a parameter used to describe how much voltage is needed to initiate channel conduction. Figure 6 shows the applicable test configuration. In this circuit, it is worth noting, for instance, that if the device has a  $V_{GS(th)} = 0.5\text{ V}$ , when  $V_+ = 0.5\text{ V}$ , the channel resistance will be:

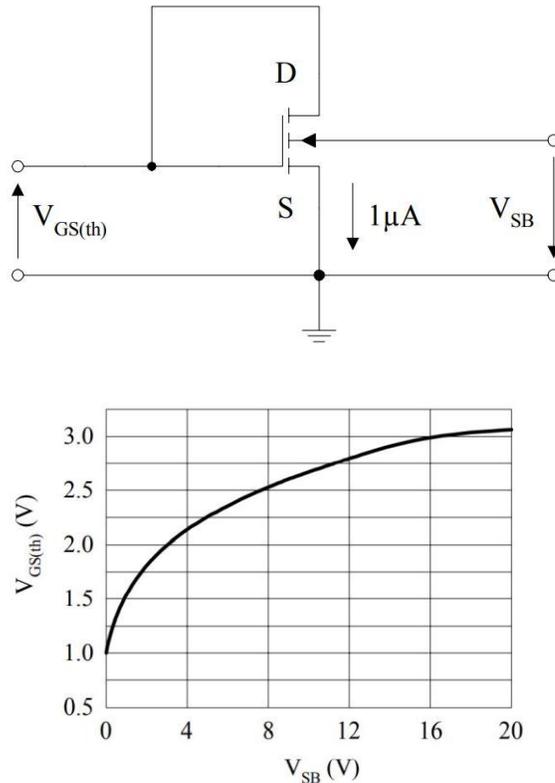
$$R_{CHANNEL} = \frac{0.5\text{V}}{1\mu\text{A}} = 500\text{k}\Omega$$



**Figure 6. Threshold Voltage Test Configuration**

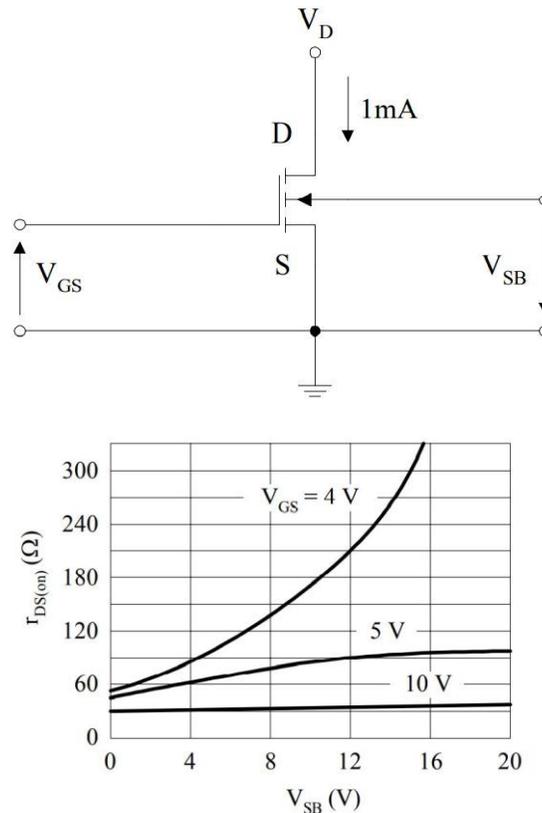
### Body Effect

For a MOSFET with a uniformly doped substrate, the threshold voltage is proportional to the square root of the applied source-to-body voltage. The [SD5000](#) family has a non-uniform substrate, and the  $V_{GS(th)}$  behaves somewhat differently. Figure 7 shows the typical  $V_{GS(th)}$  variation as a function of the source-to-body voltage  $V_{SB}$ .



**Figure 7. Threshold vs Source to Body Voltage**

As the body voltage increases in the negative direction, the threshold goes up. Consequently, if  $V_{GS}$  is small, the on-resistance of the channel can be very high. Figure 8 shows the effects of  $V_{SB}$  and  $V_{GS}$  on  $r_{DS(on)}$ . Therefore, to maintain a low on-resistance it is preferable to bias the body to a voltage close to the negative peaks of  $V_S$  and use a gate voltage as high as possible.



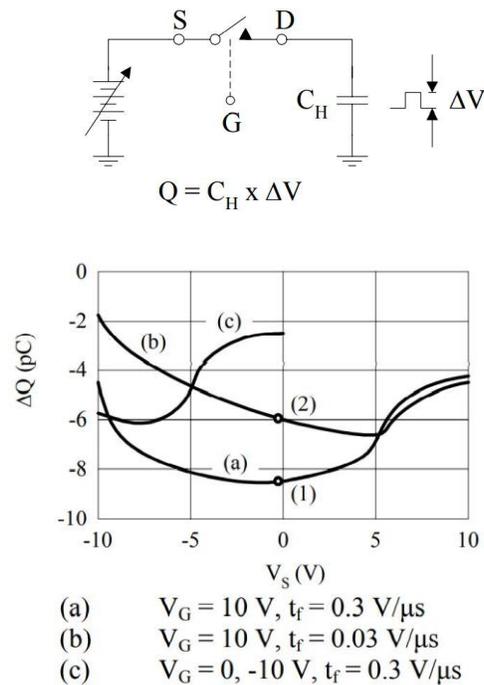
**Figure 8. On Resistance vs Source to Body and Gate to Source Voltages**

### Charge Injection

Charge injection describes that phenomenon by which a voltage excursion at the gate produces an injection of electric charges via the gate-to-drain and the gate-to-source capacitances into the analog signal path. Another popular name for this phenomenon is “switching spikes.”

Since these DMOS devices are asymmetrical<sup>1</sup>, the charge injected into the S and D terminals is different. Typical parasitic capacitances are on the order of 0.2 pF for  $C_{DG}$  and 1.5 pF for  $C_{SG}$ .

Another factor that influences the amount of charge injected is the amplitude of the gate voltage excursion. This is a directly proportional relationship: the larger the excursion, the larger the injected charge. This can be seen by comparing curves (a) and (c) in Figure 9. One other variable to consider is the rate of gate-voltage change. Large amounts of charge are injected when faster rise and fall times are present at the gate. This is shown by curves (a) and (b) in Figure 9.



**Figure 9. SD5000 Charge Injection**

Switching spikes occur at switch turn-on as well as turn-off time. When the switch turns on, the charge injection effect is minimized by the usually low signal-source impedance. This low impedance tends to produce a rapid decay of the extra charge introduced in the channel. At turnoff, however, the injected charge might become stored in a sampling capacitor and create offsets and errors. These errors will have a magnitude that is inversely proportional to the magnitude of the holding capacitance.

Figure 9 illustrates several typical charge injection characteristics. Figure 10 shows some of the corresponding waveforms. The DMOS FETs, because of their inherent low parasitic capacitances, produce very low charge injection when compared to other analog switches (PMOS, CMOS, JFET, BIFET etc.). Still, when the offsets created are unacceptable, charge injection compensation techniques exist that eliminate or minimize them. The solution basically consists of injecting another charge of equal amplitude but opposite polarity at the time when the switch turns off.

### Off-Isolation and Crosstalk

The dc on-state resistance is typically  $30 \Omega$  and the off-state resistance is typically  $1010 \Omega$ , which results in an off-state to on-state resistance ratio in excess of 108. However, for video and VHF switching applications, the upper usable frequency limit is determined by how much of the incoming signal is coupled through the parasitic capacitances and appears at the switch output when ideally no signal should appear there in the off state.

<sup>1</sup>The chip geometry is such that non-identical behavior occurs when the source and drain terminals are reversed in a circuit.

Off-Isolation is defined by the formula:

$$\text{Off - Isolation (dB)} = 20 \log \frac{V_{\text{out}}}{V_{\text{in}}}$$

When several analog switches are simultaneously being used to control high frequency signals, crosstalk becomes a very important characteristic. For video applications, the stray signal coupled via parasitic capacitances to the signal of an adjacent channel can form ghosts and signal interference. To help obtain high degrees of isolation, it becomes necessary to exercise careful circuit layout, reducing parasitic capacitive and inductive couplings, and to use proper shielding and bypassing techniques. Figure 11 shows the excellent off-isolation and crosstalk performance typical of this family of DMOS analog switches.

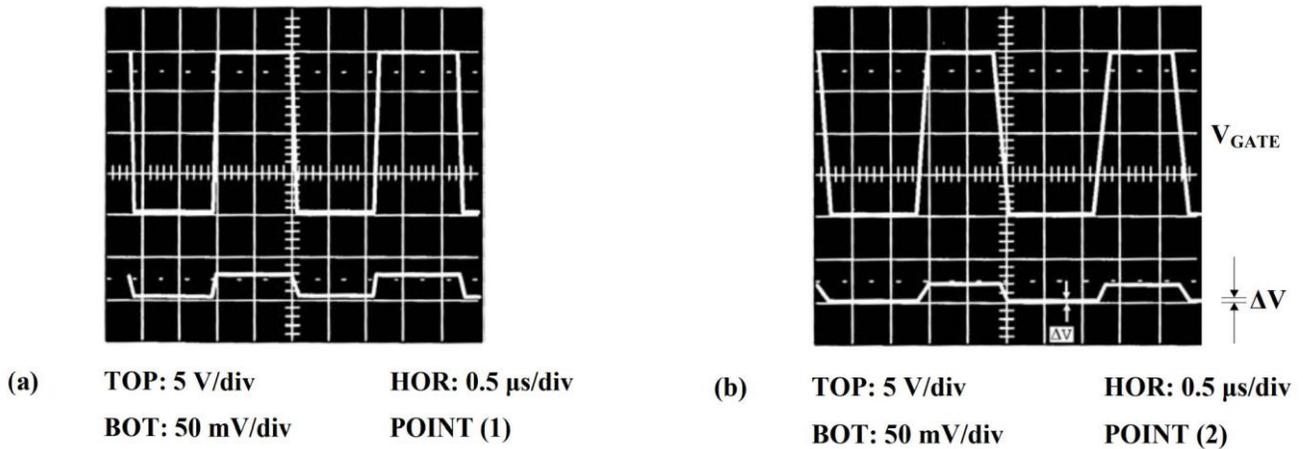
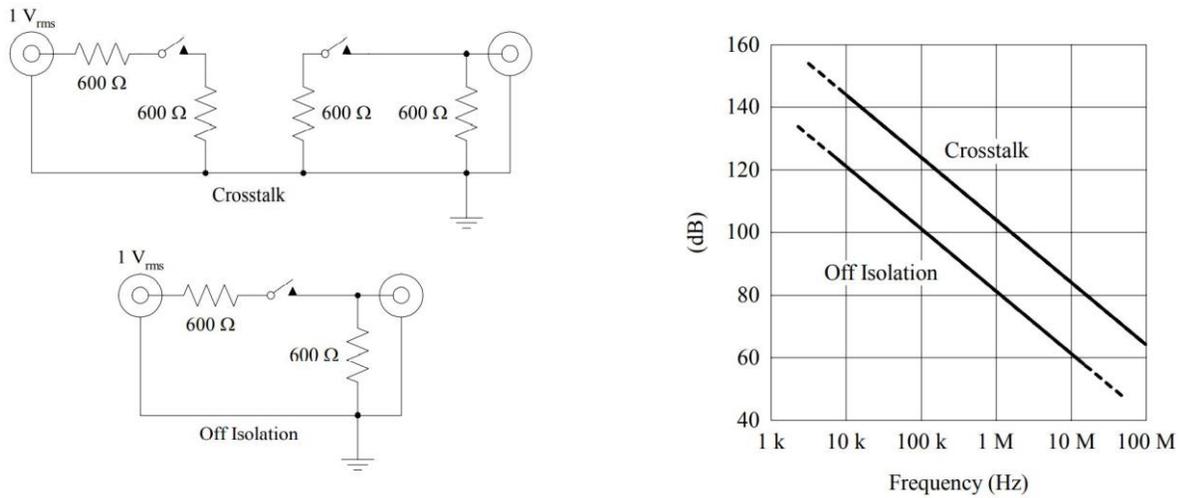


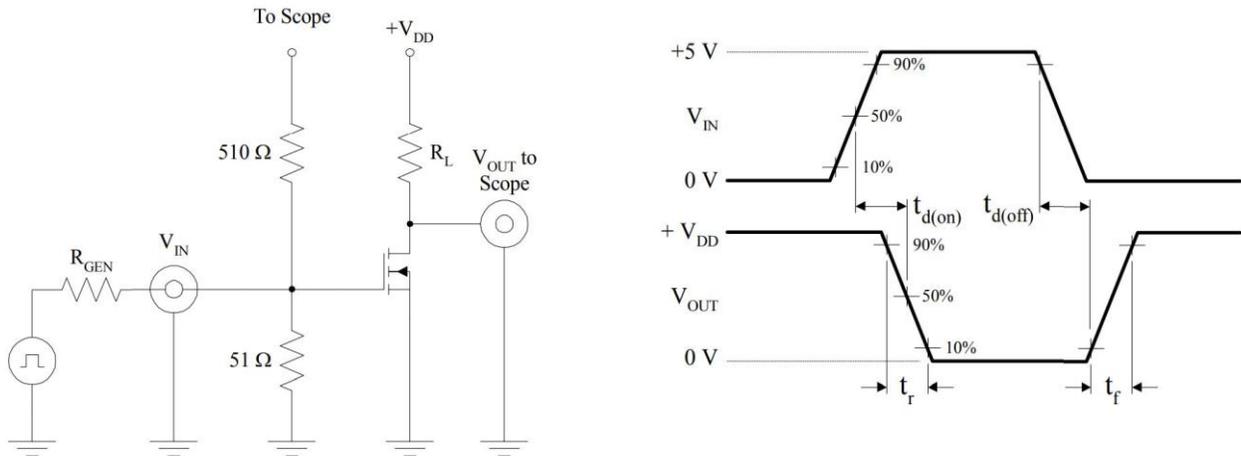
Figure 10. Waveforms for Points (1) and (2) of Figure 9

**Insertion Loss**

At low frequencies, the attenuation caused by the switch is a function of its on-resistance and the load impedance. They form a simple series voltage divider network. As an example, for a 600 Ω load impedance the insertion loss for voice signals (1 V<sub>rms</sub> at 3 kHz) is less than 0.3 dB. Thus, the [SD5000](#) series make good audio crosspoint switches.



**Figure 11. SD5000 Crosstalk and Off Isolation vs Frequency**



**Figure 12. Switching Test Circuit**

## Speed

Because the on-resistance and input capacitance are low, the DMOS switches are capable of subnanosecond switching speeds. At these speeds the external circuit rather than the FET itself is often responsible for the rise and fall times that can be obtained. Let's consider the switching test circuit of Figure 12. At turn-on, the fall time observed at the drain is a function of  $R_G$  and of the input pulse amplitude and rise time. The sooner CGS reaches  $V_{GS(th)}$ , the sooner turn-on will occur, and the lower the  $r_{DS(on)}$  reached, the faster CDS will be discharged.

The turn-off time (or the rise time of VD) is not as much limited by the velocity at which CGS can be discharged by the gate control pulse, as it is by the time it takes to charge up CDS and CDG via the load resistor  $R_L$ . Table 1 shows typical performances obtained. It is important to realize that stray capacitance and parasitic inductances, as well as scope probe capacitance, can seriously affect the rise and fall times (switching speed).

$V_{DD}$ (V)	$R_L$ ( $\Omega$ )	$t_{d(on)}$ (ns)	$t_r$ (ns)	<sup>2</sup> $t_{OFF}$ (ns)
5	330	0.6	0.8	4
5	680	0.6	0.7	8
10	680	0.7	0.8	8
15	1k	0.9	1.0	12

<sup>2</sup> $t_{OFF}$  is dependant on  $R_L$  and does not depend on the device characteristics.

**Table 1. Typical Switching Times**

## Drivers

The switch driver's function is to translate logic control levels (either TTL, CMOS, or ECL) into the appropriate voltages needed at the gate so that the switch can be turned on or off. The [SD5000](#) can be operated as an inverter capable of driving up to 20 V. This high-voltage rating, together with its high speed, make it an excellent driver for the other members of the family. Figure 13 shows several driver circuits. Since switching times depend on the CGS charge/discharge times, it is important to note that the driver's current source/sink capability plays a very important role in the process.

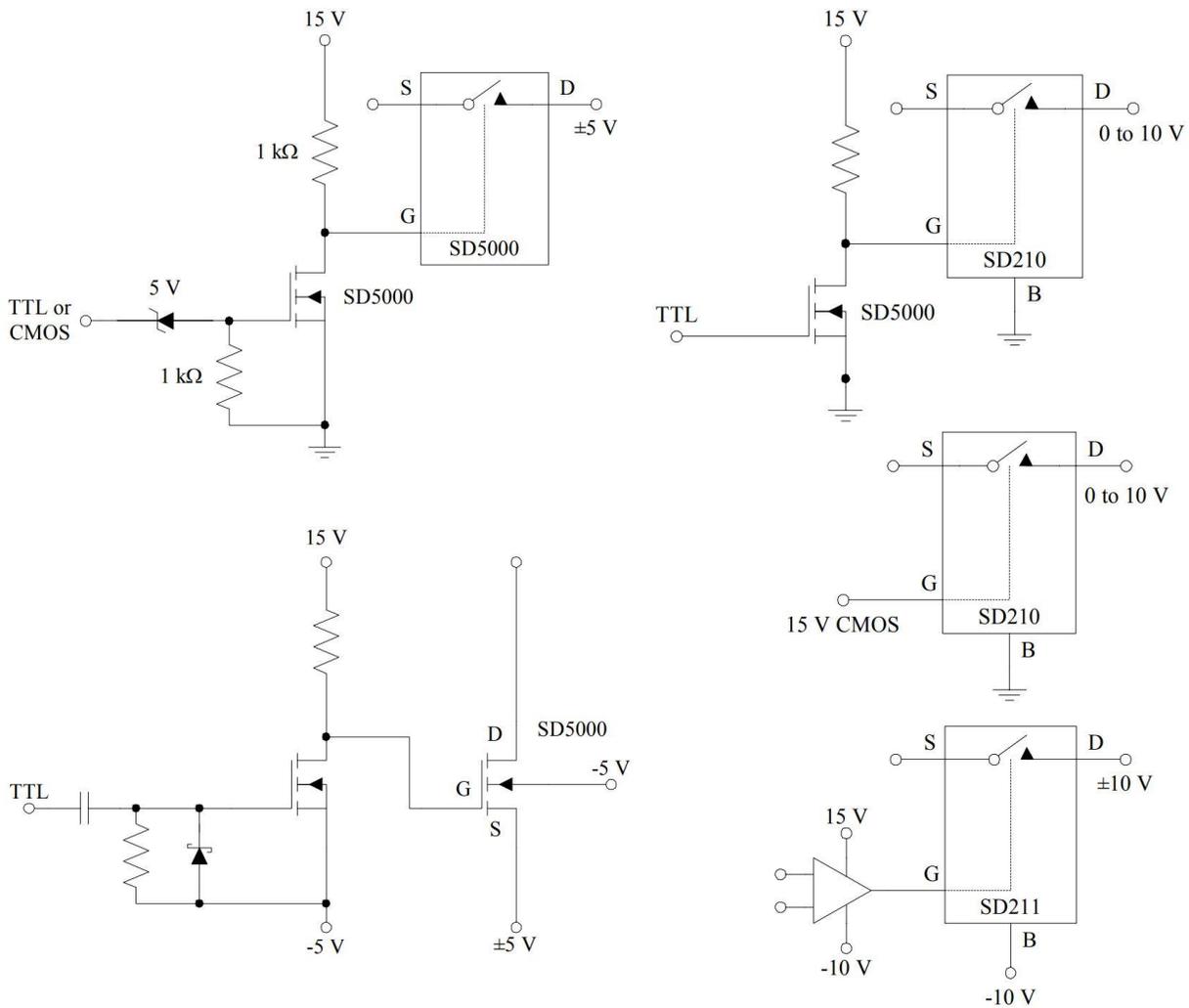
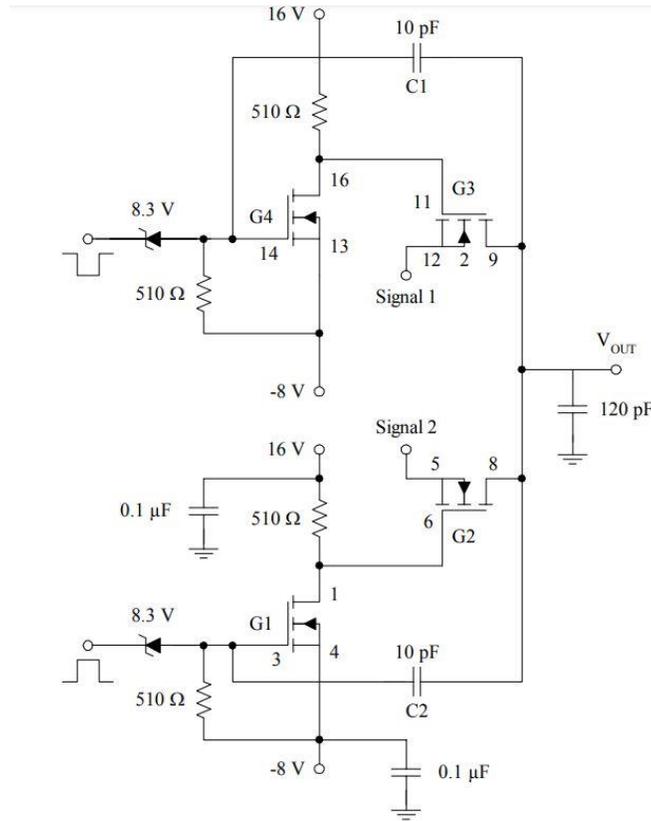


Figure 13. Various DMOS Drivers

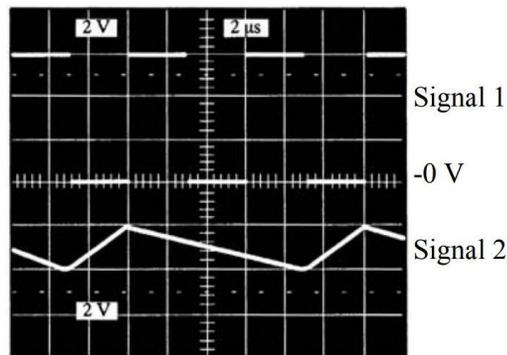
### High-Speed Multiplexer

In a typical application, the circuit of Figure 14 is used to multiplex and sample-and-hold two analog signals at a 5-MHz rate. Two of the switches in an [SD5000](#) are used as level shifter/drivers to provide the gate drive of the single-pole-double-throw arrangement formed by switches 3 and 4. Capacitors C1 and C2 provide charge injection compensation.



**Figure 14. 5-MHz Multiplexer and Sample and Hold Circuit**

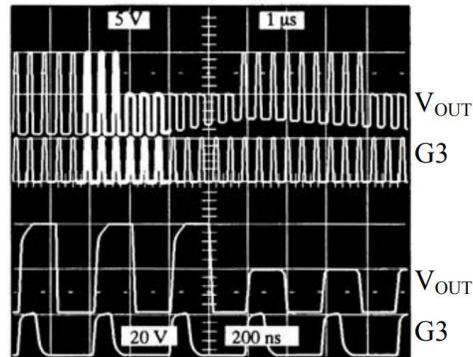
Signal 1 is a 6-V, 156-kHz square wave. Signal 2 is a 2-V<sub>pp</sub>, 78-kHz alternating waveform with a dc offset of -3.4 V (Figure 15).



**Figure 15. The Two Analog Signals to Be Sampled**

Figure 16 illustrates the resulting composite waveform present at the holding capacitor along with the gate 3 control signal.

As can be seen, the switching times are about 15 ns, the acquisition time is 80 ns, and the holding time is about 90 ns. The total sample-and-hold cycle takes 200 ns. Even though not maximized, this speed is faster than what any other presently available (50 ns) analog switch products can achieve.

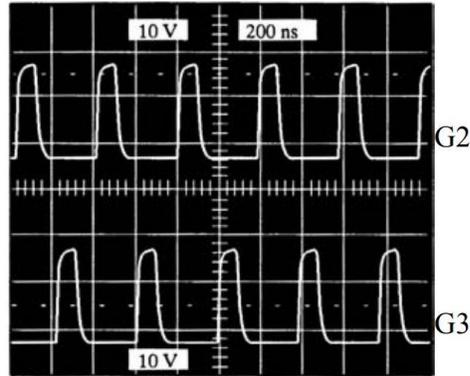


**Figure 16. Composite Sample and Hold Output and the Gate 3 Control Signal**

FREQ (Hz)	SIG LVL (dBm)	INS LOSS (dB)	OFF ISOL (dB)	XTALK (dB)
100 K	0	1.8	80	113
1 M	0	1.8	70	92
5 M	0	1.9	69	69
10 M	0	2.0	61	65
10 M	6	2.0	61	66
10 M	12	2.0	61	68

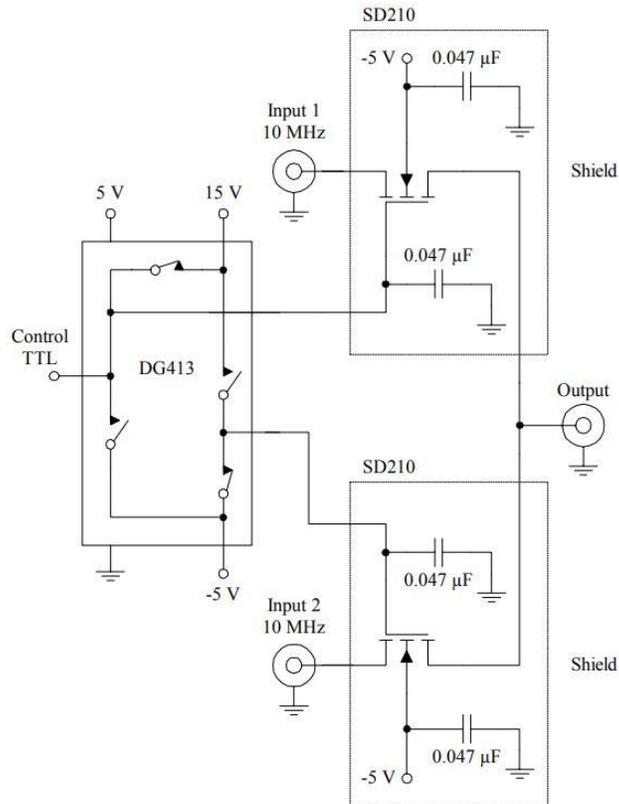
**Table 2. SPDT Switching Performance**

The timing and amplitude of gate 2 and gate 3 control-signals can be examined in Figure 17.



**Figure 17. Gate Control Signals for the SPDT Switch Configuration**

Figure 18 shows a single-pole single-throw configuration used to select one of two AM modulated 10-MHz signals. Figure 19 illustrates the two waveforms available at the output. Table 2 contains typical values of crosstalk and off-isolation attainable with this configuration.



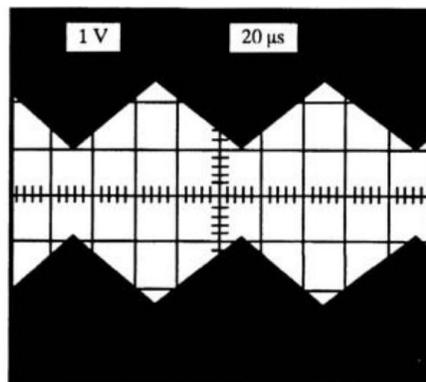
**Figure 18. High Frequency SPDT Switch**

### A High-Speed S/H Circuit

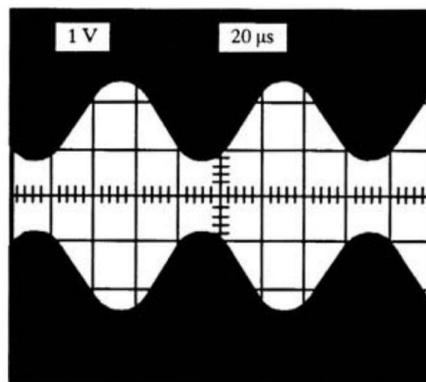
Figure 20 shows a fast unity gain input buffer (Si581) driving an [SD5000](#) Switch. One half of the [SD5000](#) is configured as dummy switches for charge injection compensation. A JFET output buffer minimizes droop. Transistors Q1 through Q4 level shift the ECL control input signals into a voltage (referenced to the analog signal voltage) used to drive the DMOS FETs.

### DAC Deglitcher

A Very small charge injection makes DMOS FETs excellent DAC deglitcher switches. Figure 21 illustrates a typical circuit configuration.



Channel 1 On



Channel 2 On

**Figure 19. Two 10-MHZ AM Modulated Outputs for the SPDT Switch of Figure 18**

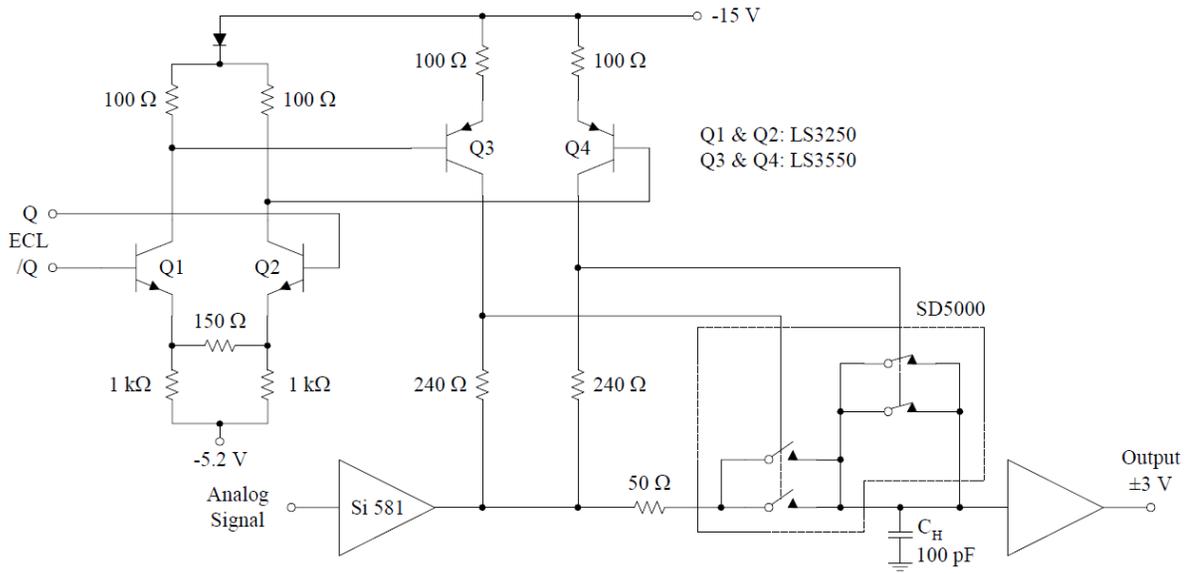


Figure 20. Fast S/H Circuit Achieves Minimum Step Errors

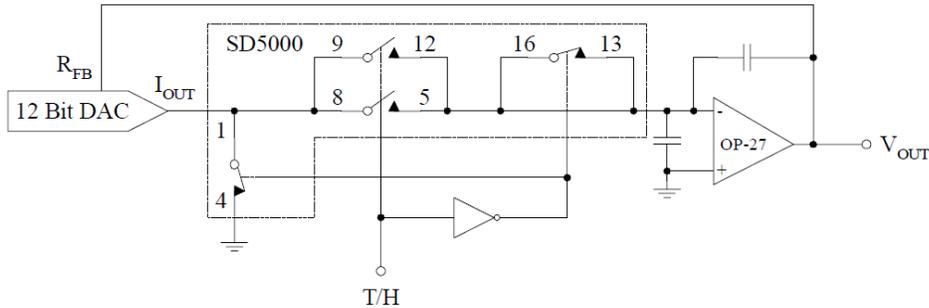


Figure 21. DAC Deglitcher Using DMOS Switches

Part Number	Package	Type	Zener Protection	$r_{DS(on)}$ ( $\Omega$ )	$V_{(BR)DS}$ Min (V)
SD210DE	TO-72	Single	None	45	30
SD214DE	TO-72	Single	None	45	20
SD/SST211	TO-72/SOT-143	Single	Yes	45/50	30
SD/SST213	TO-72/SOT-143	Single	Yes	45/50	10
SD/SST215	TO-72/SOT-143	Single	Yes	45/50	20
SD5000N	PDIP	Quad	Yes	70	20
SD5001N	PDIP	Quad	Yes	70	10
SD5000I	CDIP	Quad	Yes	70	20
SD5400CY	SOIC	Quad	Yes	75	20
SD5401CY	SOIC	Quad	Yes	75	10
SD/SST823 <sup>3</sup>	TO-72/SOT-143	Single	Yes	5	15
SD/SST824 <sup>3</sup>	TO-72/SOT-143	Single	Yes	5	20

<sup>3</sup> Future devices available Q1 2003

Table 3. DMOS Device Part Numbers and Packages