

MOSFET

OptiMOS™ 5 Power-Transistor, 60 V

Features

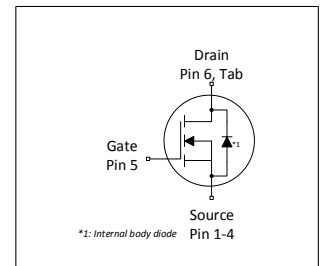
- Optimized for low voltage motor drives application
- Optimized for battery powered applications
- Enables automated optical solder inspection
- 100% avalanche tested
- N-channel
- 175°C rated
- Pb-free lead plating; RoHS compliant

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	1.5	m Ω
I_D	242	A
Q_{oss}	81	nC
$Q_G(0V...10V)$	71	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
IST015N06NM5	sTOLL	015N06N5	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	242 171 36	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	968	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	380	mJ	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	167 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}^2)$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.45	0.9	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	40	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}$, $I_D=95\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.5 10	1.0 100	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.3 1.9	1.5 2.4	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=25\text{ A}$
Gate resistance	R_G	-	1.6	-	Ω	-
Transconductance ¹⁾	g_{fs}	70	140	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=50\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	5200	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	1200	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	48	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	22.48	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	63.6	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	44.6	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	17.7	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	23	-	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	14.6	-	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	12.9	-	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	21	-	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	71	89	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.3	-	V	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	63	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	81	-	nC	$V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	121	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	968	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.84	1.2	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	65.4	-	ns	$V_R=30\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	101.1	-	nC	$V_R=30\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

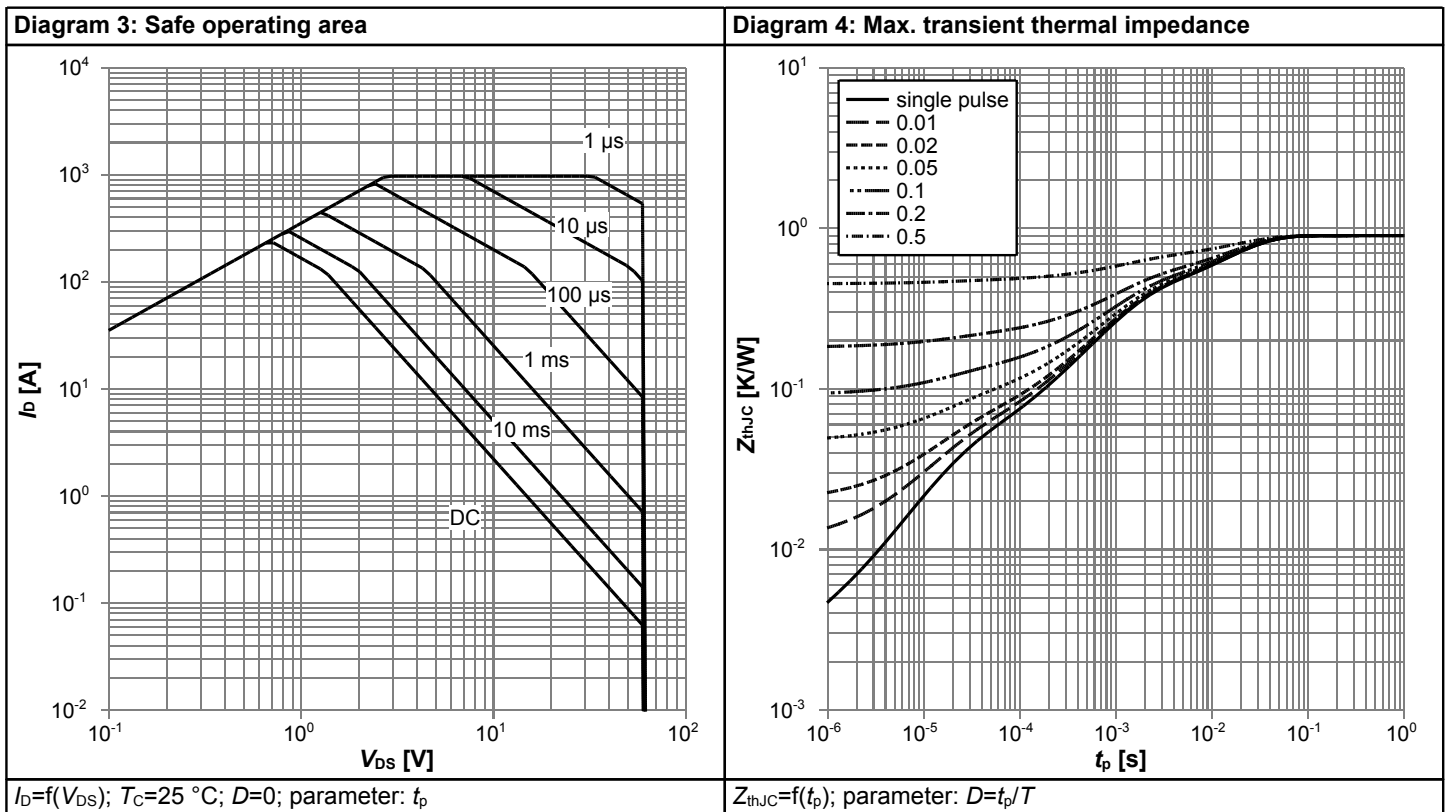
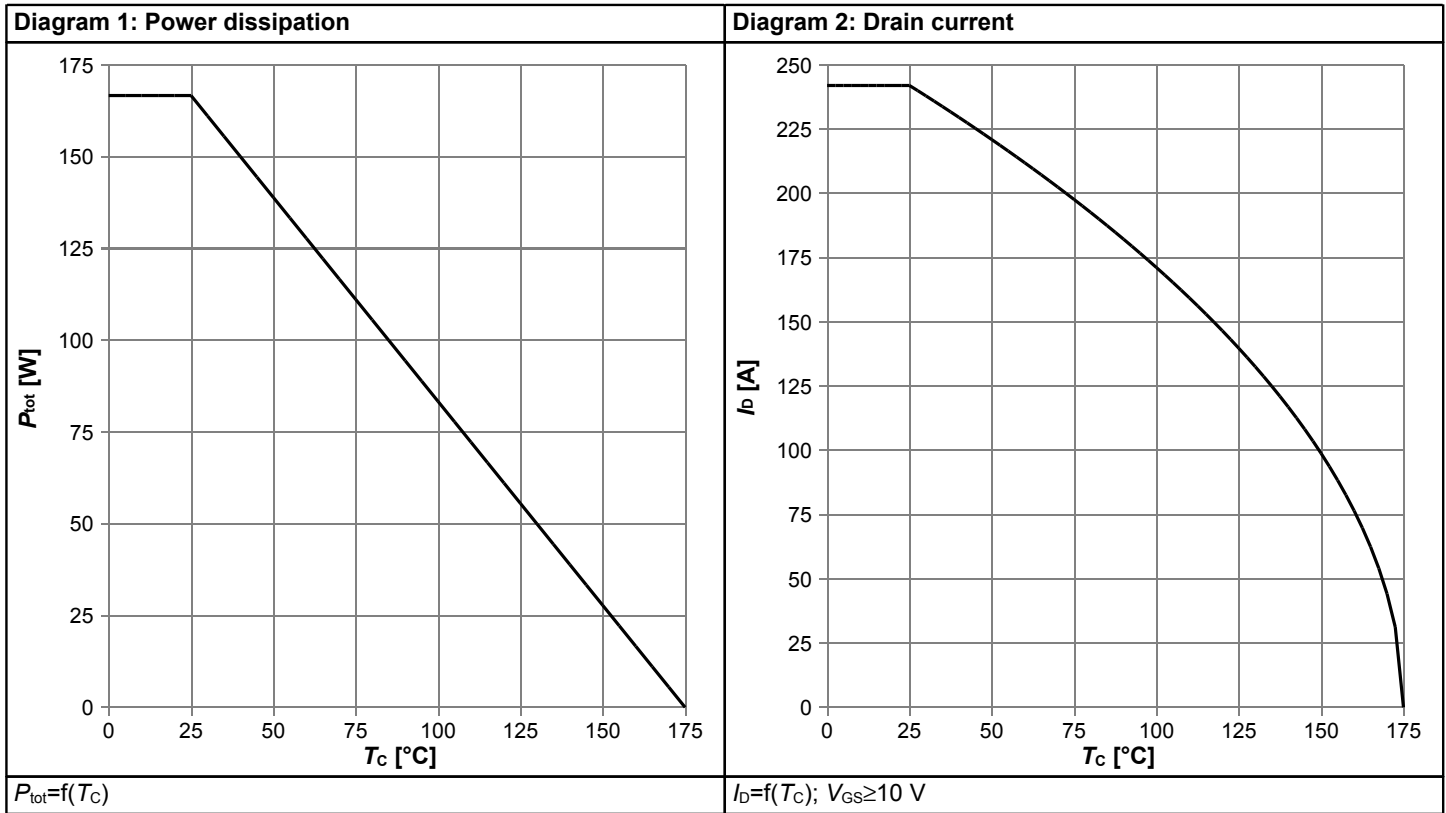
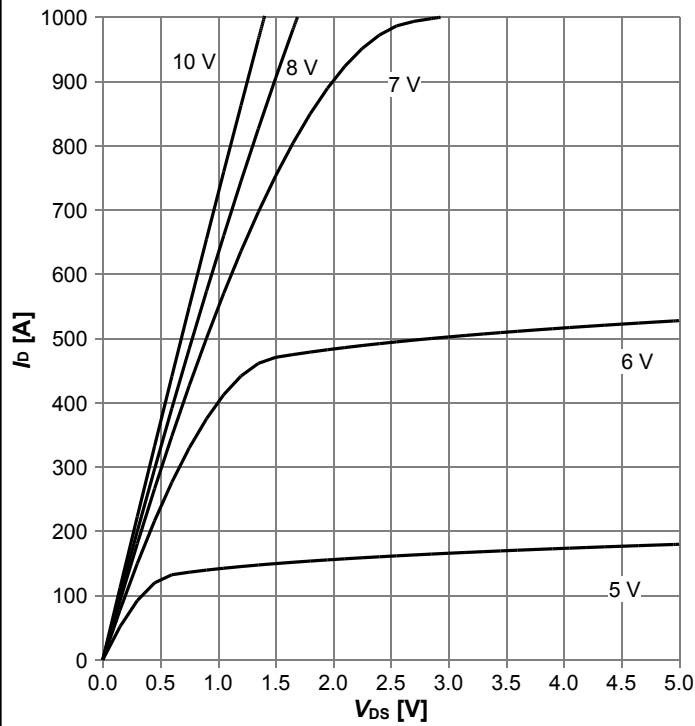
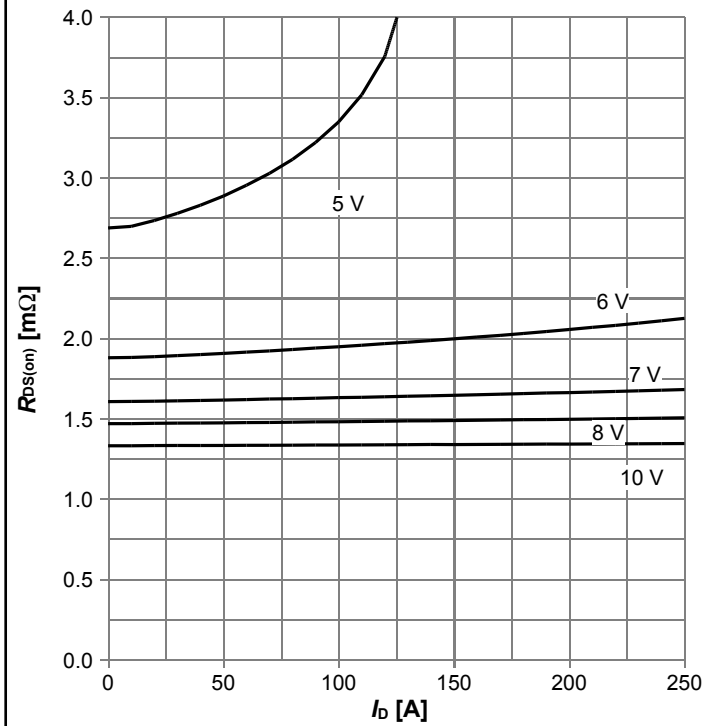


Diagram 5: Typ. output characteristics



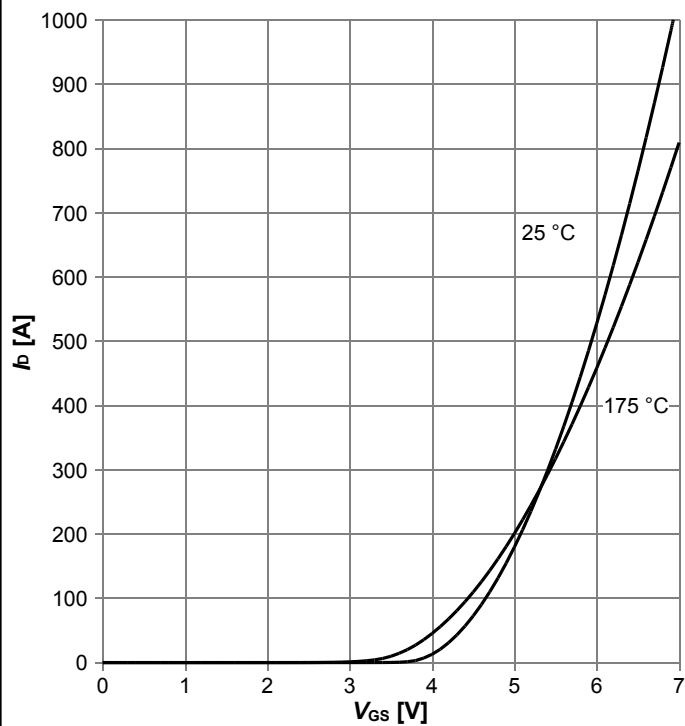
$I_D=f(V_{DS})$, $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



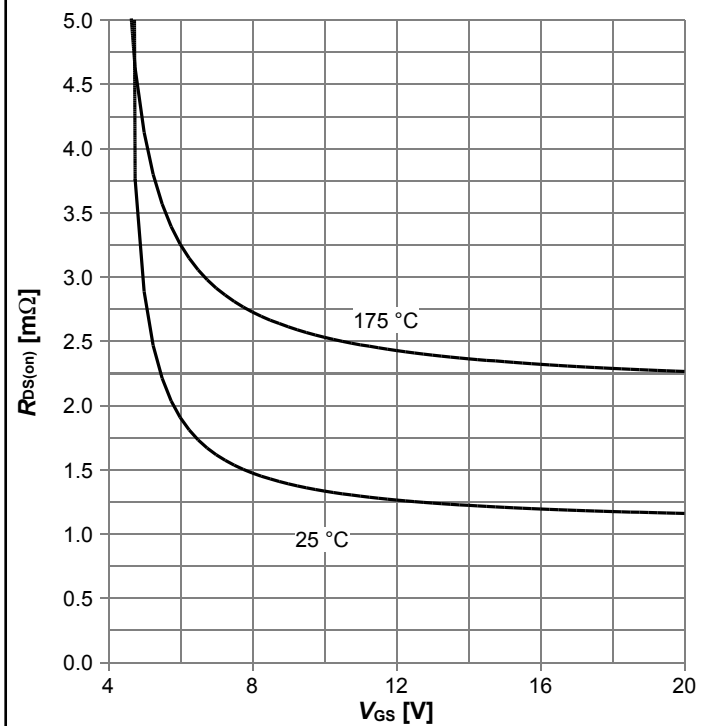
$R_{DS(on)}=f(I_D)$, $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



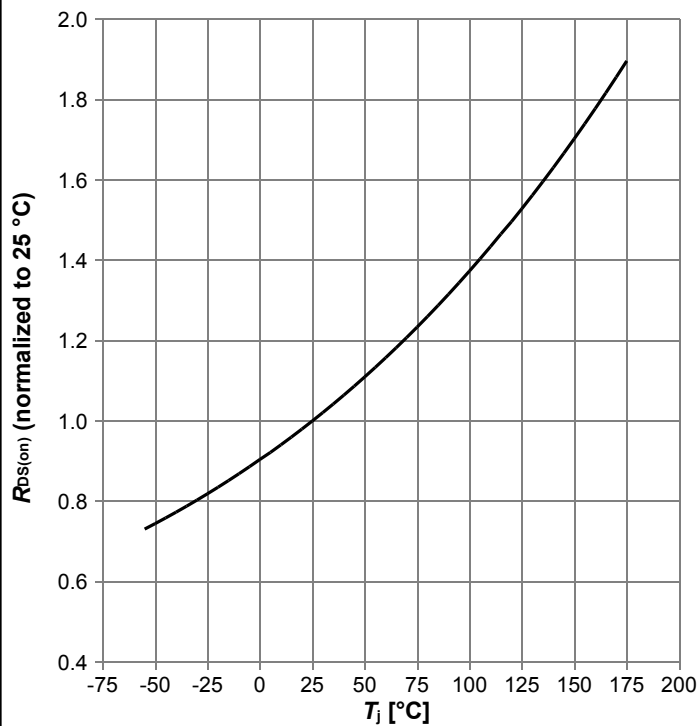
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



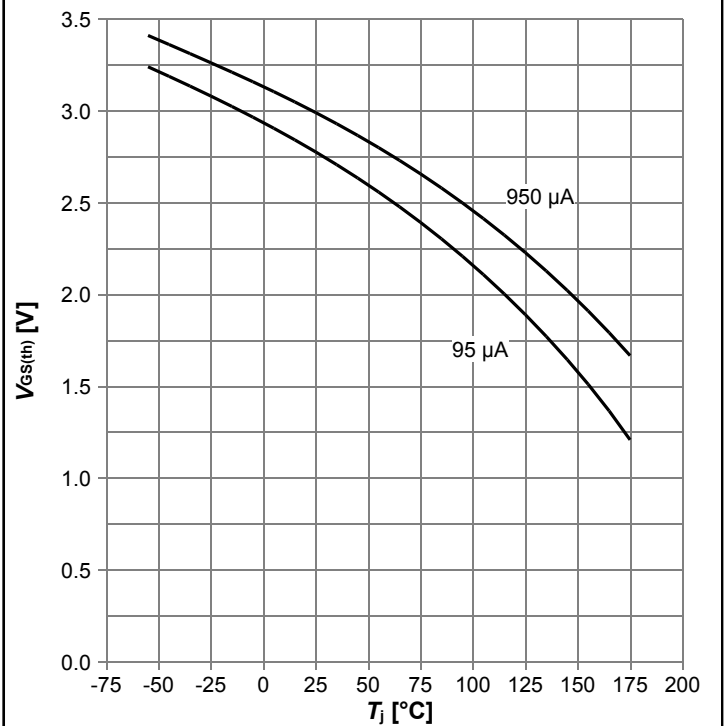
$R_{DS(on)}=f(V_{GS})$, $I_D=50\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



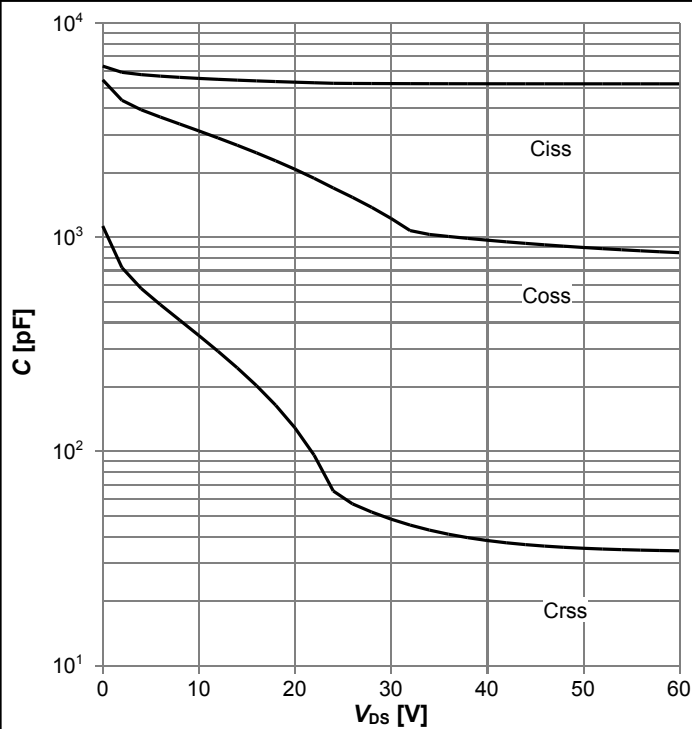
$R_{DS(on)}=f(T_j)$, $I_D=50$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



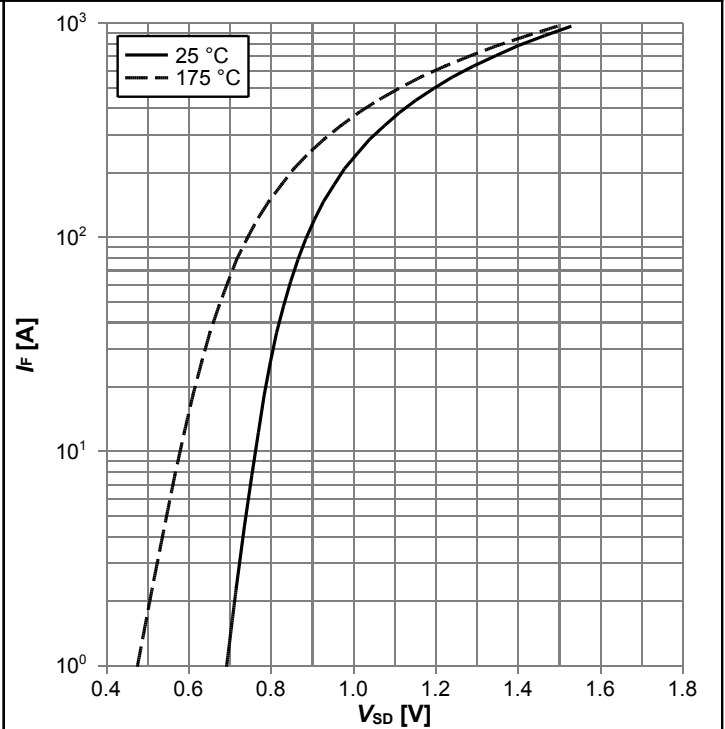
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



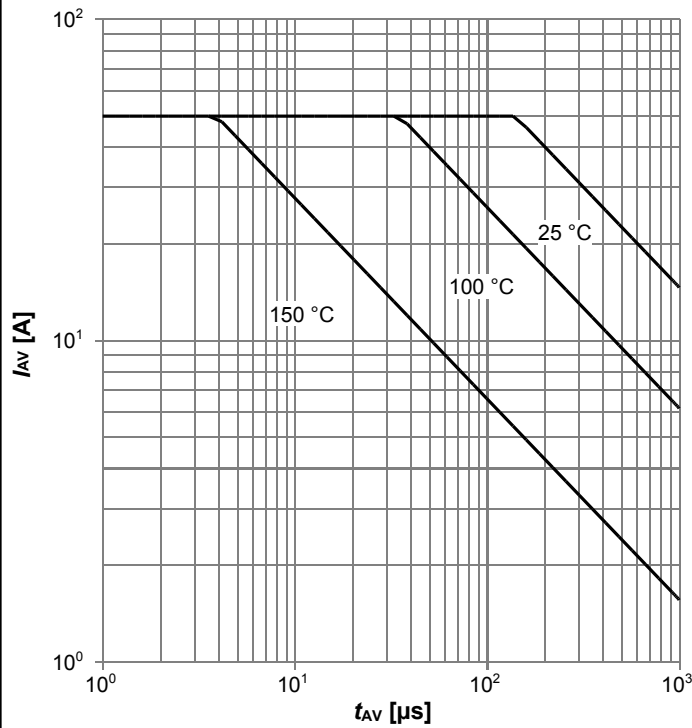
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



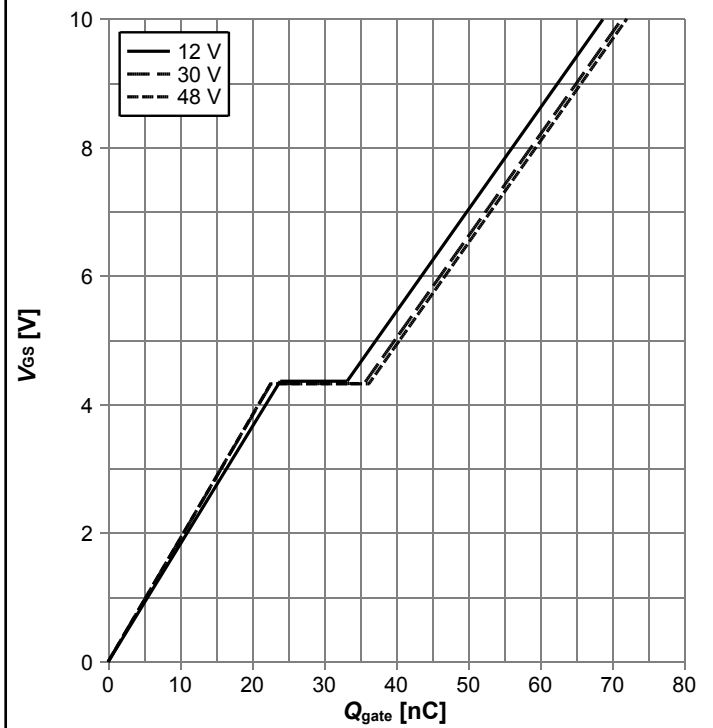
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



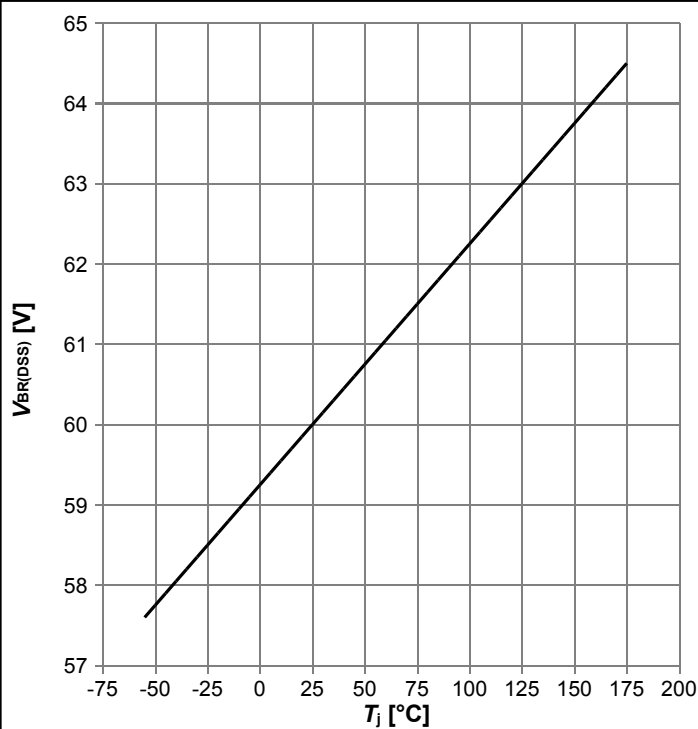
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate}), I_D=50 \text{ A pulsed}, T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

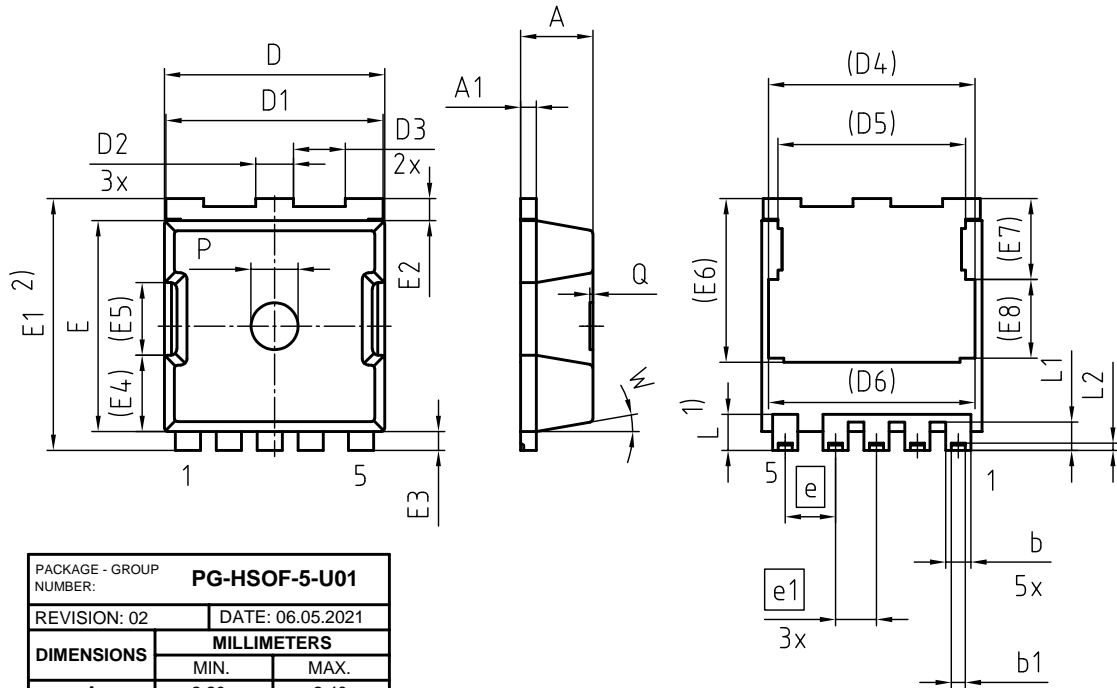


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER: PG-HSOF-5-U01		
REVISION: 02		DATE: 06.05.2021
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
A1	0.40	0.60
b	0.70	0.90
b1	0.42	0.50
D	6.80	7.20
D1	6.80	7.00
D2	1.10	1.30
D3	1.55	1.75
D4	6.56	
D5	5.96	
D6	5.60	
E	6.50	6.90
E1	7.80	8.20
E2	0.60	0.80
E3	0.50	0.70
E4	2.43	
E5	2.30	
E6	5.20	
E7	2.57	
E8	2.50	
e	1.60	
e1	1.30	
L	1.05	1.25
L1	0.80	1.00
L2	0.13	0.33
P	1.40	1.60
Q	0.00	0.10
W	8.50°	11.50°

1) LEAD LENGTH UP TO ANTI FLASH PROFILE, MOLD FLASHES EXCLUDED.

2) EXCLUDING BURR

Figure 1 Outline sTOLL, dimensions in mm

Revision History

IST015N06NM5

Revision: 2022-04-28, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-04-28	Release of final version

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