MOSFET – N-Channel, QFET

600 V, 7.4 A, 1.0 Ω

FQB7N60, FQI7N60

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
600 V	1.0 Ω @ 10 V	7.4 A

Description

This N−Channel enhancement mode power MOSFET is produced using **onsemi**'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 7.4 A, 600 V, $R_{DS(on)}$ = 1.0 Ω (Max.) @ V_{GS} = 10 V, I_D = 3.7 A
- Low Gate Charge (Typ. 29 nC)
- Low Crss (Typ. 16 pF)
- 100% Avalanche Tested
- This Device is Pb−Free, Halide Free and is RoHS Compliant

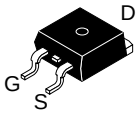
MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter	FQB7N60TM FQI7N60TU	Unit
V_{DSS}	Drain−Source Voltage	600	V
I_D	Drain Current − Continuous (T_C = 25°C)	7.4	A
	− Continuous (T_C = 100°C)	4.7	A
I_{DM}	Drain Current − Pulsed (Note 1)	29.6	A
V_{GSS}	Gate−Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	580	mJ
I_{AR}	Avalanche Current (Note 1)	7.4	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	14.2	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *	3.13	W
	Power Dissipation (T_C = 25°C)	142	W
	− Derate above 25°C	1.14	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	°C

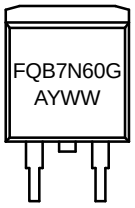
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. L = 19.5 mH, I_{AS} = 7.4 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 7.4 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

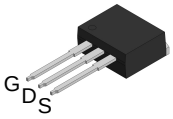
MARKING DIAGRAM



D²PAK−3 (TO−263, 3−LEAD) CASE 418AJ

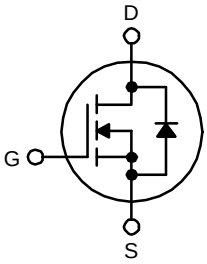


FQB7N60 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package



I2PAK (TO−262 3 LD) CASE 418AV

&Z = Assembly Plant Code
&3 = 3−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
FQI7N60 = Device Code



N−Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	FQB7N60TM FQI7N60TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.88	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2−oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in^2 Pad of 2−oz Copper), Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	600	−	−	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	−	0.67	−	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	−	−	10	μA
		V_{DS} = 480 V, T_C = 125°C	−	−	100	μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	−	−	100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0 V	−	−	−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	−	5.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 3.7 A	−	0.8	1.0	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 3.7 A	−	6.4	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	−	1100	1430	pF
C_{oss}	Output Capacitance		−	135	175	pF
C_{rss}	Reverse Transfer Capacitance		−	16	21	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 300 V, I_D = 7.4 A, R_G = 25 Ω (Note 4)	−	30	70	ns
t_r	Turn−On Rise Time		−	80	170	ns
$t_{d(off)}$	Turn−Off Delay Time		−	65	140	ns
t_f	Turn−Off Fall Time		−	60	130	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 7.4 A, V_{GS} = 10 V (Note 4)	−	29	38	nC
Q_{gs}	Gate−Source Charge		−	7	−	nC
Q_{gd}	Gate−Drain Charge		−	14.5	−	nC
DRAIN−SOURCE CHARACTERISTICS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		−	−	7.4	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		−	−	29.6	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.4 A	−	−	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 7.4 A, dI_F / dt = 100 A/μs	−	320	−	ns
Q_{rr}	Reverse Recovery Charge		−	2.4	−	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

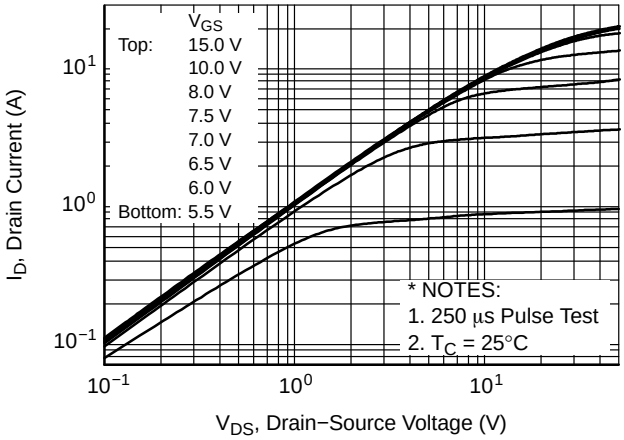


Figure 1. On−Region Characteristics

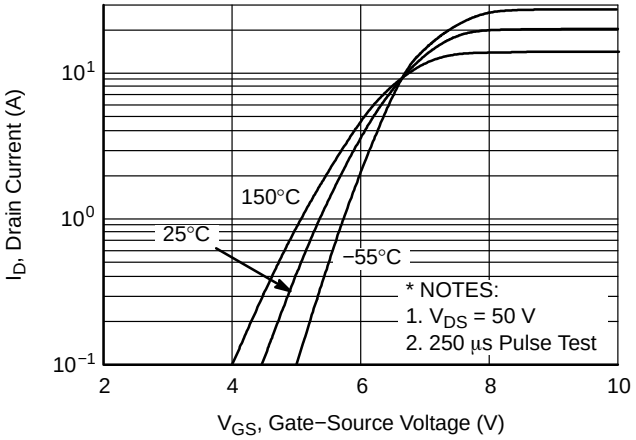


Figure 2. Transfer Characteristics

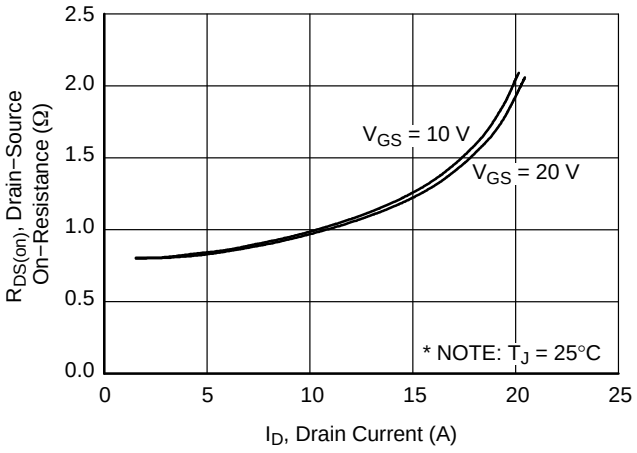


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

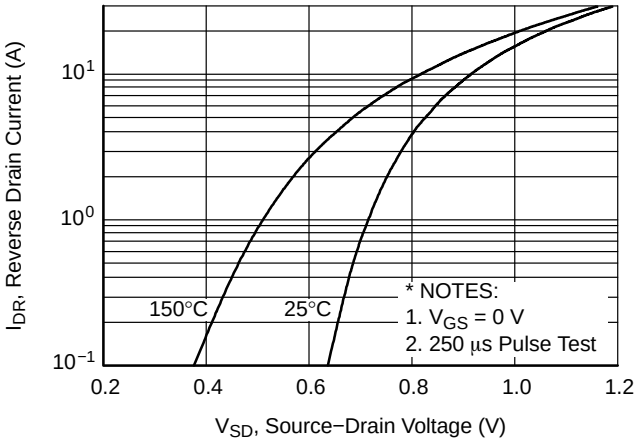


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

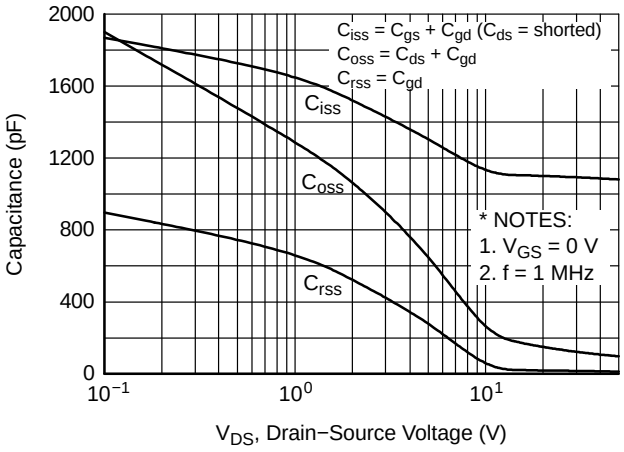


Figure 5. Capacitance Characteristics

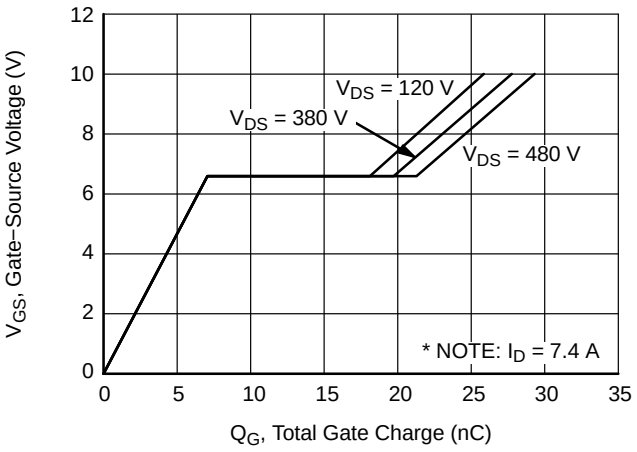


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

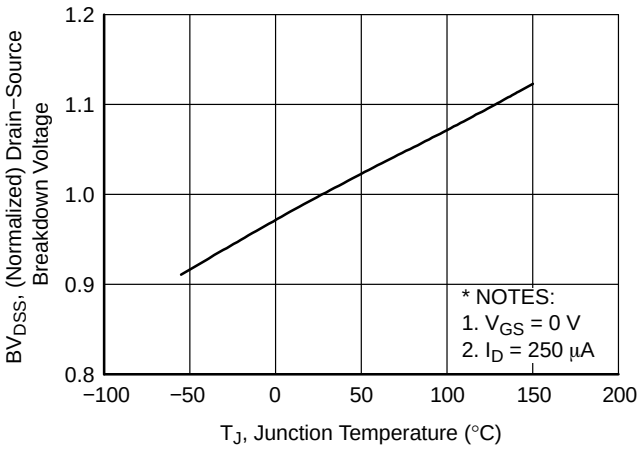


Figure 7. Breakdown Voltage Variation vs. Temperature

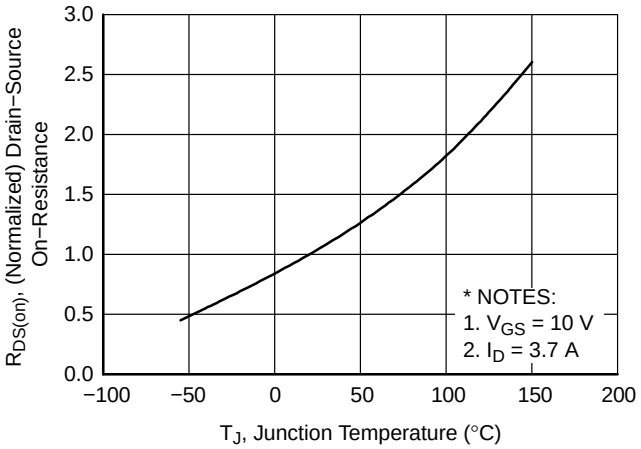


Figure 8. On−Resistance Variation vs. Temperature

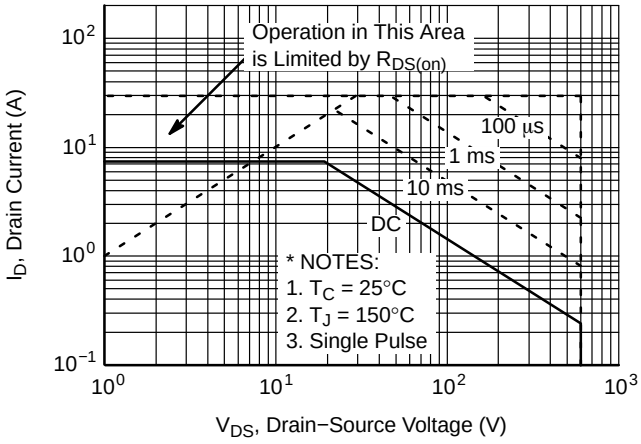


Figure 9. Maximum Safe Operating Area

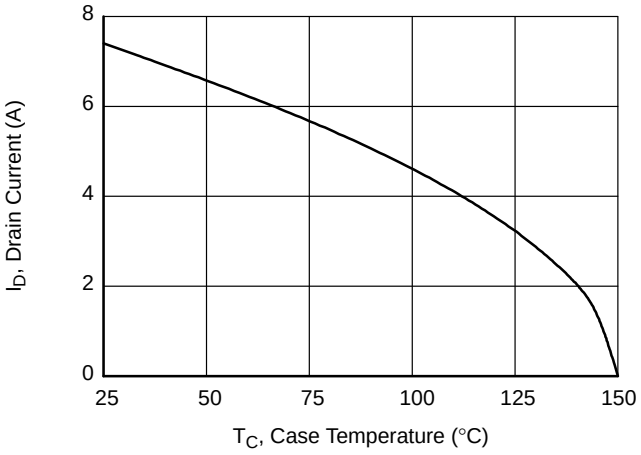


Figure 10. Maximum Drain Current vs. Case Temperature

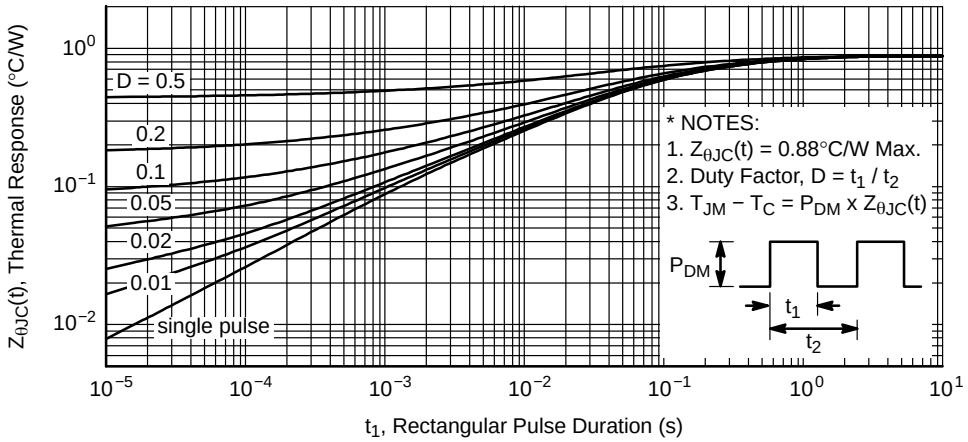


Figure 11. Transient Thermal Response Curve

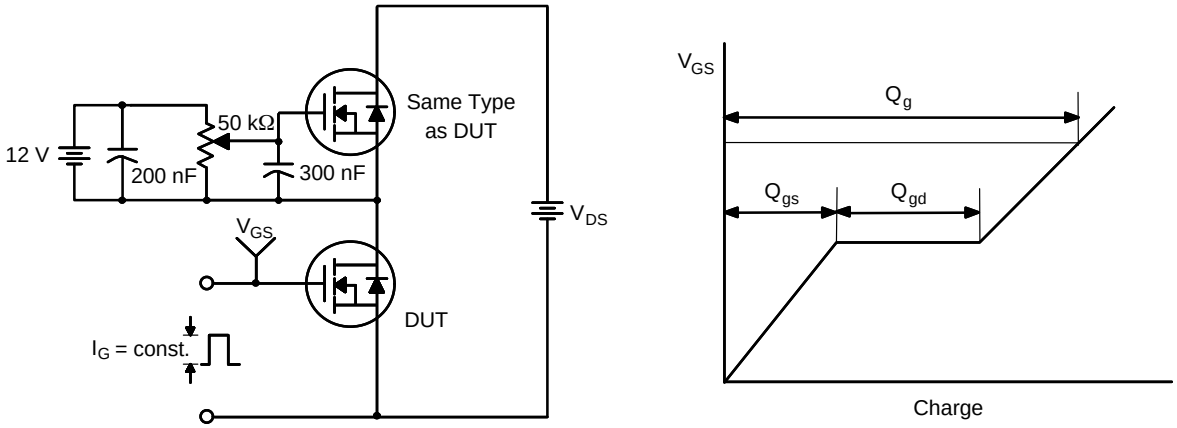


Figure 12. Gate Charge Test Circuit & Waveform

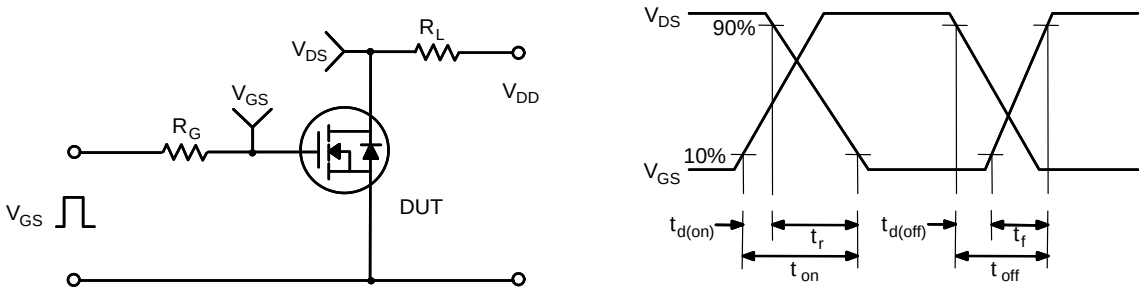


Figure 13. Resistive Switching Test Circuit & Waveforms

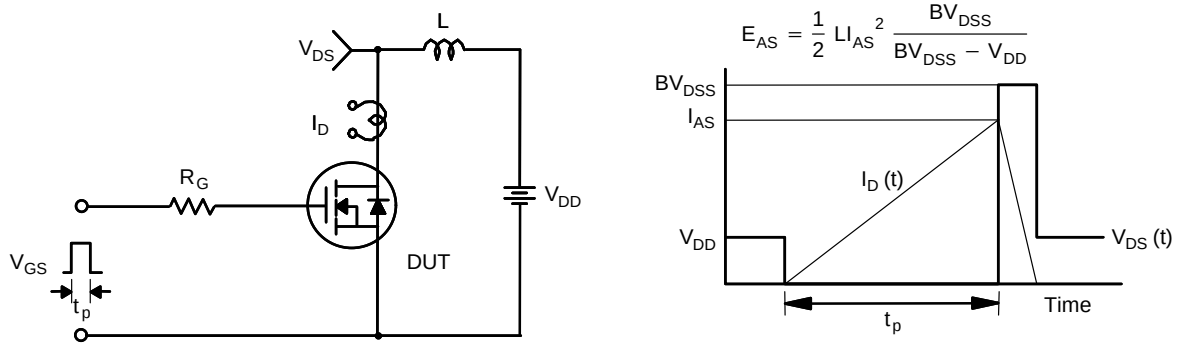


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

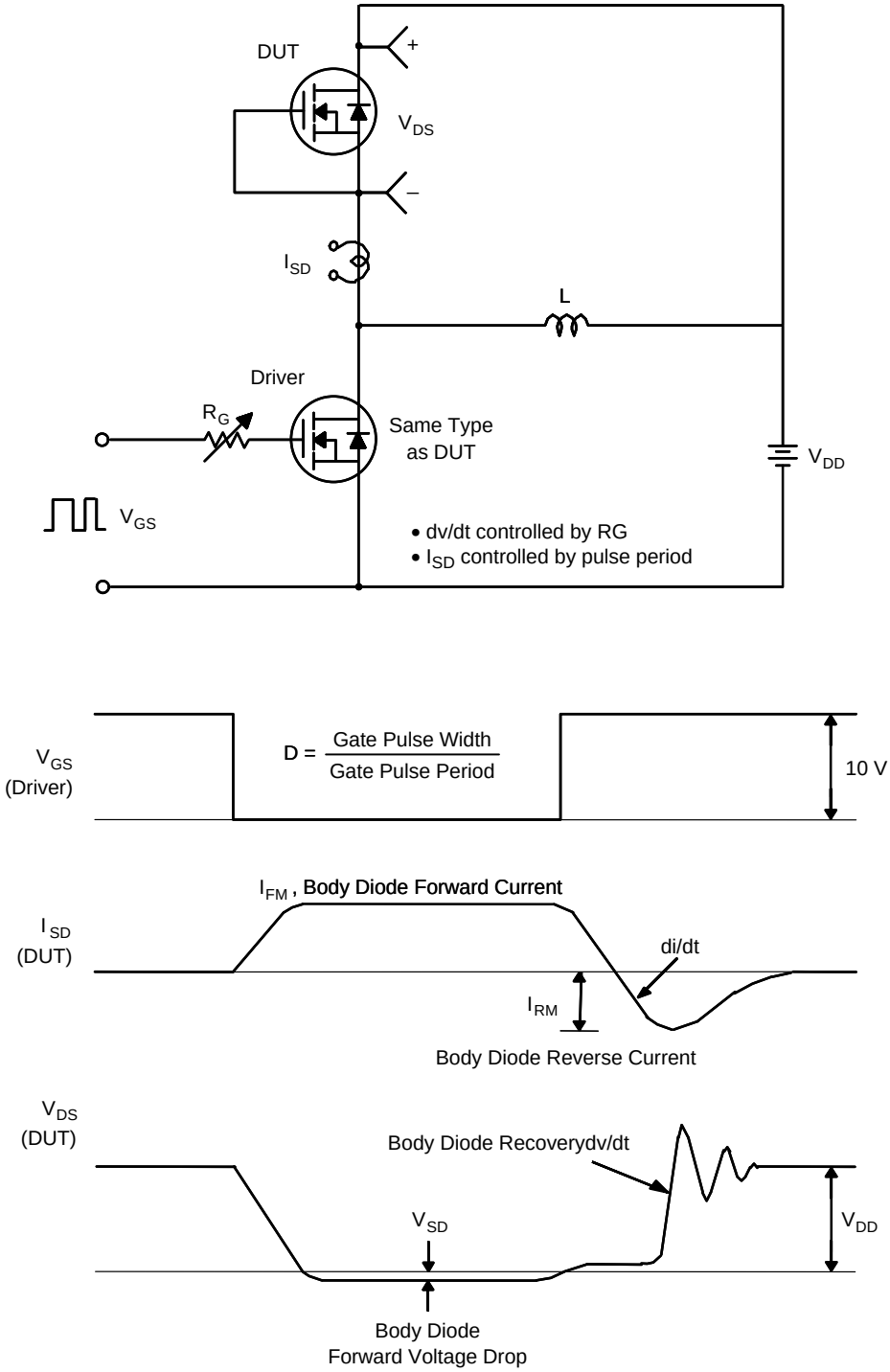


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

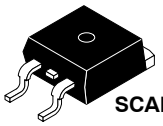
ORDERING INFORMATION

Part Number	Top Mark	Package	Reel Size	Tape Width	Shipping†
FQB7N60TM	FQB7N60	D^2PAK−3	330 mm	24 mm	800 Units / Tape & Reel
FQI7N60TU	FQI7N60	I2PAK	N/A	N/A	50 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

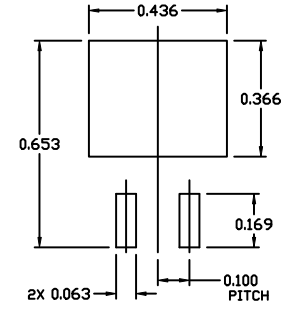
ON Semiconductor®



SCALE 1:1

D²PAK–3 (TO–263, 3–LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021



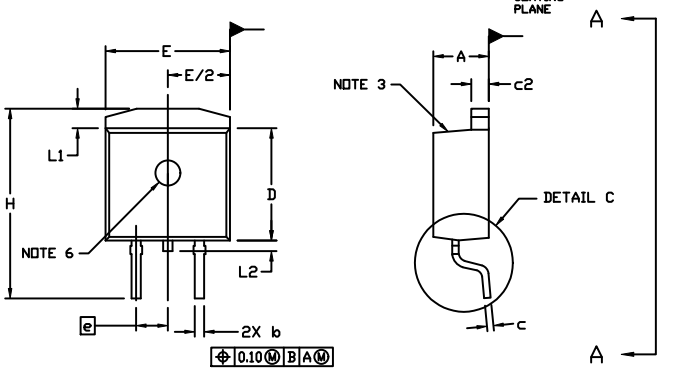
RECOMMENDED
MOUNTING FOOTPRINT

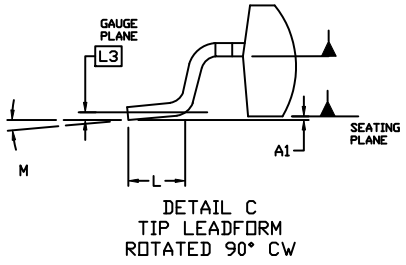
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

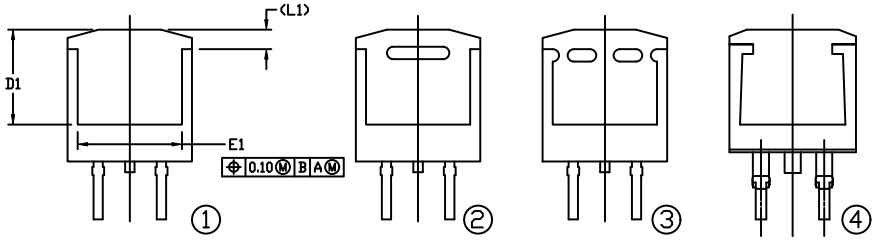
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°





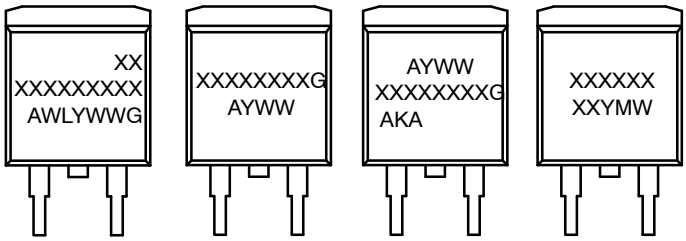
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A–A

VIEW A–A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC | Standard | Rectifier | SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D²PAK–3 (TO–263, 3–LEAD)**	**PAGE 1 OF 1**

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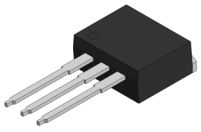
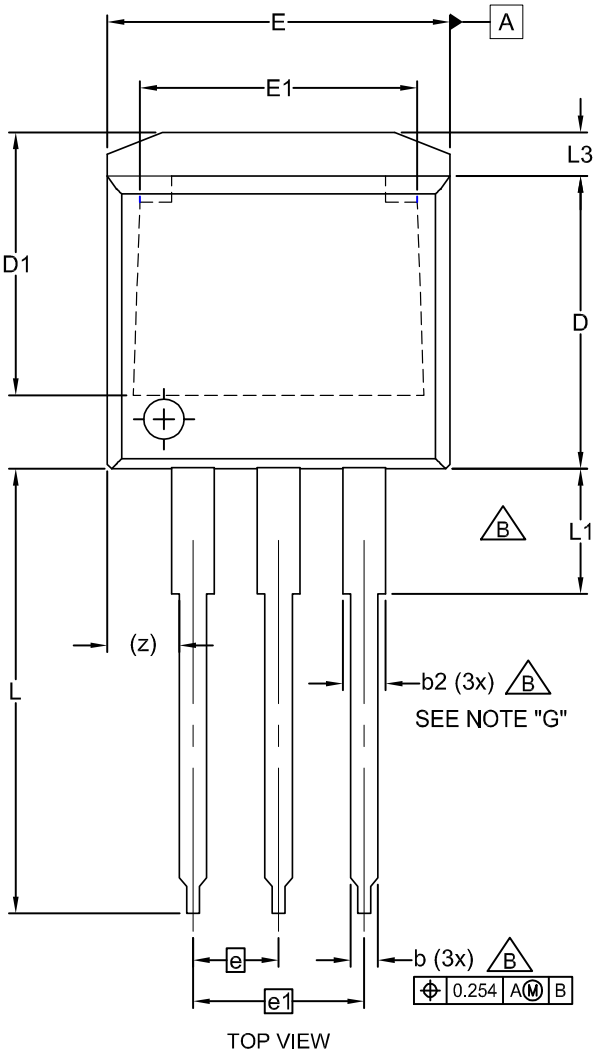
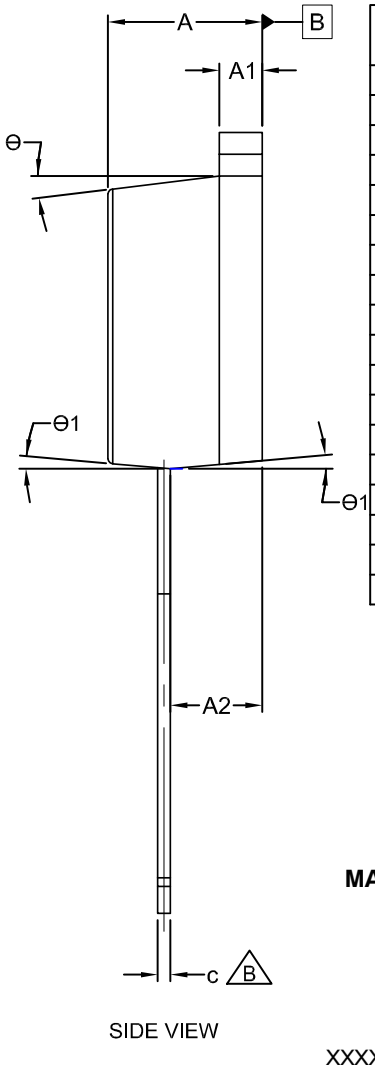
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



I2PAK (TO−262 3 LD)
CASE 418AV
ISSUE A

DATE 30 AUG 2022



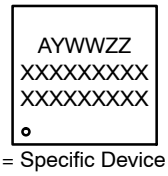


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.06	4.45	4.83
A1	1.14	1.27	1.40
A2	2.03	2.41	2.79
b	0.64	0.77	0.90
b2	1.14	1.46	1.78
c	0.33	0.49	0.64
D	8.64	9.15	9.65
D1	6.86	7.37	7.88
E	9.65	9.97	10.29
E1	6.22	7.28	8.33
e	2.54 BSC		
e1	5.08 BSC		
L	12.70	13.72	14.73
L1	2.80	3.38	3.96
L3	1.00	1.20	1.40
z	2.13 REF		
Θ	0°	--	7°
Θ1	0°	--	5°

NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
B. DOES NOT COMPLY JEDEC STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	I2PAK (TO−262 3 LD)	PAGE 1 OF 1

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