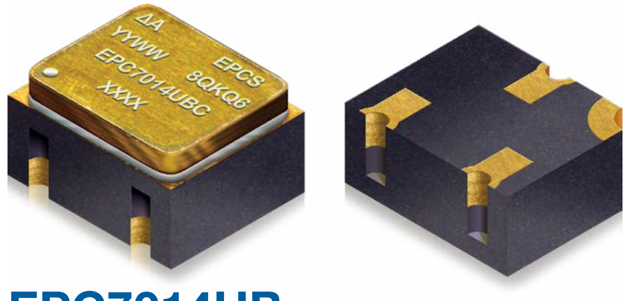
Features

- Ultra-low Q_G For High Efficiency
- Logic Level
- Light Weight –0.058 grams
- No Wire Bond for Higher Reliability and Low Inductance
- Total Dose
  - Rated to 1000 krad
- Single Event
  - SEE immunity for LET of 85 MeV/(mg/cm^2) with V_{DS} up to 100% of rated Breakdown
- Low Dose Rate at 100 mRad/sec
  - Maintains Pre-Rad specification
- Neutron
  - Maintains Pre-Rad specification for up to 3 x 10^{15} Neutrons/cm^2



EPC7014UB

Rad Hard e-GaN® 60 V, 1 A, 580 mΩ Surface Mount (UB)

Description

EPC Space Rad Hard eGaN® power switching HEMTs have been specifically designed for critical applications in the high reliability or commercial satellite space environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

Application

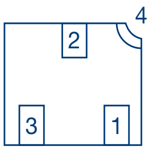
- Commercial Satellite EPS & Avionics
- Deep Space Probes
- High Speed Rad Hard DC-DC Conversion
- Rad Hard Motor Controllers
- Nuclear Facilities

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 3)	200	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	35	

I/O Pin Assignment *(Bottom View)*

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source
4	L	Lid Pad Connection



Absolute Maximum Rating *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain to Source Voltage (Note 1)	60	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	72	
I_D	Continuous Drain Current ID @ V_{GS} = 5 V, T_C = 25°C	1	A
I_{DM}	Single-Pulse Drain Current $t_{pulse} \leq$ 80 µs	4	
V_{GS}	Gate to Source Voltage (Note 2)	+7 / -4	V
T_J , T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
T_{sol}	Package Mounting Surface Temperature	260	
ESD	ESD Class	ΔA	

Electrical Characteristics *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
Drain to Source Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = 0.1 mA		60	-	-	V
Drain to Source Leakage	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	T_C = 25°C	-	10	100	µA
			T_C = 125°C	-		1000	µA
Gate to Source Forward Leakage	I_{GSS}	V_{GS} = 5 V	T_C = 25°C	-	0.01	500	µA
Gate to Source Reverse Leakage	I_{GSS}	V_{GS} = -3 V	T_C = 25°C		-50	-100	µA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.14 mA	T_C = 25°C	0.8	1	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T$	V_{DS} = V_{GS}, I_D = 0.14 mA	-55°C < T_A < 150°C	-	-	-	mV/°C
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	I_D = 1 A, V_{GS} = 5 V	T_C = 25°C	-	340	580	mΩ
Source to Drain Forward Voltage (Note 5)	V_{SD}	I_S = 0.5 A, V_G = 0 V	T_C = 25°C		2.5		V

Dynamic Characteristics *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	C_{ISS}	V_{DS} = 30 V, V_{GS} = 0 V		16	22	pF
Output Capacitance	C_{OSS}	V_{DS} = 30 V, V_{GS} = 0 V		17	26	pF
Reverse transfer Capacitance	C_{RSS}	V_{DS} = 30 V, V_{GS} = 0 V		0.1		pF
Total Gate Charge (Note 7)	Q_G	V_{DS} = 30 V, I_D = 0.5 A		142	184	pC
Gate to Source Charge (Note 7)	Q_{GS}	V_{DS} = 30 V, I_D = 0.5 A		43		pC
Gate to Drain Charge (Note 7)	Q_{GD}	V_{DS} = 30 V, I_D = 0.5 A		25		pC

Radiation Characteristics

EPC Space eGaN® HEMTs are tested according to MIL-STD-750 Method 1019 for total ionizing dose validation. Every manufacturing lot is tested for total ionizing dose of Gamma radiation with an in-situ bias for (i) V_{GS} = 5 V, (ii) V_{DS} = V_{GS} = 0 V and (iii) V_{DS} = 80% B_{VDSS}.

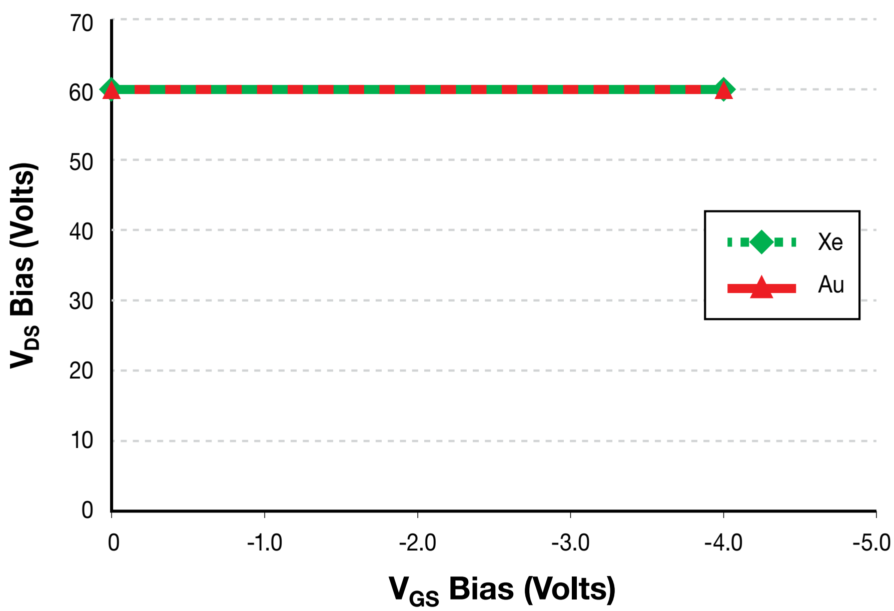
Electrical Characteristics up to 1000 krads *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Drain to Source Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = 0.1 mA	60	-	-	V
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 2 mA	0.8	1.0	2.5	
Drain to Source Leakage	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	-	0.01	100	µA
Gate to Source Forward Leakage	I_{GSS}	V_{GS} = 5 V	-	0.5	500	
Gate to Source Reverse Leakage	I_{GSS}	V_{GS} = -4 V	-	-0.5	-100	
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	I_D = 1 A, V_{GS} = 5 V	-	340	580	mΩ

Typical Single Event Effect Safe Operating Area

Note : All Single Event Effect testing is performed on the K-500 Cyclotron at Texas A&M University

Test	Environment				V_{DS} Voltage (V)	
See SOA	Ion	LET MeV/mg/cm^2	Range µm	Energy MeV	V_{GS} = 0 V	V_{GS} = -4V
	Xe	50	131	1653	60	60
	Au	83.7	130	2482	60	60



Typical Single Event Effect Safe Operating Area

Figure 1: Typical Output Characteristics at 25°C

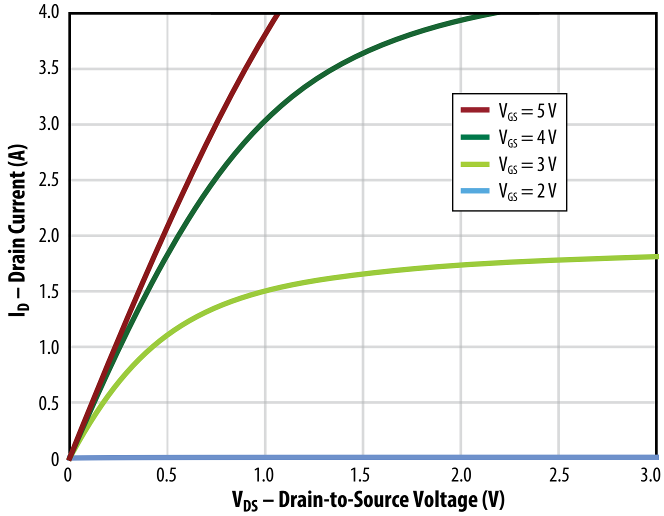


Figure 2: Transfer Characteristics

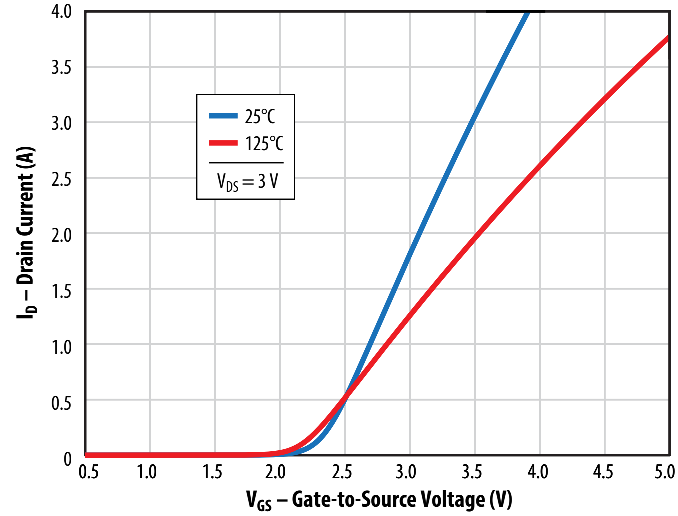


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

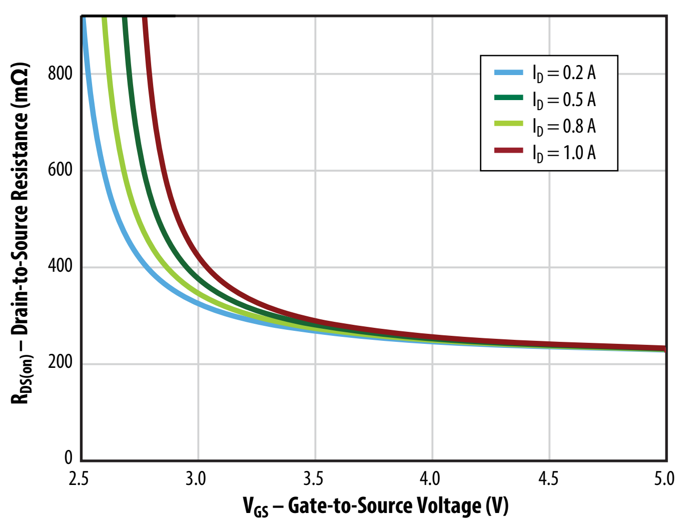


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

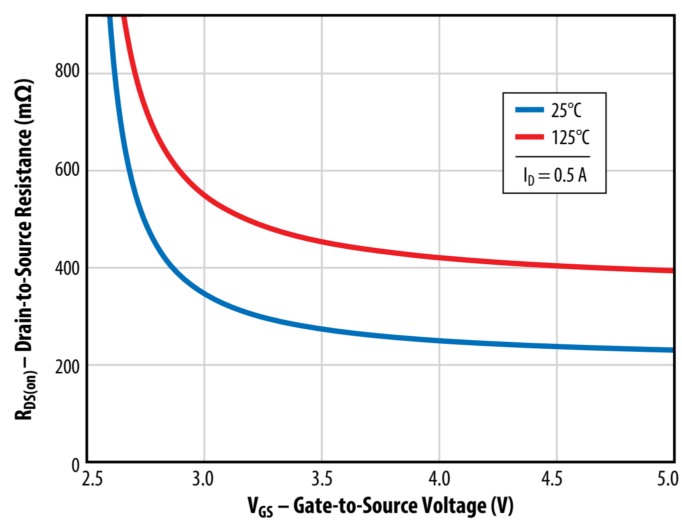


Figure 5a: Capacitance (Linear Scale)

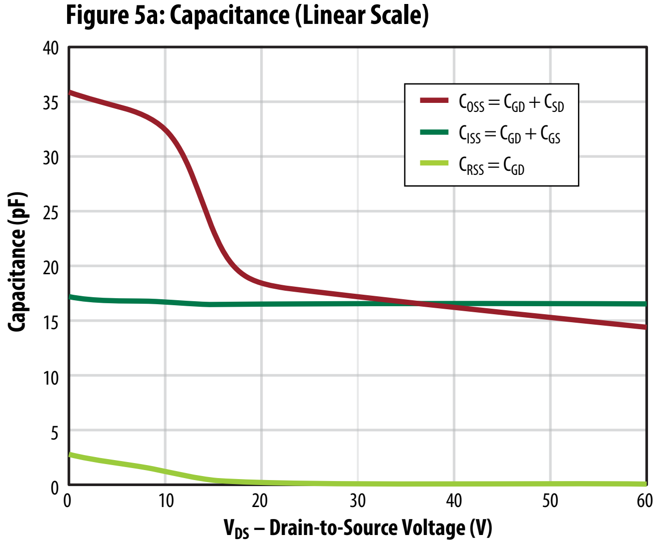


Figure 5b: Capacitance (Log Scale)

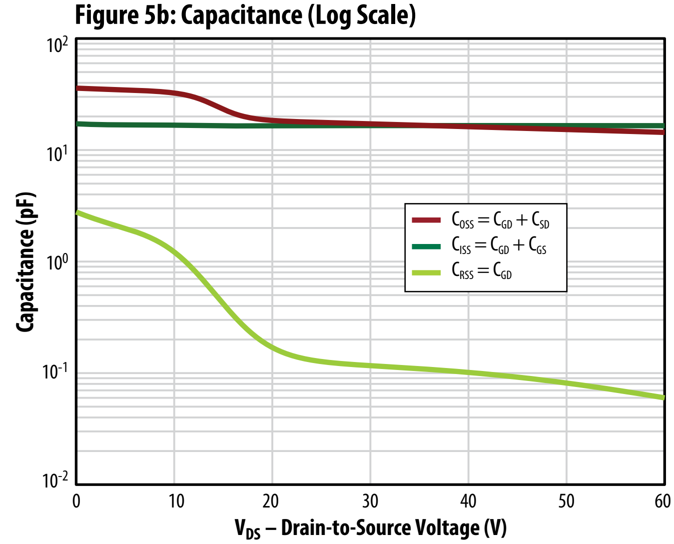


Figure 6: Output Charge and C_{OSS} Stored Energy

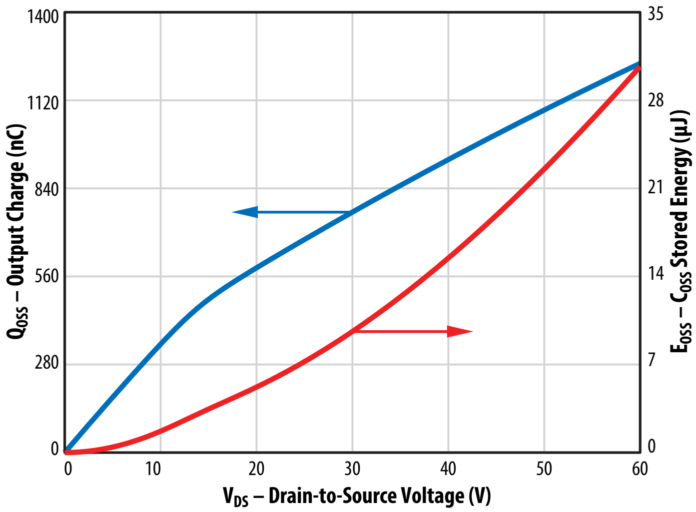


Figure 7: Gate Charge

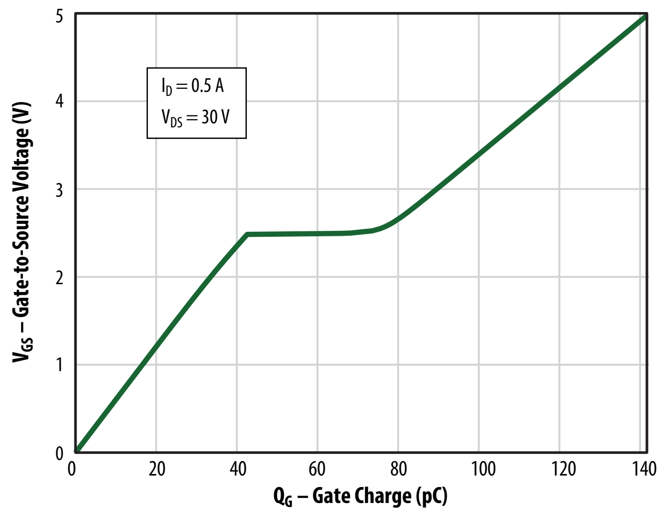


Figure 8: Reverse Drain-Source Characteristics

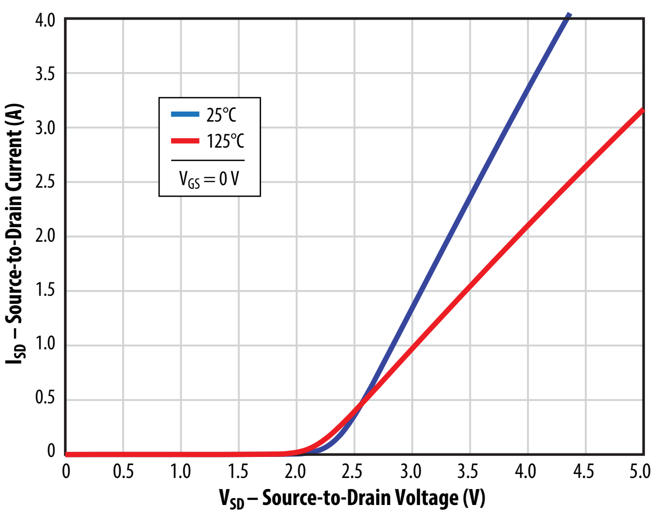


Figure 9: Normalized On-State Resistance vs. Temperature

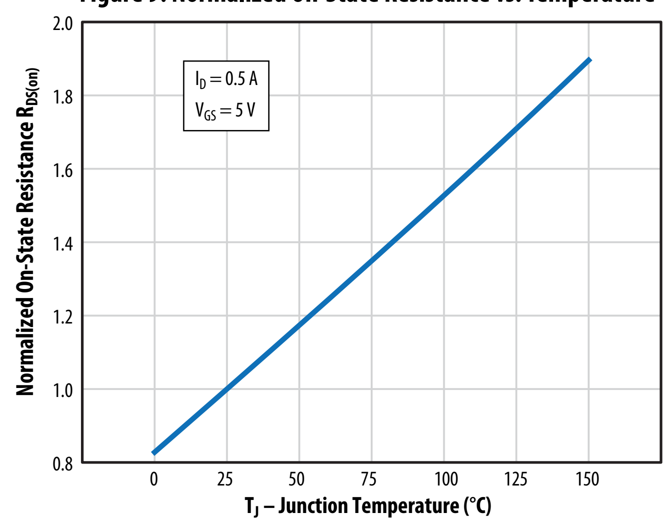
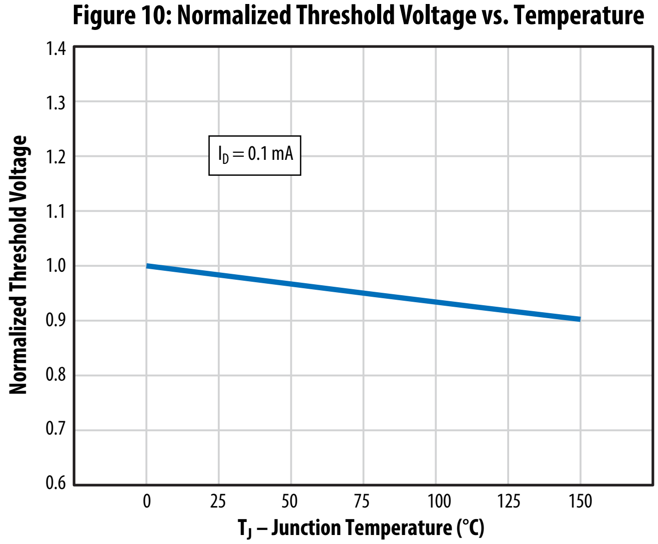


Figure 10: Normalized Threshold Voltage vs. Temperature



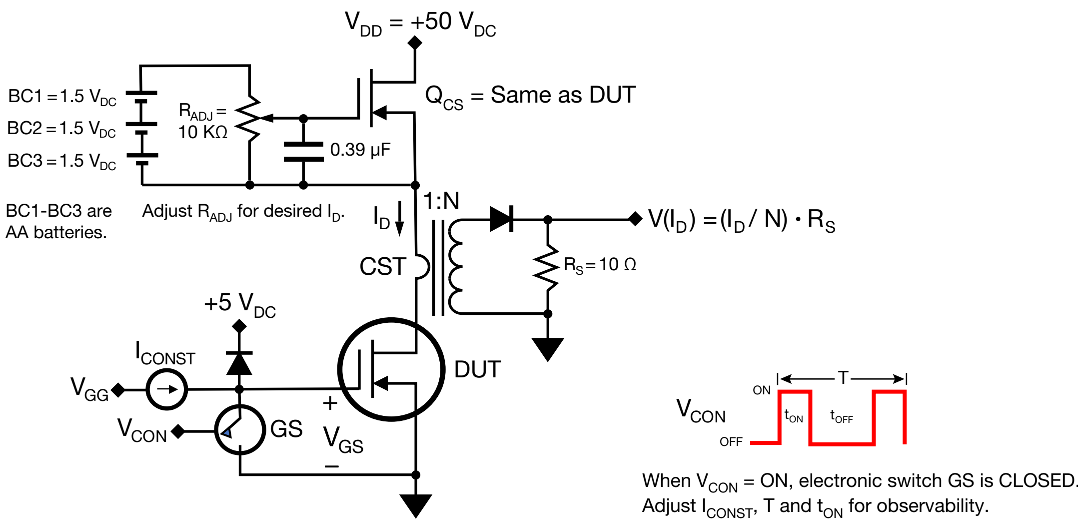


Figure 11. Charge Test Circuit

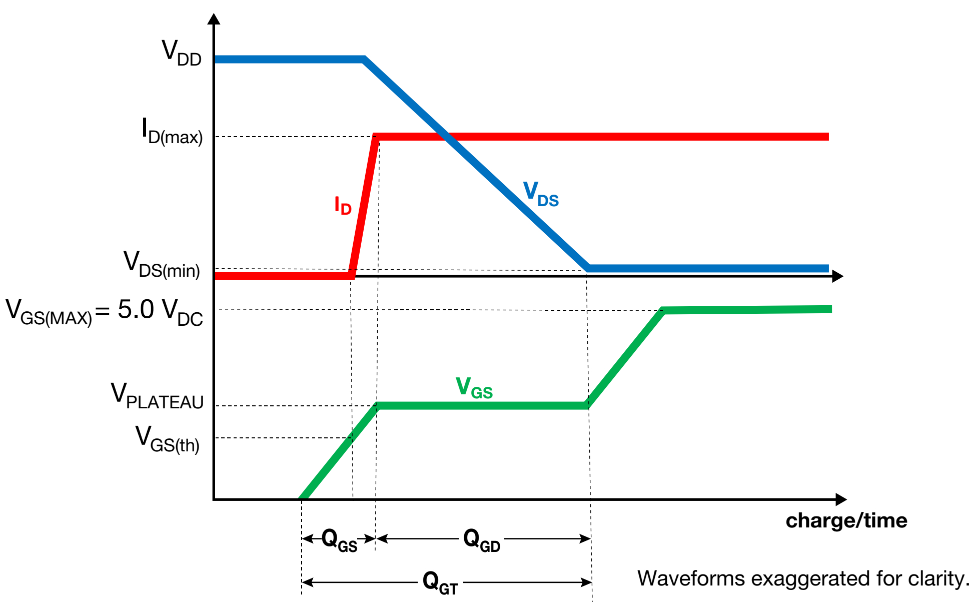
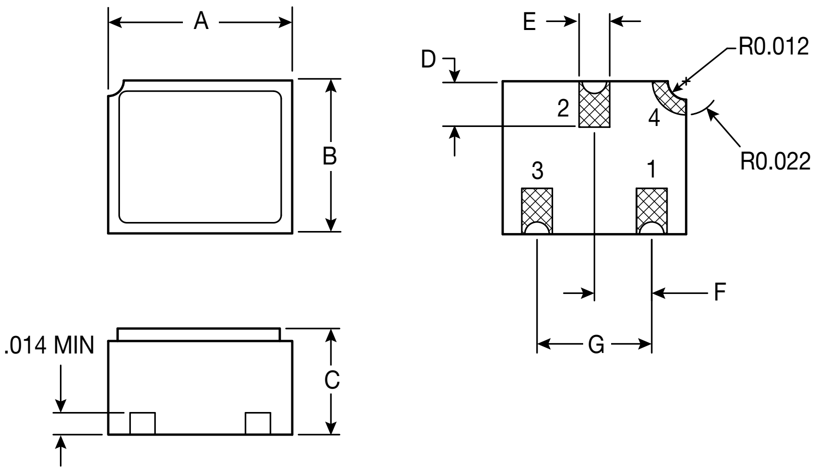


Figure 12. Typical Gate Charge Test Waveform

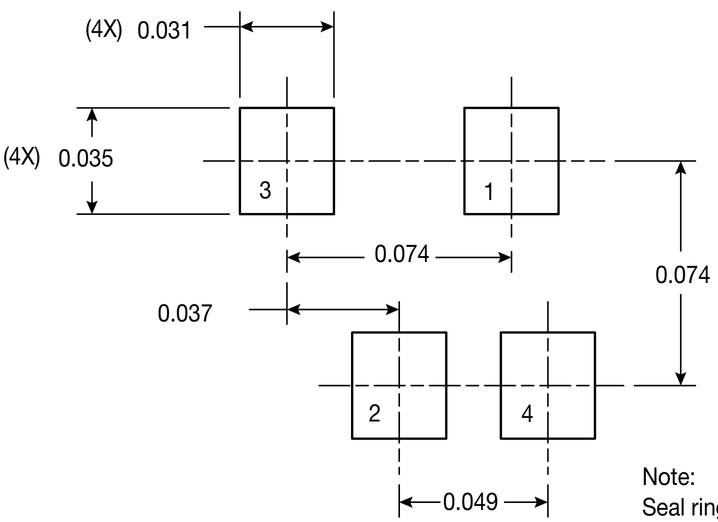
Package Outline and Dimensions



Symbol	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.115	0.128	2.921	3.251
B	0.095	0.108	2.413	2.743
C	0.064	0.082	1.625	2.083
D	0.024	0.036	0.610	0.910
E	0.016	0.024	0.410	0.610
F	0.035	0.039	0.889	0.991
G	0.071	0.079	1.803	2.006

Standard Terminal Pad finish is a solder alloy of 63%Sn37%Pb

UB Footprint for Printed Circuit Board Design



Note:
Seal ring/lid ground optional (pin/pad 4)

Notes

Note 1. NEVER exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.

Note 2. NEVER exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend use at no greater than +5 V as the HEMT is fully conducting at this point.

Note 3. $R_{\theta JA}$ measured with LCC3 package mounted to double-sided PCB, 0.063” thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.

Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 µs and duty cycle is 1%, maximum.

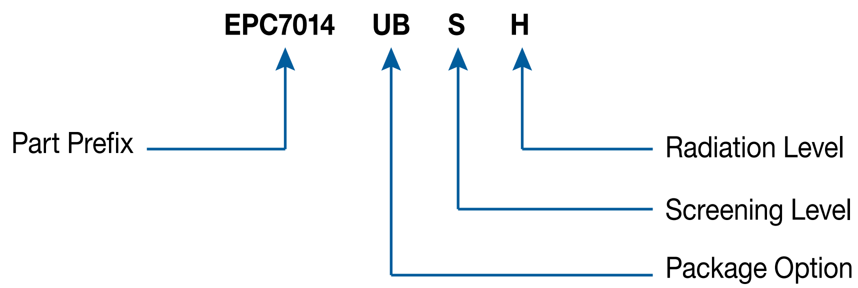
Note 5. With pulse measurement width 100–380 µs.

Note 6. $C_{ISS} = C_{GS} + C_{GD}$ with C_{DS} shorted. $C_{OSS} = C_{DS} + C_{GD}$. $C_{RSS} = C_{GD}$.

Note 7. The gate charge parameters are measured using the circuit shown in Figure 11. Qs and associated components BT1, P1 and C1 form a high speed current source that serves as the test load for the DUT. A constant gate current (I_{const}) of 1.5-3 mA is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}). The DUT is switched ON and OFF using ground-sensed switch GS. The gate current is adjusted to yield the desired charge per unit time (I_{const} · time per division) on the measuring oscilloscope. The GS pulse drive ON time (t_{on})is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch (t_{off} /t_{on}) should be set to 1% maximum. Please note that all gate-related signals are referenced to the “Source Sense” pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{DC}.

Note 8. Guaranteed by design/device construction. Not tested.

EPC Space Part Number Information



Ordering Information Availability

Screening Options	Rad Assurance Options
1 character	1 character
C = Developmental Unit V = Lite Screened S = Space Level[1]	R = 100 krad F = 300 krad G = 500 krad H = 1000 krad

Part Number	Screening Level	Shipping
EPC7014UBC	Engineering Samples	Waffle trays
EPC7014UBSH	Space Level	

[1] Screening and qualification consistent to an equivalent MIL-PRF-19500 specification.

EPC7014UBC devices are intended for engineering development purposes only and are NOT intended to be used as flight units.

Data Package Order Detail
Consistent to MIL-PRF-19500 general specification

SPACE Screen

1. EPC7014UBSH – DATA PACKAGE with QCI Group

A. Certificate of Compliance

B. Serialization Records

C. Assembly Flow Chart

D. SEM Photos and Report

E. Preconditioning – Attributes Data Sheet

– HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data

– HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data

– X-Ray and X-Ray Report

F. Group A – Attributes Data Sheet

– Subgroups A1, A2, A3 and A7 Data

G. Group B – Attributes Data Sheet

– Subgroups B1, B2, B3, B4, B5 and B6 Data

H. Group C – Attributes Data Sheet

– Subgroups C1, C2, C3, C4, C6 and C7 Data

I. Group D – Attributes Data Sheet

– Pre and Post Radiation Data

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Patents

EPC Corporation and EPC Space hold numerous worldwide patents. Any that apply to the product(s) listed in this document are identified by markings on the product(s) or on internal components of the product(s) in accordance with local patent laws.

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Revisions

Datasheet Revision	Product Status
REV Q1	Characterization and Qualification
Preliminary	Production Released

Information subject to change without notice.
Revised September, 2023