

MPSW45, MPSW45A

One Watt Darlington Transistors

NPN Silicon

Features

- Pb-Free Packages are Available*

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|----------------|-------------|---------------------------|
| Collector - Emitter Voltage MPSW45 MPSW45A | V_{CES} | 40 50 | Vdc |
| Collector - Base Voltage MPSW45 MPSW45A | V_{CBO} | 50 60 | Vdc |
| Emitter - Base Voltage | V_{EBO} | 12 | Vdc |
| Collector Current - Continuous | I_C | 1.0 | Adc |
| Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 1.0 8.0 | W mW/ $^\circ\text{C}$ |
| Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | P_D | 2.5 20 | W mW/ $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|-----------------|-----|---------------------------|
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 125 | $^\circ\text{C}/\text{W}$ |
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 50 | $^\circ\text{C}/\text{W}$ |

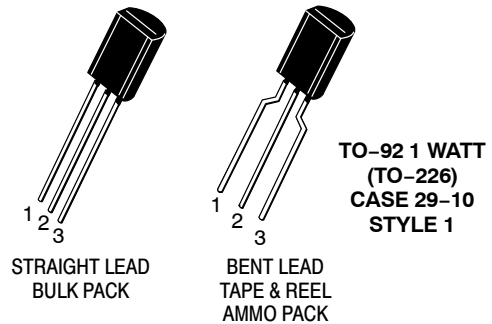
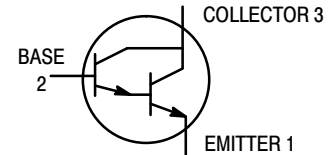
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

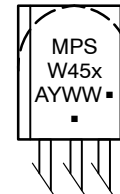


ON Semiconductor®

<http://onsemi.com>



MARKING DIAGRAM



MPSW45x = Device Code
 x = 45A Devices
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MPSW45, MPSW45A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|--|-------------------|----------------------|----------|------------|------|
| OFF CHARACTERISTICS | | | | | |
| Collector – Emitter Breakdown Voltage (I _C = 100 μAdc, V _{BE} = 0) | MPSW45 MPSW45A | V _{(BR)CES} | 40 50 | – – | Vdc |
| Collector – Base Breakdown Voltage (I _C = 100 μAdc, I _E = 0) | MPSW45 MPSW45A | V _{(BR)CBO} | 50 60 | – – | Vdc |
| Emitter – Base Breakdown Voltage (I _E = 10 μAdc, I _C = 0) | | V _{(BR)EBO} | 12 | – | Vdc |
| Collector Cutoff Current (V _{CB} = 30 Vdc, I _E = 0) (V _{CB} = 40 Vdc, I _E = 0) | MPSW45 MPSW45A | I _{CBO} | – – | 100 100 | nAdc |
| Emitter Cutoff Current (V _{EB} = 10 Vdc, I _C = 0) | | I _{EBO} | – | 100 | nAdc |

ON CHARACTERISTICS (Note 1)

| | | | | | |
|--|--|----------------------|---------------------------|-------------------|-----|
| DC Current Gain (I _C = 200 mAdc, V _{CE} = 5.0 Vdc) (I _C = 500 mAdc, V _{CE} = 5.0 Vdc) (I _C = 1.0 Adc, V _{CE} = 5.0 Vdc) | | h _{FE} | 25,000 15,000 4,000 | 150,000 – – | – |
| Collector – Emitter Saturation Voltage (I _C = 1.0 Adc, I _B = 2.0 mAdc) | | V _{CE(sat)} | – | 1.5 | Vdc |
| Base – Emitter Saturation Voltage (I _C = 1.0 Adc, I _B = 2.0 mAdc) | | V _{BE(sat)} | – | 2.0 | Vdc |
| Base – Emitter On Voltage (I _C = 1.0 Adc, V _{CE} = 5.0 Vdc) | | V _{BE(on)} | – | 2.0 | Vdc |

SMALL-SIGNAL CHARACTERISTICS

| | | | | | |
|---|--|-----------------|-----|-----|-----|
| Current – Gain – Bandwidth Product (I _C = 200 mAdc, V _{CE} = 5.0 Vdc, f = 100 MHz) | | f _T | 100 | – | MHz |
| Collector – Base Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz) | | C _{cb} | – | 6.0 | pF |

1. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

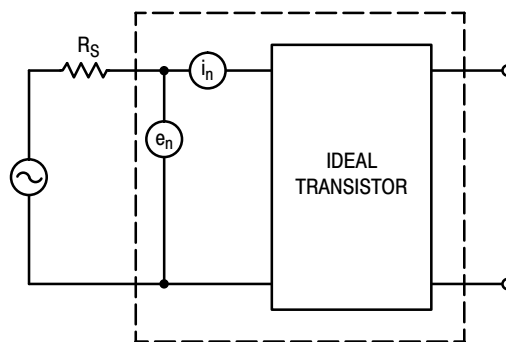


Figure 1. Transistor Noise Model

MPSW45, MPSW45A

NOISE CHARACTERISTICS

($V_{CE} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$)

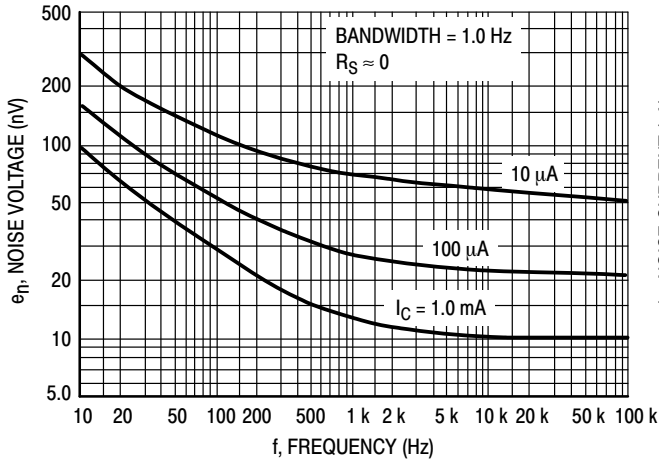


Figure 2. Noise Voltage

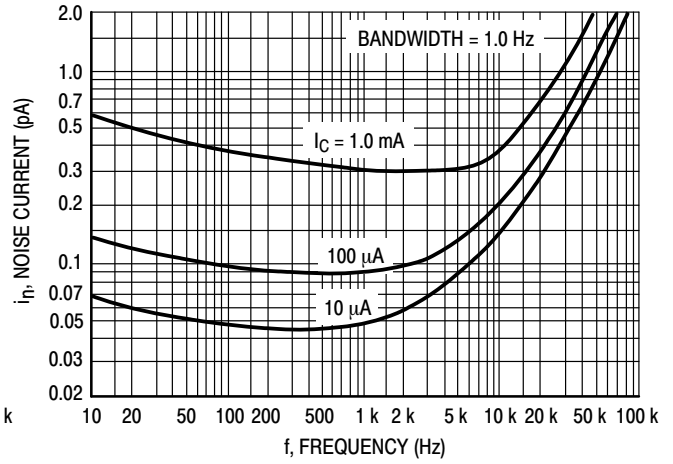


Figure 3. Noise Current

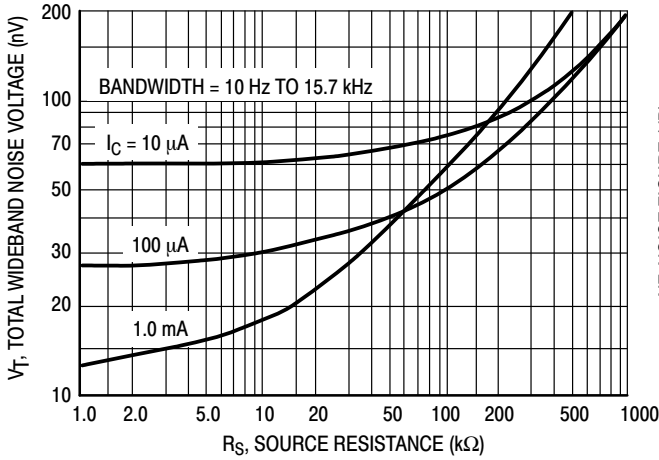


Figure 4. Total Wideband Noise Voltage

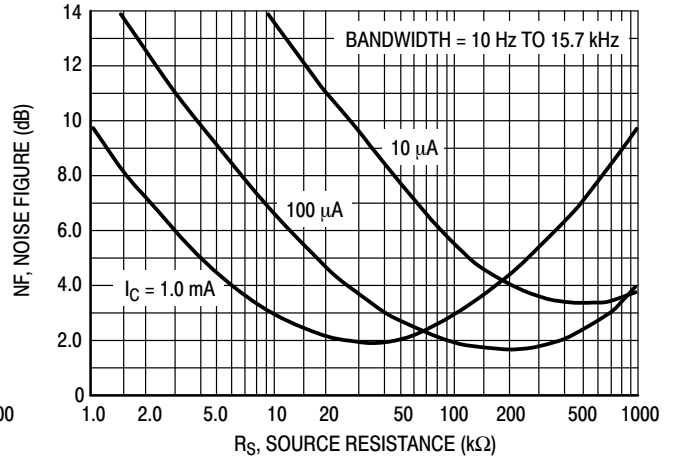


Figure 5. Wideband Noise Figure

MPSW45, MPSW45A

SMALL-SIGNAL CHARACTERISTICS

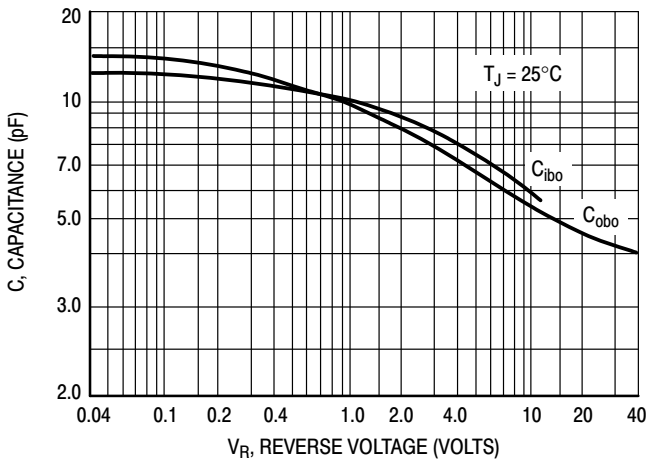


Figure 6. Capacitance

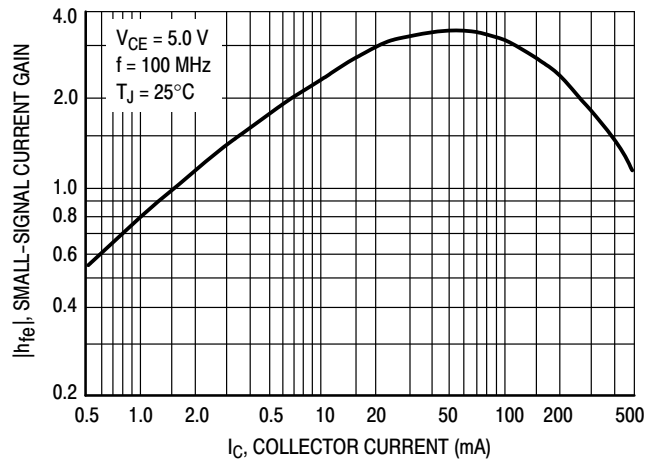


Figure 7. High Frequency Current Gain

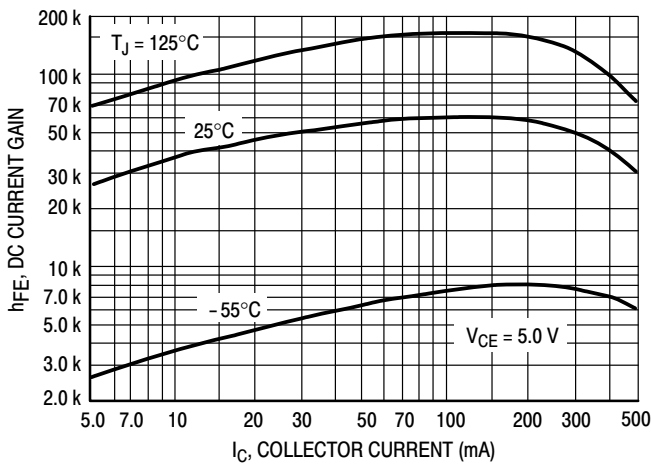


Figure 8. DC Current Gain

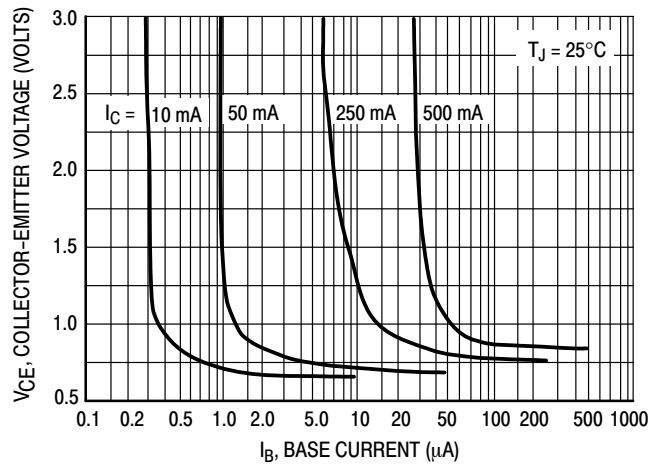


Figure 9. Collector Saturation Region

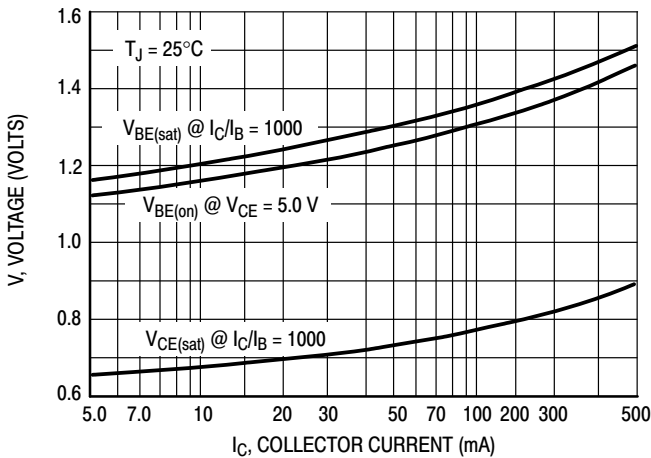


Figure 10. "On" Voltages

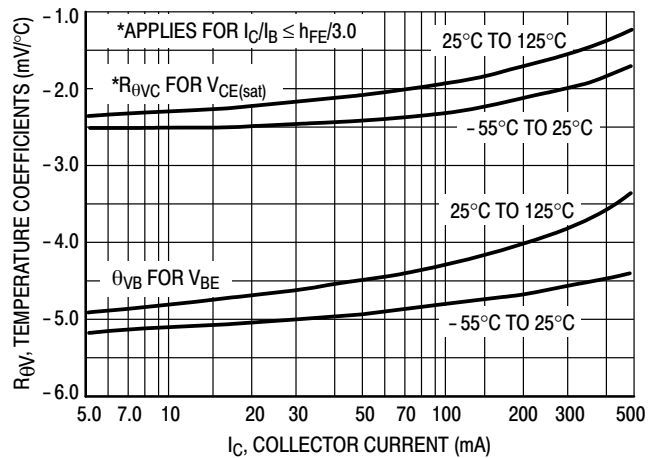


Figure 11. Temperature Coefficients

MPSW45, MPSW45A

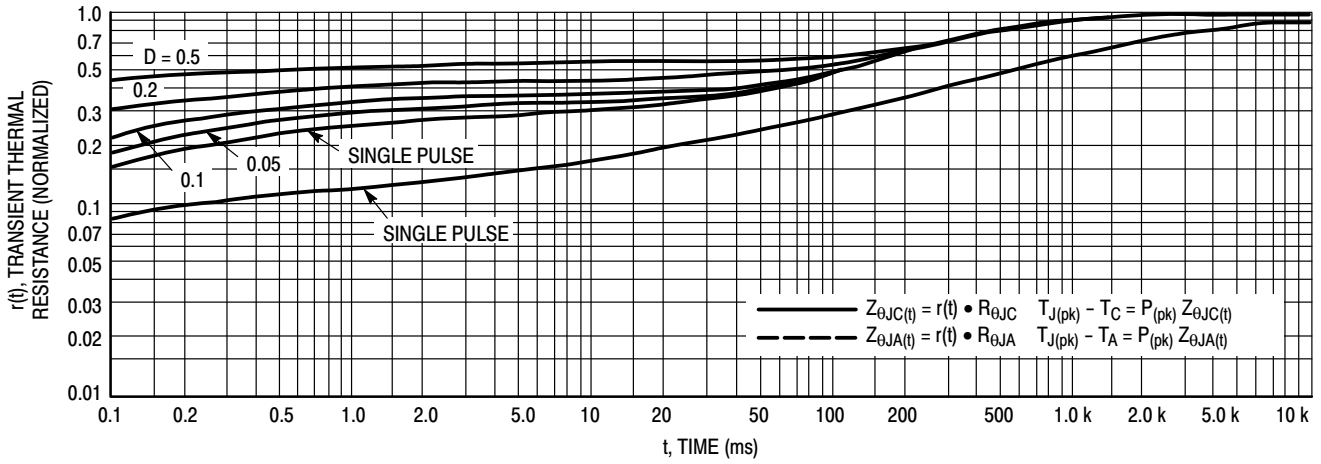


Figure 12. Thermal Response

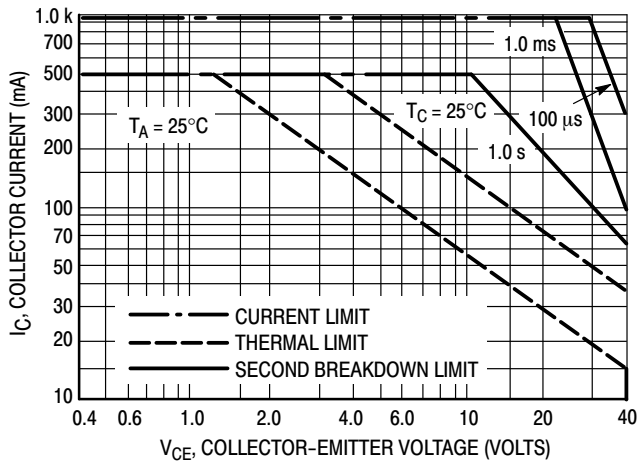
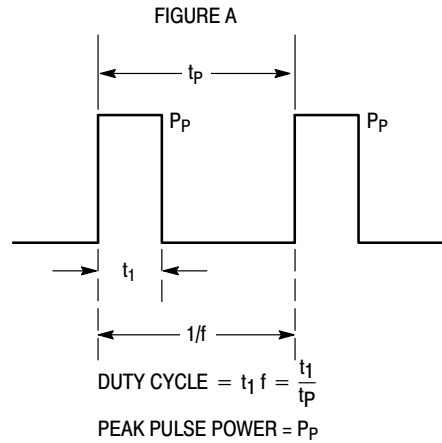


Figure 13. Active Region Safe Operating Area



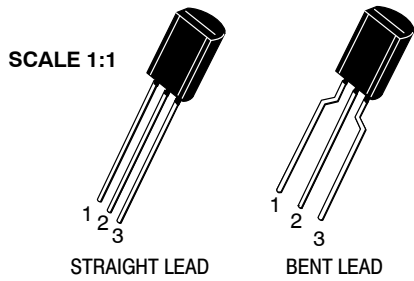
Design Note: Use of Transient Thermal Resistance Data

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|--------------|--------------------|-----------------------|
| MPSW45G | TO-92 (Pb-Free) | 5,000 Units / Box |
| MPSW45RLREG | TO-92 (Pb-Free) | 2,000 / Tape & Reel |
| MPSW45A | TO-92 | 5,000 Units / Box |
| MPSW45AG | TO-92 (Pb-Free) | 5,000 Units / Box |
| MPSW45ARLRA | TO-92 | 2,000 / Tape & Reel |
| MPSW45ARLRAG | TO-92 (Pb-Free) | 2,000 / Tape & Reel |
| MPSW45AZL1 | TO-92 | 2,000 / Ammo Pack |
| MPSW45AZL1G | TO-92 (Pb-Free) | 2,000 / Ammo Pack |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

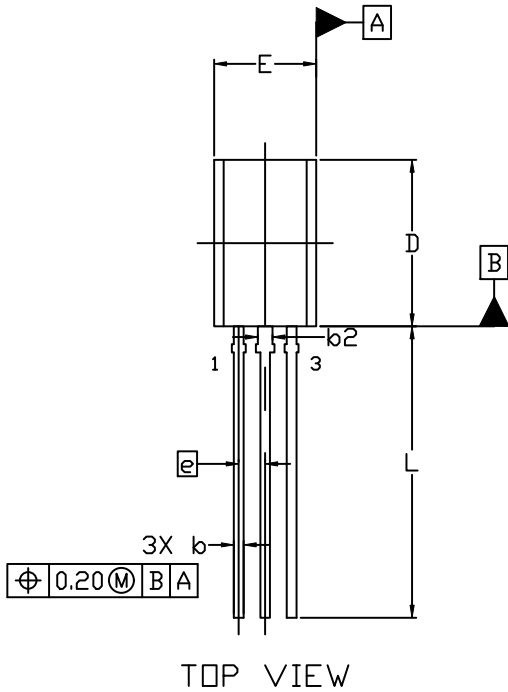
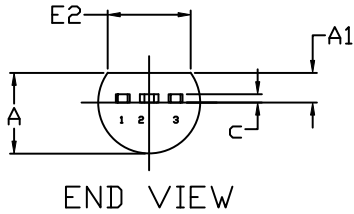
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D

DATE 05 MAR 2021

STRAIGHT LEAD



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 3.75 | 3.90 | 4.05 |
| A1 | 1.28 | 1.43 | 1.58 |
| b | 0.38 | 0.465 | 0.55 |
| b2 | 0.62 | 0.70 | 0.78 |
| c | 0.35 | 0.40 | 0.45 |
| D | 7.85 | 8.00 | 8.15 |
| E | 4.75 | 4.90 | 5.05 |
| E2 | 3.90 | --- | --- |
| e | 1.27 BSC | | |
| L | 13.80 | 14.00 | 14.20 |

STYLES AND MARKING ON PAGE 3

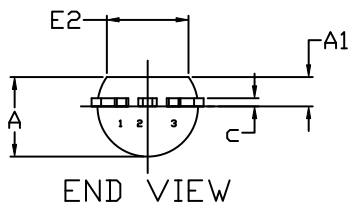
| | | |
|-------------------------|------------------------------|--|
| DOCUMENT NUMBER: | 98AON52857E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | TO-92 (TO-226) 1 WATT | PAGE 1 OF 3 |

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

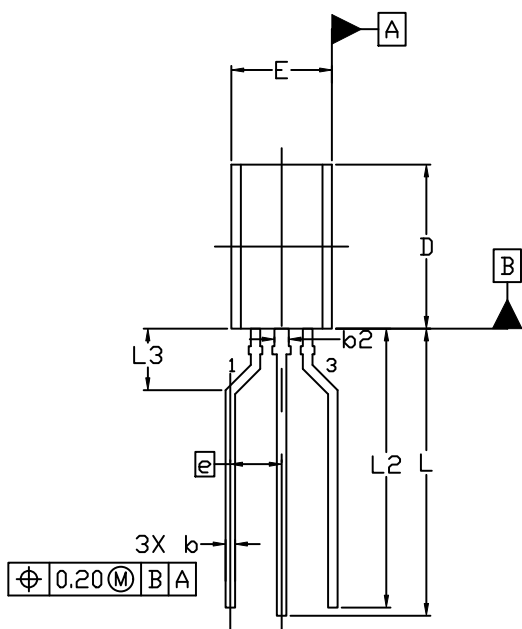
TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD



END VIEW



TOP VIEW


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 3.75 | 3.90 | 4.05 |
| A1 | 1.28 | 1.43 | 1.58 |
| b | 0.38 | 0.465 | 0.55 |
| b2 | 0.62 | 0.70 | 0.78 |
| c | 0.35 | 0.40 | 0.45 |
| D | 7.85 | 8.00 | 8.15 |
| E | 4.75 | 4.90 | 5.05 |
| E2 | 3.90 | --- | --- |
| e | 2.50 BSC | | |
| L | 13.80 | 14.00 | 14.20 |
| L2 | 13.20 | 13.60 | 14.00 |
| L3 | 3.00 REF | | |

STYLES AND MARKING ON PAGE 3

| | | |
|-------------------------|------------------------------|--|
| DOCUMENT NUMBER: | 98AON52857E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | TO-92 (TO-226) 1 WATT | PAGE 2 OF 3 |

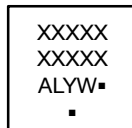
ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D**

DATE 05 MAR 2021

- | | | | | |
|---|--|--|---|---|
| <p>STYLE 1: PIN 1. EMITTER 2. BASE 3. COLLECTOR</p> | <p>STYLE 2: PIN 1. BASE 2. EMITTER 3. COLLECTOR</p> | <p>STYLE 3: PIN 1. ANODE 2. ANODE 3. CATHODE</p> | <p>STYLE 4: PIN 1. CATHODE 2. CATHODE 3. ANODE</p> | <p>STYLE 5: PIN 1. DRAIN 2. SOURCE 3. GATE</p> |
| <p>STYLE 6: PIN 1. GATE 2. SOURCE & SUBSTRATE 3. DRAIN</p> | <p>STYLE 7: PIN 1. SOURCE 2. DRAIN 3. GATE</p> | <p>STYLE 8: PIN 1. DRAIN 2. GATE 3. SOURCE & SUBSTRATE</p> | <p>STYLE 9: PIN 1. BASE 1 2. EMITTER 3. BASE 2</p> | <p>STYLE 10: PIN 1. CATHODE 2. GATE 3. ANODE</p> |
| <p>STYLE 11: PIN 1. ANODE 2. CATHODE & ANODE 3. CATHODE</p> | <p>STYLE 12: PIN 1. MAIN TERMINAL 1 2. GATE 3. MAIN TERMINAL 2</p> | <p>STYLE 13: PIN 1. ANODE 1 2. GATE 3. CATHODE 2</p> | <p>STYLE 14: PIN 1. EMITTER 2. COLLECTOR 3. BASE</p> | <p>STYLE 15: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2</p> |
| <p>STYLE 16: PIN 1. ANODE 2. GATE 3. CATHODE</p> | <p>STYLE 17: PIN 1. COLLECTOR 2. BASE 3. EMITTER</p> | <p>STYLE 18: PIN 1. ANODE 2. CATHODE 3. NOT CONNECTED</p> | <p>STYLE 19: PIN 1. GATE 2. ANODE 3. CATHODE</p> | <p>STYLE 20: PIN 1. NOT CONNECTED 2. CATHODE 3. ANODE</p> |
| <p>STYLE 21: PIN 1. COLLECTOR 2. EMITTER 3. BASE</p> | <p>STYLE 22: PIN 1. SOURCE 2. GATE 3. DRAIN</p> | <p>STYLE 23: PIN 1. GATE 2. SOURCE 3. DRAIN</p> | <p>STYLE 24: PIN 1. EMITTER 2. COLLECTOR/ANODE 3. CATHODE</p> | <p>STYLE 25: PIN 1. MT 1 2. GATE 3. MT 2</p> |
| <p>STYLE 26: PIN 1. V_{CC} 2. GROUND 2 3. OUTPUT</p> | <p>STYLE 27: PIN 1. MT 2. SUBSTRATE 3. MT</p> | <p>STYLE 28: PIN 1. CATHODE 2. ANODE 3. GATE</p> | <p>STYLE 29: PIN 1. NOT CONNECTED 2. ANODE 3. CATHODE</p> | <p>STYLE 30: PIN 1. DRAIN 2. GATE 3. SOURCE</p> |
| <p>STYLE 31: PIN 1. GATE 2. DRAIN 3. SOURCE</p> | <p>STYLE 32: PIN 1. BASE 2. COLLECTOR 3. EMITTER</p> | <p>STYLE 33: PIN 1. RETURN 2. INPUT 3. OUTPUT</p> | <p>STYLE 34: PIN 1. INPUT 2. GROUND 3. LOGIC</p> | <p>STYLE 35: PIN 1. GATE 2. COLLECTOR 3. EMITTER</p> |

**GENERIC
MARKING DIAGRAM***




- XXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|------------------------------|--|
| DOCUMENT NUMBER: | 98AON52857E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | TO-92 (TO-226) 1 WATT | PAGE 3 OF 3 |

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales