

PNP Epitaxial Silicon Transistor

KSA1298

Low Frequency Power Amplifier

• Complement to KSC3265

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

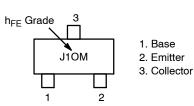
Symbol	Parameter	Ratings	Unit
V_{CBO}	Collector-Base Voltage	-30	V
V_{CEO}	Collector-Emitter Voltage	-25	V
V _{EBO}	Emitter-Base Voltage	-5	V
I _C	Collector Current	-800	mA
Ι _Β	Base Current	-160	mA
P _C	Collector Power Dissipation	200	mW
TJ	Junction Temperature	150	°C
T _{STG}	Storage Temperature	-55 ~ 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



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MARKING DIAGRAM



J1O = Specific Device Code

M = Date Code

ORDERING INFORMATION

Device	Package	Shipping
KSA1298YMTF	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
BV _{CEO}	Collector-Emitter Breakdown Voltage	$I_C = -10 \text{ mA}, I_B = 0$	-25	-	-	V
BV _{EBO}	Emitter-Base Breakdown Voltage	$I_E = -1 \text{ mA}, I_C = 0$	- 5	-	-	V
I _{CBO}	Collector Cut-off Current	$V_{CB} = -30 \text{ V}, I_{E} = 0$	-	-	-100	nA
I _{EBO}	Emitter Cut-off Current	$V_{BE} = -5 \text{ V}, I_{C} = 0$	-	-	-100	nA
h _{FE1} h _{FE2}	DC Current Gain	$V_{CE} = -1 \text{ V, } I_{C} = -100 \text{ mA}$ $V_{CE} = -1 \text{ V, } I_{C} = -800 \text{ mA}$	100 40	- -	320 -	
V _{CE} (sat)	Collector-Emitter Saturation Voltage	$I_C = -500 \text{ mA}, I_B = -20 \text{ mA}$	-	-	-0.4	V
V _{BE} (on)	Base-Emitter On Voltage	$V_{CE} = -1 \text{ V, } I_{C} = -10 \text{ mA}$	-0.5	-	-0.8	V
f _T	Current Gain Bandwidth Product	$V_{CE} = -5 \text{ V}, I_{C} = -10 \text{ mA}$	_	120	_	MHz
C _{ob}	Output Capacitance	$V_{CB} = -10 \text{ V}, I_{E} = 0, f = 1 \text{ MHz}$	_	13	-	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

h_{FE1} Classification

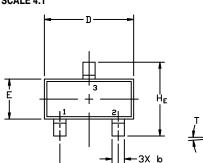
Classification	0	Y	
h _{FE1}	100 ~ 200	160 ~ 320	

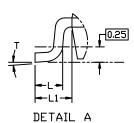


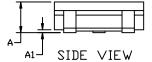


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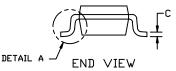
DATE 01 MAR 2023







TOP VIEW



NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES			
DIM	MIN.	N□M.	MAX.	MIN.	N□M.	MAX.
Α	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
С	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
Ε	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
Т	0*		10°	0*		10°

GENERIC MARKING DIAGRAM*

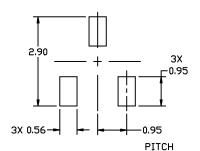


XXX = Specific Device Code

M = Date Code

■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

STYLES ON PAGE 2

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



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STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE	N	
STYLE 9:	STYLE 10:	STYLE 11:	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13:	STYLE 14:
PIN 1. ANODE	PIN 1. DRAIN	PIN 1. ANODE		PIN 1. SOURCE	PIN 1. CATHODE
2. ANODE	2. SOURCE	2. CATHODE		2. DRAIN	2. GATE
3. CATHODE	3. GATE	3. CATHODE-ANODE		3. GATE	3. ANODE
STYLE 15:	STYLE 16:	STYLE 17:	STYLE 18:	STYLE 19:	STYLE 20:
PIN 1. GATE	PIN 1. ANODE	PIN 1. NO CONNECTION	PIN 1. NO CONNECTION	N PIN 1. CATHODE	PIN 1. CATHODE
2. CATHODE	2. CATHODE	2. ANODE	2. CATHODE	2. ANODE	2. ANODE
3. ANODE	3. CATHODE	3. CATHODE	3. ANODE	3. CATHODE-ANODE	3. GATE
STYLE 21:	STYLE 22:	STYLE 23:	STYLE 24:	STYLE 25:	STYLE 26:
PIN 1. GATE	PIN 1. RETURN	PIN 1. ANODE	PIN 1. GATE	PIN 1. ANODE	PIN 1. CATHODE
2. SOURCE	2. OUTPUT	2. ANODE	2. DRAIN	2. CATHODE	2. ANODE
3. DRAIN	3. INPUT	3. CATHODE	3. SOURCE	3. GATE	3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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