

# NPN Silicon Power Darlington

High Voltage Autoprotected D<sup>2</sup>PAK for Surface Mount

## BUB323Z

The BUB323Z is a planar, monolithic, high-voltage power Darlington with a built-in active zener clamping circuit. This device is specifically designed for unclamped, inductive applications such as Electronic Ignition, Switching Regulators and Motor Control.

### Features

- Integrated High-Voltage Active Clamp
- Tight Clamping Voltage Window (350 V to 450 V) Guaranteed Over the -40°C to +125°C Temperature Range
- Clamping Energy Capability 100% Tested in a Live Ignition Circuit
- High DC Current Gain/Low Saturation Voltages Specified Over Full Temperature Range
- Design Guarantees Operation in SOA at All Times
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS

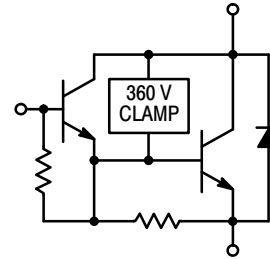
Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	V <sub>CEO</sub>	350	Vdc
Collector-Emitter Voltage	V <sub>EBO</sub>	6.0	Vdc
Collector Current – Continuous	I <sub>C</sub>	10	Adc
– Peak	I <sub>CM</sub>	20	
Base Current – Continuous	I <sub>B</sub>	3.0	Adc
– Peak	I <sub>BM</sub>	6.0	
Total Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	150 1.0	W W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +175	°C

### THERMAL CHARACTERISTICS

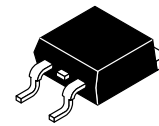
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.0	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8 in from Case for 5 Seconds	T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

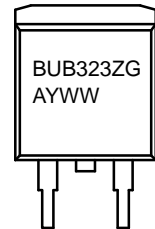
AUTOPROTECTED  
DARLINGTON  
10 AMPERES  
360-450 VOLTS CLAMP  
150 WATTS



### MARKING DIAGRAM



D<sup>2</sup>PAK  
CASE 418B  
STYLE 1



BUB323Z = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

# BUB323Z

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS (Note 1)

Collector–Emitter Clamping Voltage ( $I_C = 7.0\text{ A}$ ) ( $T_C = -40^\circ\text{C}$ to $+125^\circ\text{C}$ )	$V_{\text{CLAMP}}$	350	–	450	Vdc
Collector–Emitter Cutoff Current ( $V_{\text{CE}} = 200\text{ V}$ , $I_B = 0$ )	$I_{\text{CEO}}$	–	–	100	$\mu\text{Adc}$
Emitter–Base Leakage Current ( $V_{\text{EB}} = 6.0\text{ Vdc}$ , $I_C = 0$ )	$I_{\text{EBO}}$	–	–	50	$\text{mAdc}$

### ON CHARACTERISTICS (Note 1)

Base–Emitter Saturation Voltage ( $I_C = 8.0\text{ Adc}$ , $I_B = 100\text{ mAdc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 0.25\text{ Adc}$ )	$V_{\text{BE(sat)}}$	– –	– –	2.2 2.5	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 7.0\text{ Adc}$ , $I_B = 70\text{ mAdc}$ )  ( $I_C = 8.0\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )  ( $I_C = 10\text{ Adc}$ , $I_B = 0.25\text{ Adc}$ )	$V_{\text{CE(sat)}}$	– – –	– – –	1.6 1.8 1.8 2.1 1.7	Vdc
Base–Emitter On Voltage ( $I_C = 5.0\text{ Adc}$ , $V_{\text{CE}} = 2.0\text{ Vdc}$ ) ( $I_C = 8.0\text{ Adc}$ , $V_{\text{CE}} = 2.0\text{ Vdc}$ )	$V_{\text{BE(on)}}$	1.1 1.3	– –	2.1 2.3	Vdc
Diode Forward Voltage Drop ( $I_F = 10\text{ Adc}$ )	$V_F$	–	–	2.5	Vdc
DC Current Gain ( $I_C = 6.5\text{ Adc}$ , $V_{\text{CE}} = 1.5\text{ Vdc}$ ) ( $I_C = 5.0\text{ Adc}$ , $V_{\text{CE}} = 4.6\text{ Vdc}$ )	$h_{\text{FE}}$	150 500	– –	– 3400	–

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 0.2\text{ Adc}$ , $V_{\text{CE}} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	–	–	2.0	MHz
Output Capacitance ( $V_{\text{CB}} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	$C_{\text{ob}}$	–	–	200	pF
Input Capacitance ( $V_{\text{EB}} = 6.0\text{ V}$ )	$C_{\text{ib}}$	–	–	550	pF

### CLAMPING ENERGY (See Notes)

Repetitive Non–Destructive Energy Dissipated at turn–off: ( $I_C = 7.0\text{ A}$ , $L = 8.0\text{ mH}$ , $R_{\text{BE}} = 100\ \Omega$ ) (see Figures 2 and 4)	$W_{\text{CLAMP}}$	200	–	–	mJ
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### SWITCHING CHARACTERISTICS: Inductive Load ( $L = 10\text{ mH}$ )

Fall Time	$(I_C = 6.5\text{ A}$ , $I_{\text{B1}} = 45\text{ mA}$ , $V_{\text{BE(off)}} = 0$ , $R_{\text{BE(off)}} = 0$ , $V_{\text{CC}} = 14\text{ V}$ , $V_Z = 300\text{ V}$ )	$t_{\text{fi}}$	–	625	–	ns
Storage Time		$t_{\text{si}}$	–	10	30	$\mu\text{s}$
Cross–over Time		$t_c$	–	1.7	–	$\mu\text{s}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle = 2.0%.

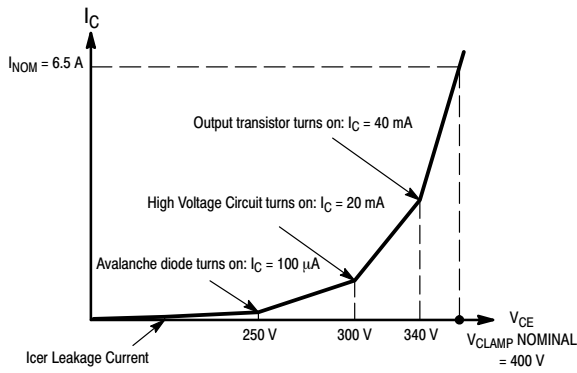


Figure 1.  $I_C = f(V_{CE})$  Curve Shape

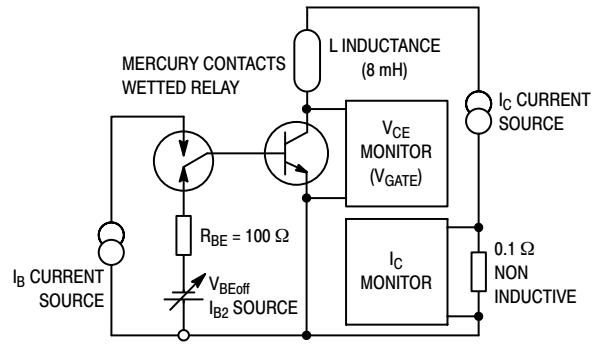


Figure 2. Basic Energy Test Circuit

By design, the BU323Z has a built-in avalanche diode and a special high voltage driving circuit. During an auto-protect cycle, the transistor is turned on again as soon as a voltage, determined by the zener threshold and the network, is reached. This prevents the transistor from going into a Reverse Bias Operating limit condition. Therefore, the device will have an extended safe operating area and will always appear to be in “FBSOA.” Because of the built-in zener and associated network, the  $I_C = f(V_{CE})$  curve exhibits an unfamiliar shape compared to standard products as shown in Figure 1.

The bias parameters,  $V_{CLAMP}$ ,  $I_{B1}$ ,  $V_{BE(off)}$ ,  $I_{B2}$ ,  $I_C$ , and the inductance, are applied according to the Device Under Test (DUT) specifications.  $V_{CE}$  and  $I_C$  are monitored by the test system while making sure the load line remains within the limits as described in Figure 4.

Note: All BU323Z ignition devices are 100% energy tested, per the test circuit and criteria described in Figures 2 and 4, to the minimum guaranteed repetitive energy, as specified in the device parameter section. The device can sustain this energy on a repetitive basis without degrading any of the specified electrical characteristics of the devices. The units under test are kept functional during the complete test sequence for the test conditions described:

$I_{C(peak)} = 7.0 \text{ A}$ ,  $I_{CH} = 5.0 \text{ A}$ ,  $I_{CL} = 100 \text{ mA}$ ,  $I_B = 100 \text{ mA}$ ,  $R_{BE} = 100 \text{ Ohms}$ ,  $V_{gate} = 280 \text{ V}$ ,  $L = 8.0 \text{ mH}$

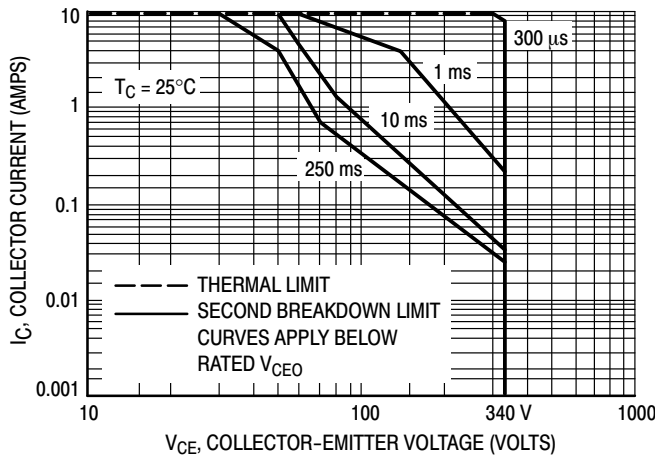
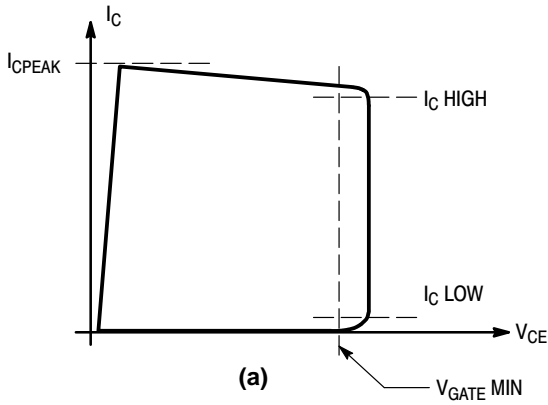
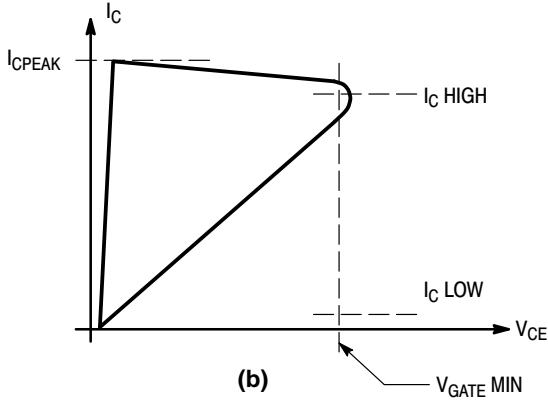


Figure 3. Forward Bias Safe Operating Area

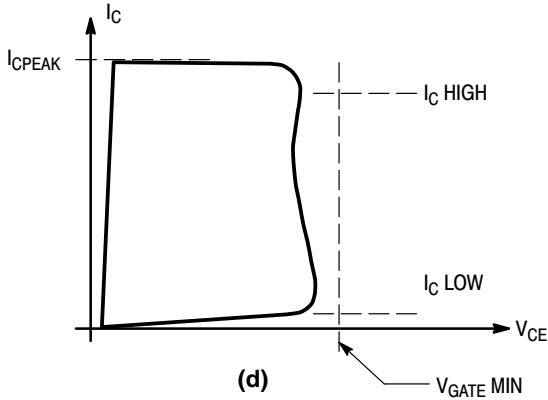
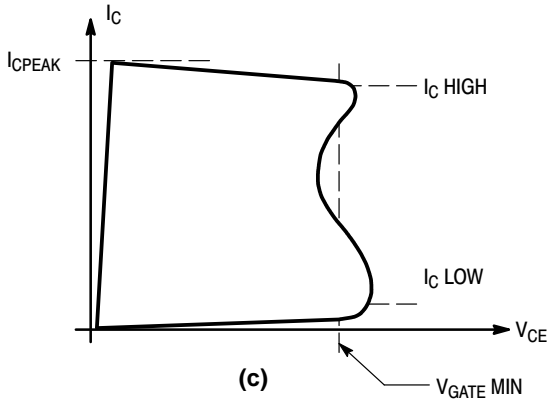


The shaded area represents the amount of energy the device can sustain, under given DC biases ( $I_C/I_B/V_{BE(off)}/R_{BE}$ ), without an external clamp; see the test schematic diagram, Figure 2.

The transistor **PASSES** the Energy test if, for the inductive load and  $I_{CPEAK}/I_B/V_{BE(off)}$  biases, the  $V_{CE}$  remains outside the shaded area and greater than the  $V_{GATE}$  minimum limit, Figure 4a.



The transistor **FAILS** if the  $V_{CE}$  is less than the  $V_{GATE}$  (minimum limit) at any point along the  $V_{CE}/I_C$  curve as shown on Figures 4b, and 4c. This assures that hot spots and uncontrolled avalanche are not being generated in the die, and the transistor is not damaged, thus enabling the sustained energy level required.



The transistor **FAILS** if its Collector/Emitter breakdown voltage is less than the  $V_{GATE}$  value, Figure 4d.

Figure 4. Energy Test Criteria for BU323Z

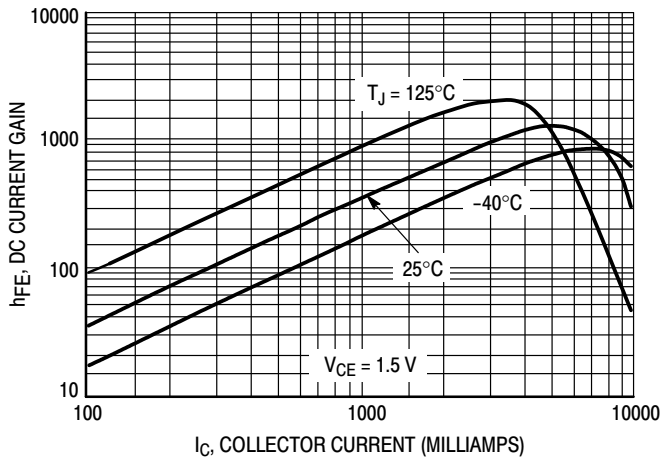


Figure 5. DC Current Gain

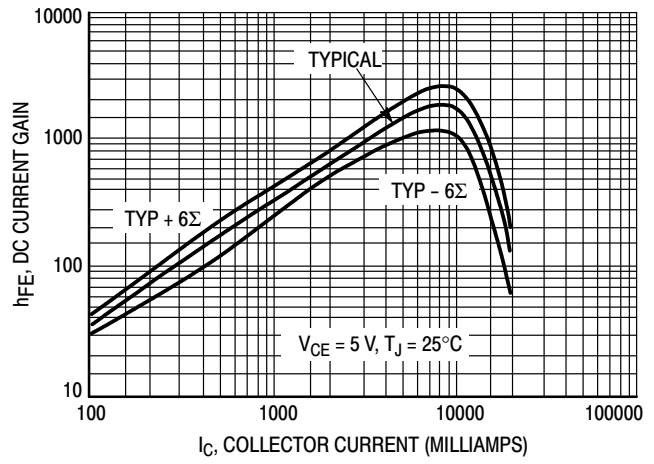


Figure 6. DC Current Gain

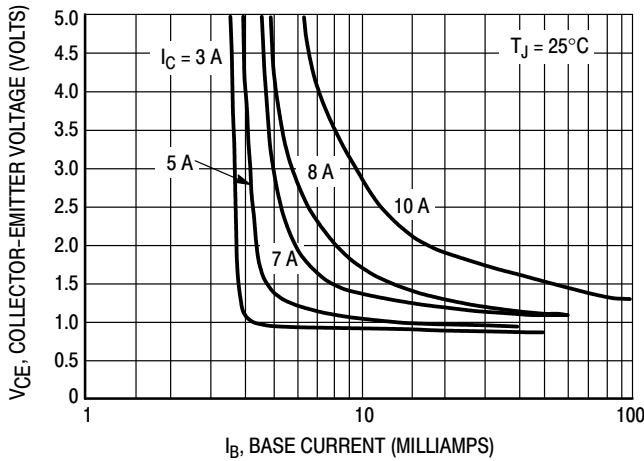


Figure 7. Collector Saturation Region

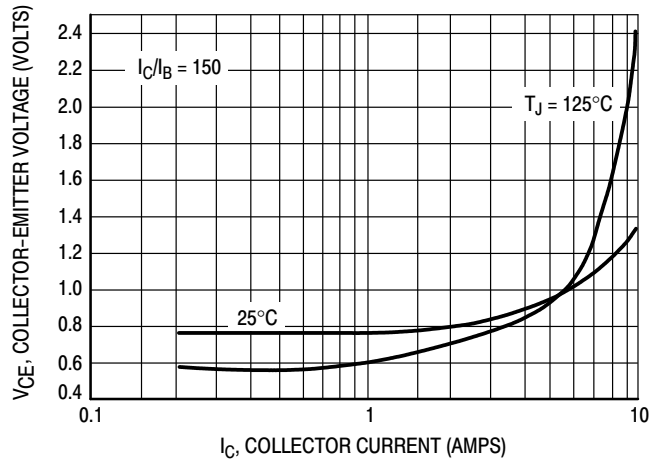


Figure 8. Collector-Emitter Saturation Voltage

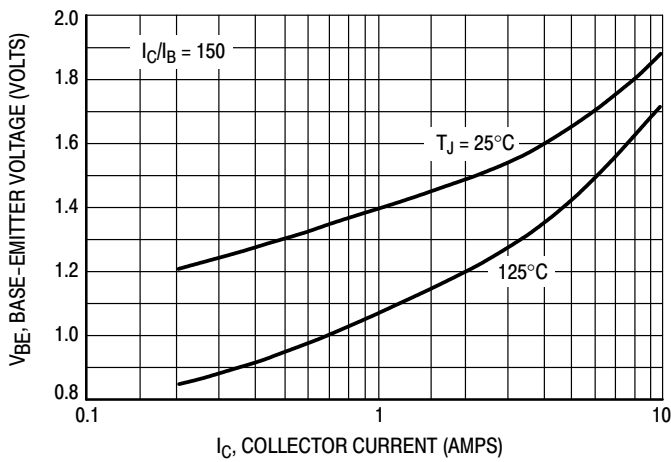


Figure 9. Base-Emitter Saturation Voltage

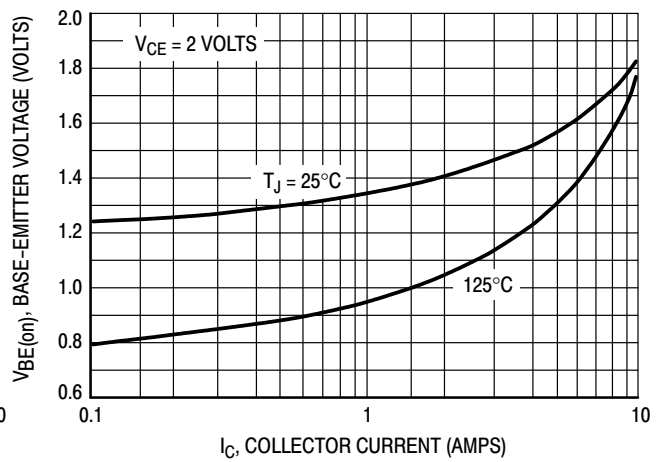


Figure 10. Base-Emitter "ON" Voltages

# BUB323Z

## ORDERING INFORMATION

Device	Package	Shipping†
BUB323ZT4G	D <sup>2</sup> PAK (Pb-Free)	800 Units / Tape & Reel

## DISCONTINUED (Note 2)

BUB323ZG	D <sup>2</sup> PAK (Pb-Free)	50 Units / Rail
NJVBUB323ZT4G*	D <sup>2</sup> PAK (Pb-Free)	800 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

2. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

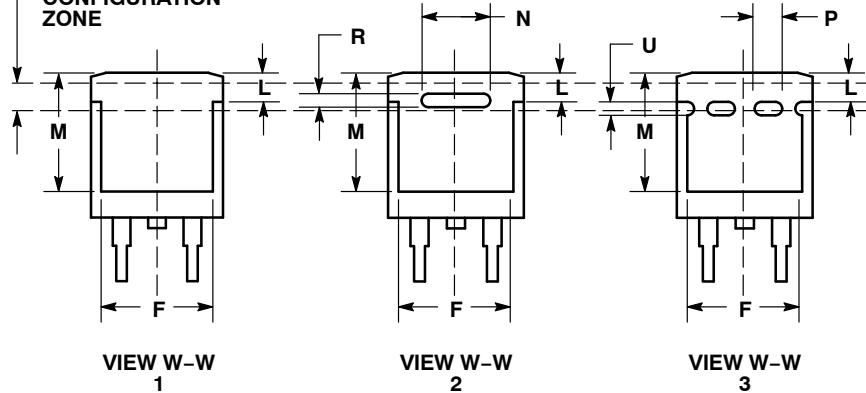


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

**VARIABLE CONFIGURATION ZONE**



- |  |   |   |  |   |  |
|--|---|---|--|---|--|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN | <b>STYLE 3:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | <b>STYLE 4:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 5:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE | <b>STYLE 6:</b><br>PIN 1. NO CONNECT<br>2. CATHODE<br>3. ANODE<br>4. CATHODE |
|--|---|---|--|---|--|

**MARKING INFORMATION AND FOOTPRINT ON PAGE 2**

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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

**GENERIC  
MARKING DIAGRAM\***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator


\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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