

2N4401

General Purpose Transistors

NPN Silicon

Features

- Pb-Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	40	Vdc
Collector – Base Voltage	V_{CBO}	60	Vdc
Emitter – Base Voltage	V_{EBO}	6.0	Vdc
Collector Current – Continuous	I_C	600	mA dc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	625 5.0	mW mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5 12	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

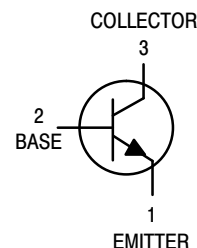
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	200	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	83.3	$^\circ\text{C/W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

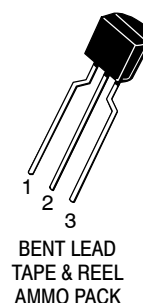
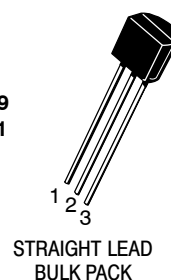


ON Semiconductor®

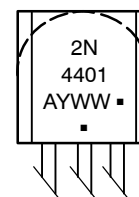
<http://onsemi.com>



TO-92
CASE 29
STYLE 1



MARKING DIAGRAM



2N4401 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

2N4401

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage (Note 1)	($I_C = 1.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	40	–	Vdc
Collector–Base Breakdown Voltage	($I_C = 0.1\text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	60	–	Vdc
Emitter–Base Breakdown Voltage	($I_E = 0.1\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	6.0	–	Vdc
Base Cutoff Current	($V_{CE} = 35\text{ Vdc}$, $V_{EB} = 0.4\text{ Vdc}$)	I_{BEV}	–	0.1	μAdc
Collector Cutoff Current	($V_{CE} = 35\text{ Vdc}$, $V_{EB} = 0.4\text{ Vdc}$)	I_{CEX}	–	0.1	μAdc

ON CHARACTERISTICS (Note 1)

DC Current Gain	($I_C = 0.1\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 1.0\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 10\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 150\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 500\text{ mA}$, $V_{CE} = 2.0\text{ Vdc}$)	h_{FE}	20 40 80 100 40	– – – 300 –	–
Collector–Emitter Saturation Voltage	($I_C = 150\text{ mA}$, $I_B = 15\text{ mA}$) ($I_C = 500\text{ mA}$, $I_B = 50\text{ mA}$)	$V_{CE(sat)}$	– –	0.4 0.75	Vdc
Base–Emitter Saturation Voltage	($I_C = 150\text{ mA}$, $I_B = 15\text{ mA}$) ($I_C = 500\text{ mA}$, $I_B = 50\text{ mA}$)	$V_{BE(sat)}$	0.75 –	0.95 1.2	Vdc

SMALL–SIGNAL CHARACTERISTICS

Current–Gain – Bandwidth Product	($I_C = 20\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f = 100\text{ MHz}$)	f_T	250	–	MHz
Collector–Base Capacitance	($V_{CB} = 5.0\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	C_{cb}	–	6.5	pF
Emitter–Base Capacitance	($V_{EB} = 0.5\text{ Vdc}$, $I_C = 0$, $f = 1.0\text{ MHz}$)	C_{eb}	–	30	pF
Input Impedance	($I_C = 1.0\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ kHz}$)	h_{ie}	1.0	15	k Ω
Voltage Feedback Ratio	($I_C = 1.0\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ kHz}$)	h_{re}	0.1	8.0	$\times 10^{-4}$
Small–Signal Current Gain	($I_C = 1.0\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ kHz}$)	h_{fe}	40	500	–
Output Admittance	($I_C = 1.0\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ kHz}$)	h_{oe}	1.0	30	μmhos

SWITCHING CHARACTERISTICS

Delay Time	($V_{CC} = 30\text{ Vdc}$, $V_{BE} = 2.0\text{ Vdc}$, $I_C = 150\text{ mA}$, $I_{B1} = 15\text{ mA}$)	t_d	–	15	ns
Rise Time		t_r	–	20	ns
Storage Time	($V_{CC} = 30\text{ Vdc}$, $I_C = 150\text{ mA}$, $I_{B1} = I_{B2} = 15\text{ mA}$)	t_s	–	225	ns
Fall Time		t_f	–	30	ns

1. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

ORDERING INFORMATION

Device	Package	Shipping [†]
2N4401	TO–92	5000 Units / Bulk
2N4401G	TO–92 (Pb–Free)	5000 Units / Bulk
2N4401RLRA	TO–92	2000 / Tape & Reel
2N4401RLRAG	TO–92 (Pb–Free)	2000 / Tape & Reel
2N4401RLRMG	TO–92 (Pb–Free)	2000 / Tape & Ammo Box
2N4401RLRP	TO–92	2000 / Tape & Ammo Box
2N4401RLRPG	TO–92 (Pb–Free)	2000 / Tape & Ammo Box

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

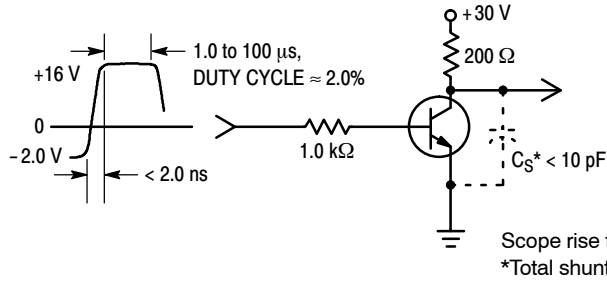


Figure 1. Turn-On Time

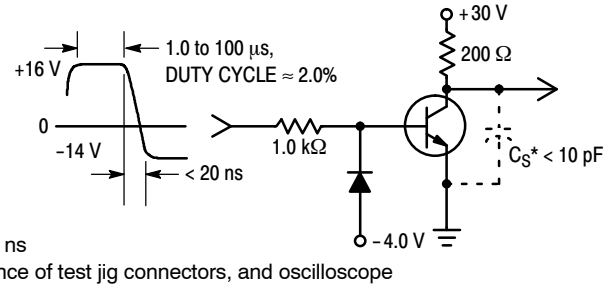


Figure 2. Turn-Off Time

TRANSIENT CHARACTERISTICS

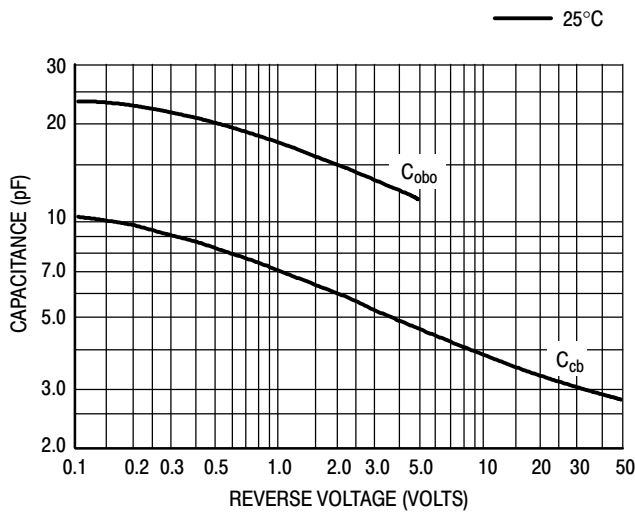


Figure 3. Capacitances

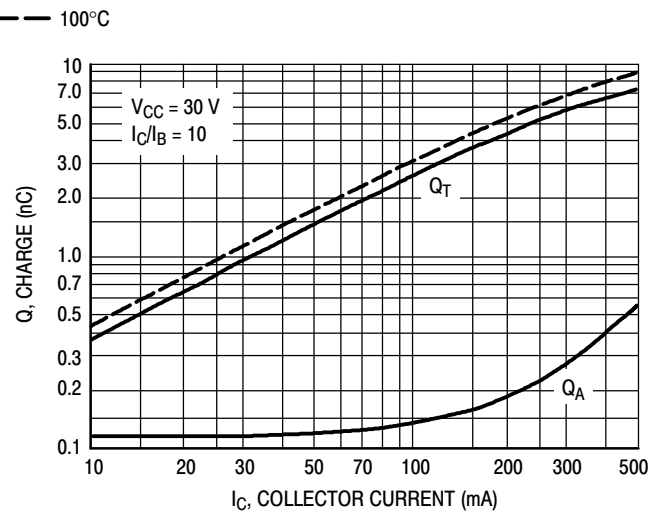


Figure 4. Charge Data

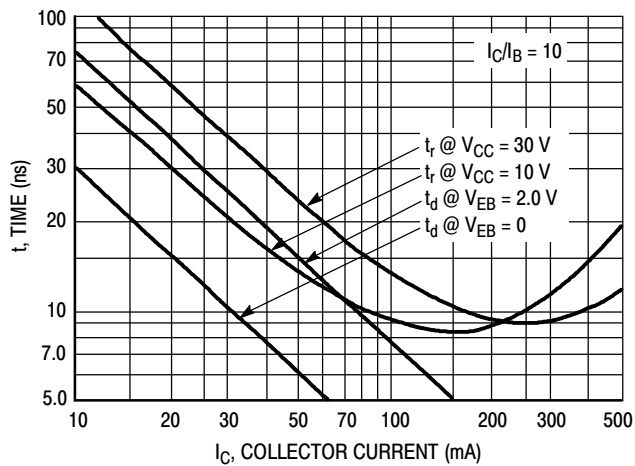


Figure 5. Turn-On Time

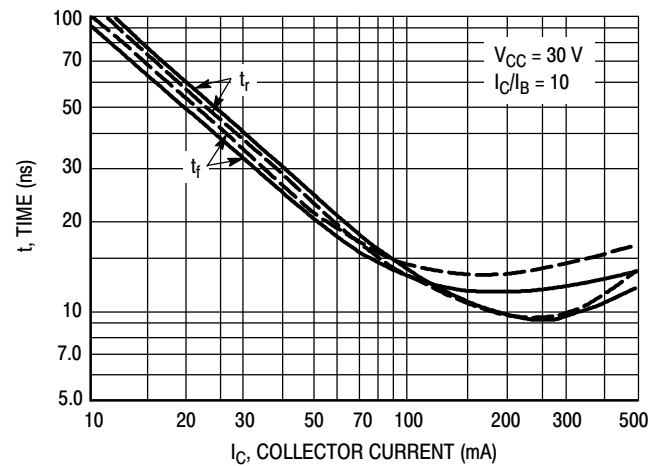
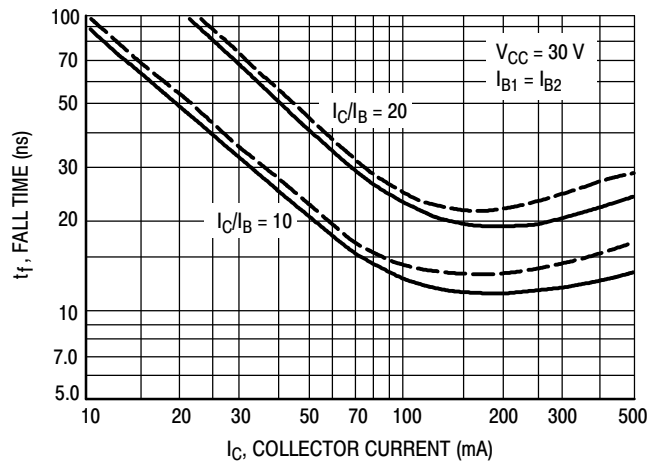
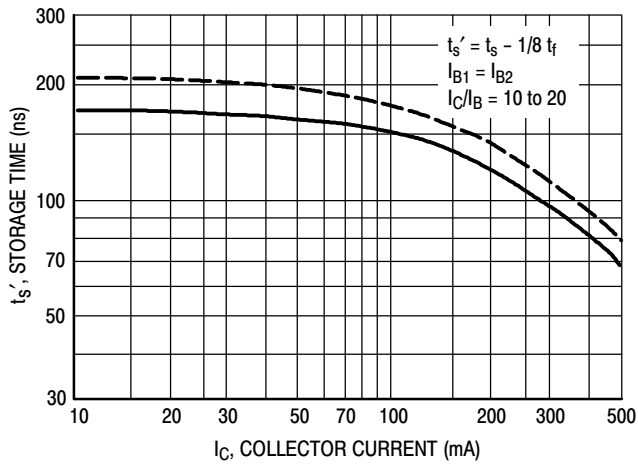
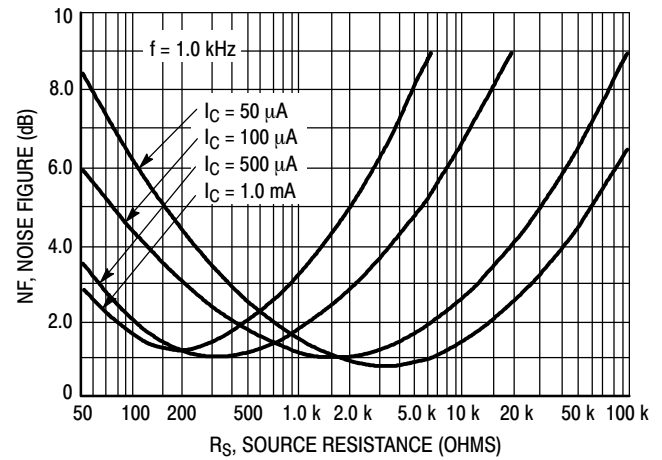
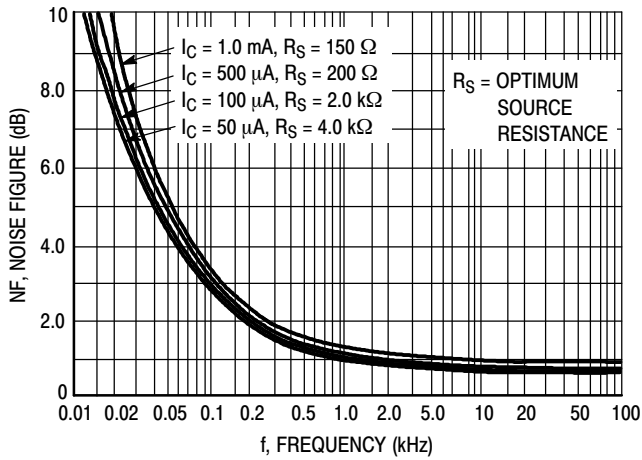


Figure 6. Rise and Fall Times



SMALL-SIGNAL CHARACTERISTICS NOISE FIGURE

$V_{CE} = 10 \text{ Vdc}$, $T_A = 25^\circ\text{C}$; Bandwidth = 1.0 Hz



2N4401

h PARAMETERS

$V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$, $T_A = 25^\circ\text{C}$

This group of graphs illustrates the relationship between h_{fe} and other “h” parameters for this series of transistors. To obtain these curves, a high-gain and a low-gain unit were

selected from the 2N4401 lines, and the same units were used to develop the correspondingly numbered curves on each graph.

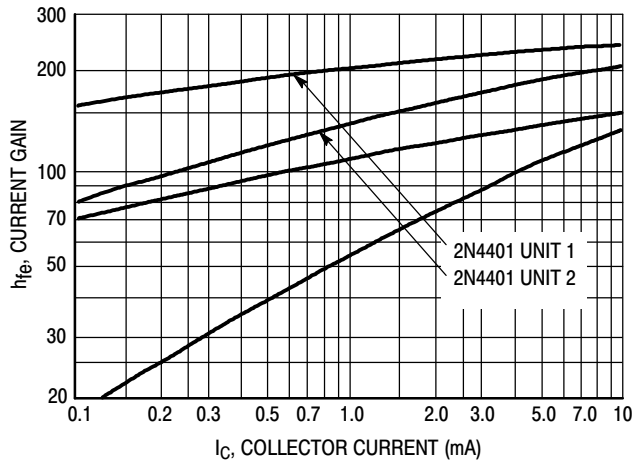


Figure 11. Current Gain

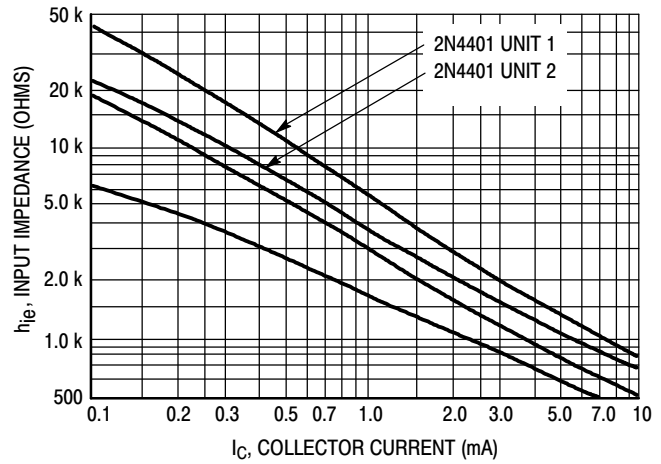


Figure 12. Input Impedance

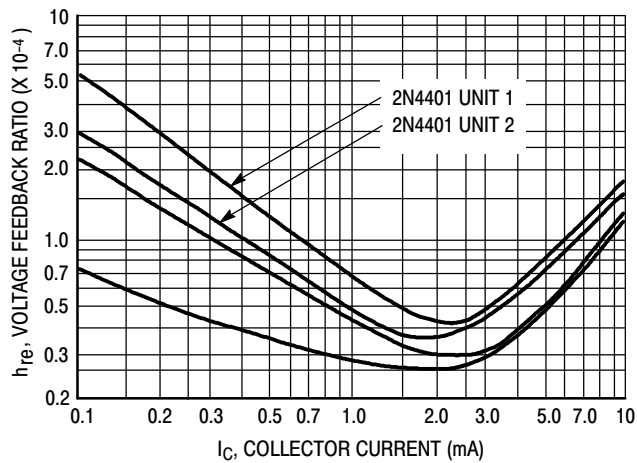


Figure 13. Voltage Feedback Ratio

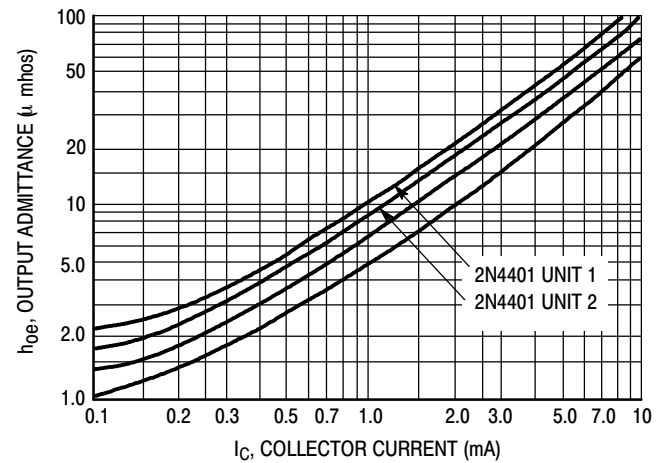


Figure 14. Output Admittance

STATIC CHARACTERISTICS

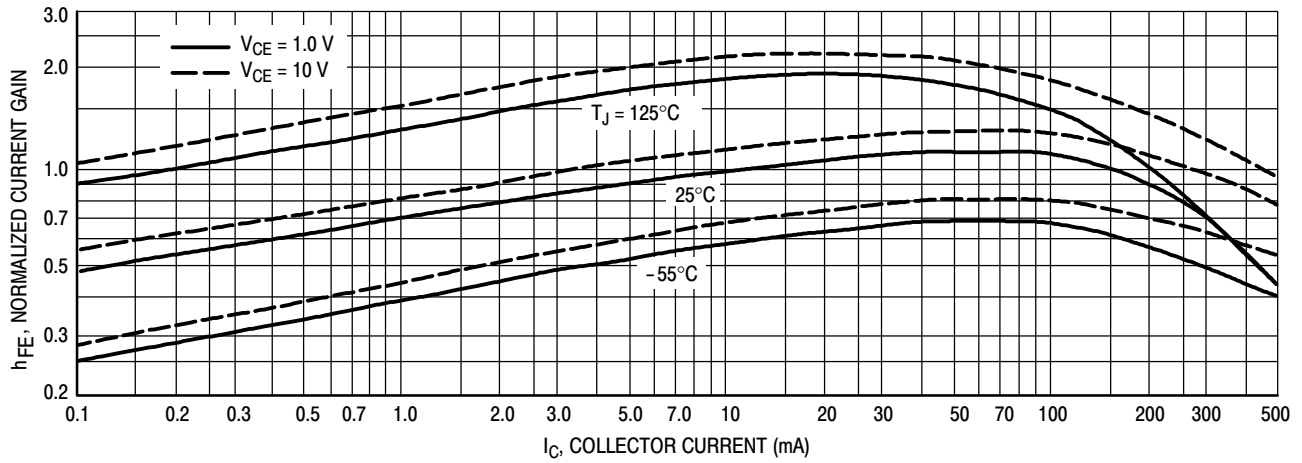


Figure 15. DC Current Gain

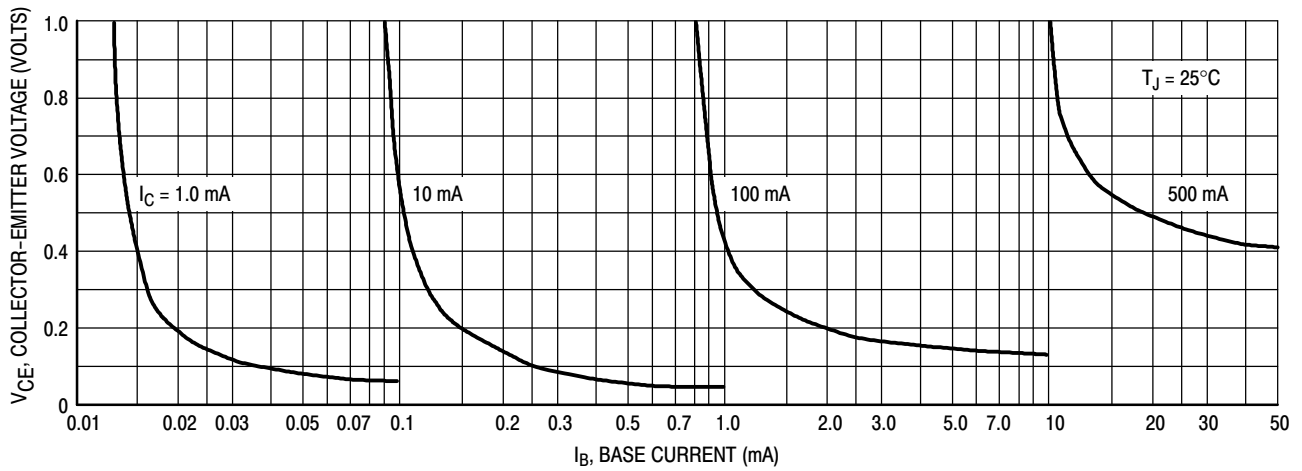


Figure 16. Collector Saturation Region

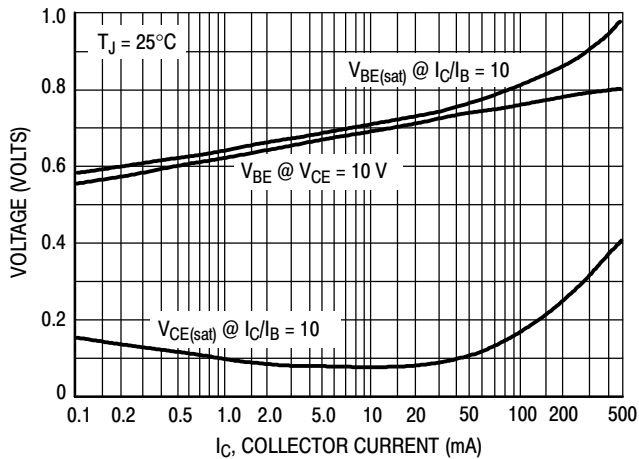


Figure 17. "On" Voltages

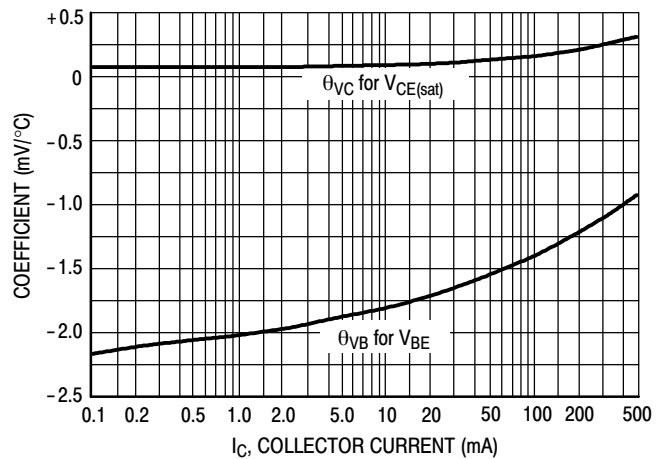


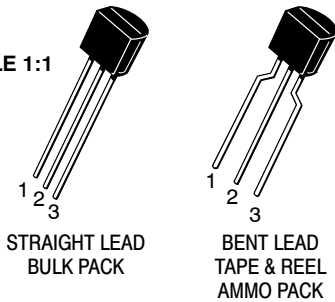
Figure 18. Temperature Coefficients

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

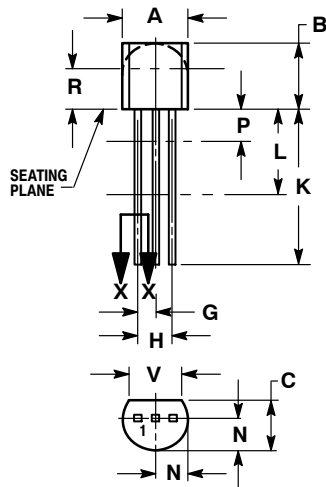
ON

SCALE 1:1

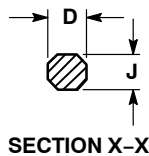


TO-92 (TO-226)
CASE 29-11
ISSUE AM

DATE 09 MAR 2007



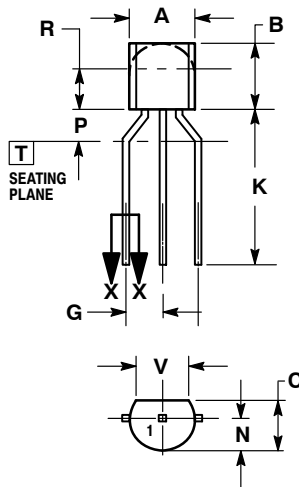
STRAIGHT LEAD
BULK PACK



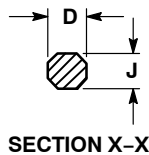
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD
TAPE & REEL
AMMO PACK



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS	
	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42022B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO-92 (TO-226)	
		PAGE 1 OF 3

TO-92 (TO-226)
CASE 29-11
ISSUE AM

DATE 09 MAR 2007

STYLE 1: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 2: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 3: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 5: PIN 1. DRAIN 2. SOURCE 3. GATE
STYLE 6: PIN 1. GATE 2. SOURCE & SUBSTRATE 3. DRAIN	STYLE 7: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 8: PIN 1. DRAIN 2. GATE 3. SOURCE & SUBSTRATE	STYLE 9: PIN 1. BASE 1 2. EMITTER 3. BASE 2	STYLE 10: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 11: PIN 1. ANODE 2. CATHODE & ANODE 3. CATHODE	STYLE 12: PIN 1. MAIN TERMINAL 1 2. GATE 3. MAIN TERMINAL 2	STYLE 13: PIN 1. ANODE 1 2. GATE 3. CATHODE 2	STYLE 14: PIN 1. EMITTER 2. COLLECTOR 3. BASE	STYLE 15: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2
STYLE 16: PIN 1. ANODE 2. GATE 3. CATHODE	STYLE 17: PIN 1. COLLECTOR 2. BASE 3. EMITTER	STYLE 18: PIN 1. ANODE 2. CATHODE 3. NOT CONNECTED	STYLE 19: PIN 1. GATE 2. ANODE 3. CATHODE	STYLE 20: PIN 1. NOT CONNECTED 2. CATHODE 3. ANODE
STYLE 21: PIN 1. COLLECTOR 2. EMITTER 3. BASE	STYLE 22: PIN 1. SOURCE 2. GATE 3. DRAIN	STYLE 23: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 24: PIN 1. EMITTER 2. COLLECTOR/ANODE 3. CATHODE	STYLE 25: PIN 1. MT 1 2. GATE 3. MT 2
STYLE 26: PIN 1. V_{CC} 2. GROUND 2 3. OUTPUT	STYLE 27: PIN 1. MT 2. SUBSTRATE 3. MT	STYLE 28: PIN 1. CATHODE 2. ANODE 3. GATE	STYLE 29: PIN 1. NOT CONNECTED 2. ANODE 3. CATHODE	STYLE 30: PIN 1. DRAIN 2. GATE 3. SOURCE
STYLE 31: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 32: PIN 1. BASE 2. COLLECTOR 3. EMITTER	STYLE 33: PIN 1. RETURN 2. INPUT 3. OUTPUT	STYLE 34: PIN 1. INPUT 2. GROUND 3. LOGIC	STYLE 35: PIN 1. GATE 2. COLLECTOR 3. EMITTER

DOCUMENT NUMBER:	98ASB42022B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO-92 (TO-226)	PAGE 2 OF 3

[illegible]

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales