# Dual 4-Input Data Selector/Multiplexer

## High−Performance Silicon−Gate CMOS

## MC74HC153A

The MC74HC153 is identical in pinout to the LS153. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The Address Inputs select one of four Data Inputs from each multiplexer. Each multiplexer has an active−low Strobe control and a noninverting output.

The HC153 is similar in function to the HC253, which has 3−state outputs.

### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 µA
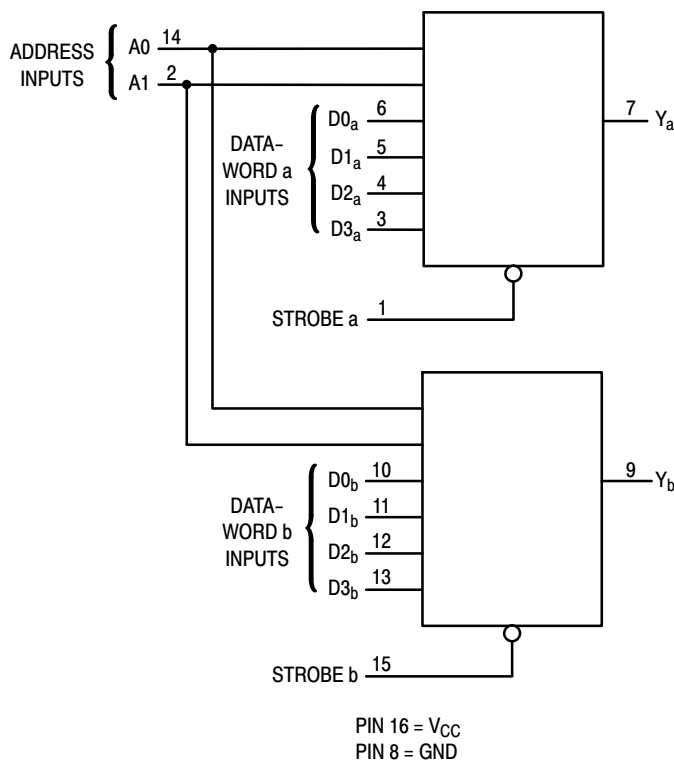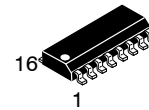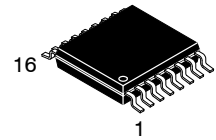- High Noise Immunity Characteristic of CMOS Devices
- These are Pb−Free Devices

**SOIC−16**
**D SUFFIX**
**CASE 751B**

**TSSOP−16**
**DT SUFFIX**
**CASE 948F**

**QFN16**
**MN SUFFIX**
**CASE 485AW**

### MARKING DIAGRAMS

```
XXXXXXX
AWLYWW
```

```
XX
XXXX
ALYW■
```

```
XXXX
ALYW■
```
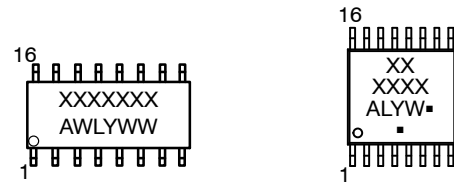
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| G or ■ | = Pb−Free Package |

(Note: Microdot may be in either location)

### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| STROBE a | 1 ● | 16 | $V_{CC}$ |
| A1 | 2 | 15 | STROBE b |
| $D3_a$ | 3 | 14 | A0 |
| $D2_a$ | 4 | 13 | $D3_b$ |
| $D1_a$ | 5 | 12 | $D2_b$ |
| $D0_a$ | 6 | 11 | $D1_b$ |
| $Y_a$ | 7 | 10 | $D0_b$ |
| GND | 8 | 9 | $Y_b$ |



**Figure 1. Logic Diagram**

PIN 16 = $V_{CC}$
PIN 8 = GND
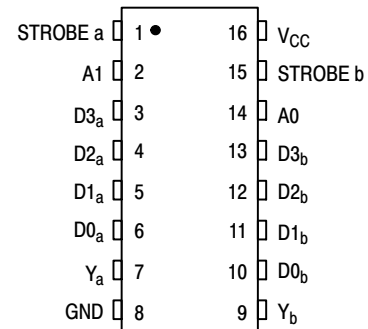
### FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| A1 | A0 | Strobe | Y |
| X | X | H | L |
| L | L | L | D0 |
| L | H | L | D1 |
| H | L | L | D2 |
| H | H | L | D3 |

D0, D1, D2, and D3 = the level of the respective data input.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# MC74HC153A

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +6.5 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to $V_{CC}$ + 0.5 | V |
| $V_{OUT}$ | DC Output Voltage | | −0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IN}$ | DC Input Current, per Pin | | ±20 | mA |
| $I_{OUT}$ | DC Output Current, per Pin | | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | | ±50 | mA |
| $I_{IK}$ | Input Clamp Current ($V_{IN}$ < 0 or $V_{IN}$ > $V_{CC}$) | | ±20 | mA |
| $I_{OK}$ | Output Clamp Current ($V_{OUT}$ < 0 or $V_{OUT}$ > $V_{CC}$) | | ±20 | mA |
| $T_{STG}$ | Storage Temperature | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | ±150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 1) | SOIC−16<br>QFN16<br>TSSOP−16 | 126<br>118<br>159 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 25°C | SOIC−16<br>QFN16<br>TSSOP−16 | 995<br>1062<br>787 | mW |
| MSL | Moisture Sensitivity | | Level 1 | − |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | − |
| $V_{ESD}$ | ESD Withstand Voltage (Note 2) | Human Body Model<br>Charged Device Model | >2000<br>N/A | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$ = 2.0 V<br>$V_{CC}$ = 4.5 V<br>$V_{CC}$ = 6.0 V | 0<br>0<br>0 | 1000<br>500<br>400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | − 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High−Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V $\|I_{out}\|$ ≤ 20 μA | 2.0 4.5 6.0 | 1.5 3.15 4.2 | 1.5 3.15 4.2 | 1.5 3.15 4.2 | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V $\|I_{out}\|$ ≤ 20 μA | 2.0 4.5 6.0 | 0.3 0.9 1.2 | 0.3 0.9 1.2 | 0.3 0.9 1.2 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\|$ ≤ 20 μA | 2.0 4.5 6.0 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$    $\|I_{out}\|$ ≤ 4.0 mA    $\|I_{out}\|$ ≤ 5.2 mA | 4.5 6.0 | 3.98 5.48 | 3.84 5.34 | 3.70 5.20 | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\|$ ≤ 20 μA | 2.0 4.5 6.0 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$    $\|I_{out}\|$ ≤ 4.0 mA    $\|I_{out}\|$ ≤ 5.2 mA | 4.5 6.0 | 0.26 0.26 | 0.33 0.33 | 0.40 0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND $I_{out}$ = 0 μA | 6.0 | 8 | 80 | 160 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
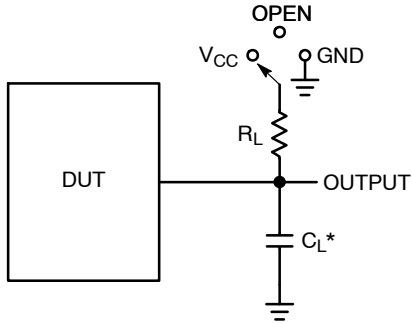
## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | − 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Input D to Output Y (Figures 2 and 3) | 2.0 4.5 6.0 | 140 28 24 | 175 35 30 | 210 42 36 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4) | 2.0 4.5 6.0 | 175 35 30 | 220 44 37 | 265 53 45 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Strobe to Output Y (Figures 2 and 5) | 2.0 4.5 6.0 | 95 19 16 | 120 24 20 | 145 29 25 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 2 and 3) | 2.0 4.5 6.0 | 75 15 13 | 95 19 16 | 110 22 19 | ns |
| $C_{in}$ | Maximum Input Capacitance | − | 10 | 10 | 10 | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Multiplexer) | 31 | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MC74HC153A

## SWITCHING WAVEFORMS



| Test | Switch Position | $C_L$ | $R_L$ |
|---|---|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open | 50 pF | 1 kΩ |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{CC}$ | | |
| $t_{PHZ}$ / $t_{PZH}$ | GND | | |

*$C_L$ Includes probe and jig capacitance

**Figure 2. Test Circuit**
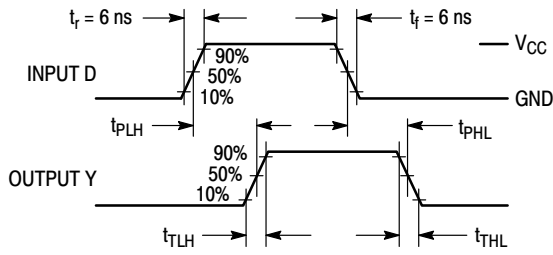


**Figure 3.**
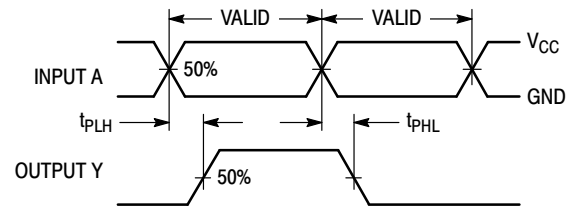


**Figure 4.**
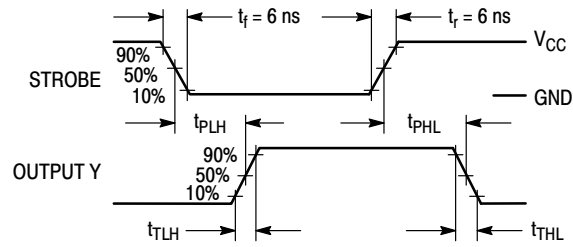


**Figure 5.**

# MC74HC153A

## PIN DESCRIPTIONS

**DATA INPUTS**

**$D0_a$ – $D3_a$, $D0_b$ – $D3_b$ (Pins 3, 4, 5, 6, 10, 11, 12, 13)**

  Data Inputs. With the outputs enabled, the addressed Data Inputs appear at the Y outputs.

**CONTROL INPUTS**

**A0, A1 (Pins 2, 14)**

  Address Inputs. These inputs address the pair of Data Inputs which appear at the corresponding outputs.

**Strobe (Pins 1, 15)**

  Active−low Strobe. A low level applied to these pins enables the corresponding outputs.

**OUTPUTS**

**$Y_a$, $Y_b$ (Pins 7, 9)**

  Noninverting data outputs.
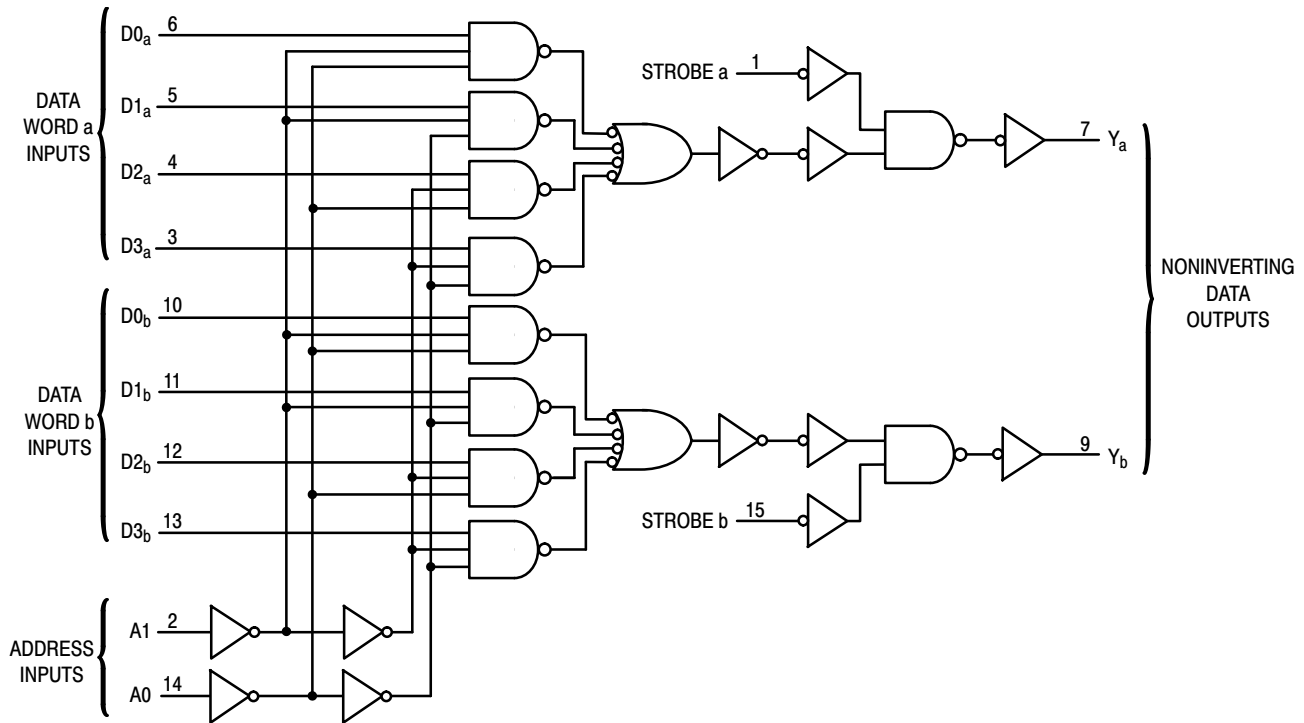


**Figure 6. Expanded Logic Diagram**

## ORDERING INFORMATION

| Device | Marking | Package | Shipping[†] |
|---|---|---|---|
| MC74HC153ADG | HC153AG | SOIC−16 | 48 Units / Rail |
| MC74HC153ADR2G | HC153AG | SOIC−16 | 2500 / Tape & Reel |
| MC74HC153ADTR2G | HC 153A | TSSOP−16 | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

# MC74HC153A

## PACKAGE DIMENSIONS

**QFN16, 2.5x3.5, 0.5P**
CASE 485AW
ISSUE O

**SCALE 2:1**

DATE 11 DEC 2008

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**PIN ONE REFERENCE**

2X △ 0.15 C

2X △ 0.15 C

**TOP VIEW**
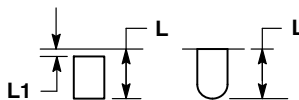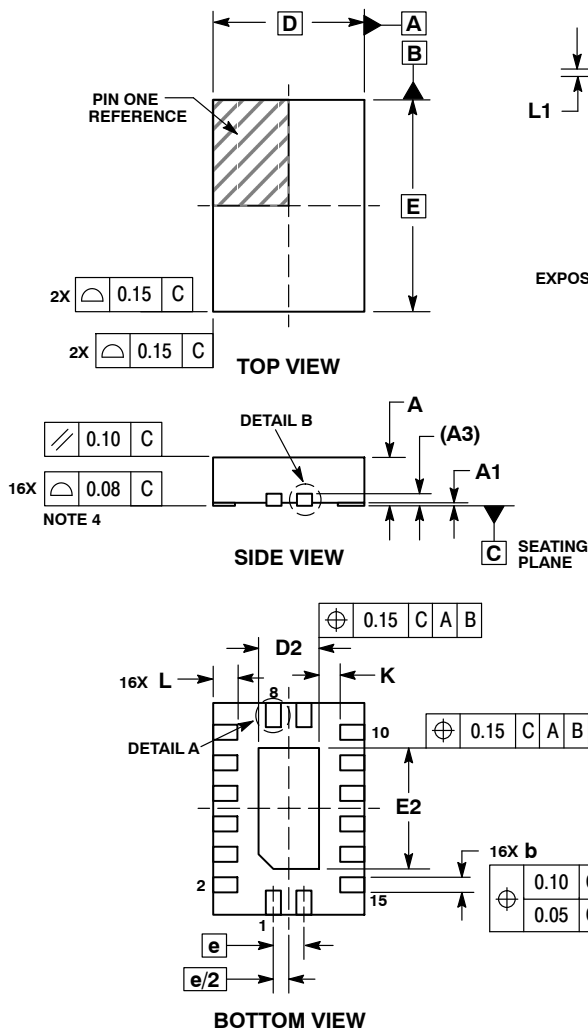
**DETAIL A**
ALTERNATE TERMINAL CONSTRUCTIONS

**EXPOSED Cu**    **MOLD CMPD**
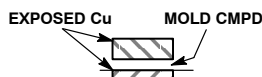
**DETAIL B**
ALTERNATE CONSTRUCTIONS

| DIM | MILLIMETERS | |
|-----|-----|-----|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.50 BSC | |
| D2 | 0.85 | 1.15 |
| E | 3.50 BSC | |
| E2 | 1.85 | 2.15 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.35 | 0.45 |
| L1 | --- | 0.15 |

0.10 C

16X △ 0.08 C
NOTE 4

**DETAIL B**

**SIDE VIEW**

**SEATING PLANE**

0.15 C A B

0.15 C A B

16X L

**DETAIL A**

0.10 C A B
0.05 C
NOTE 3

16X b

**BOTTOM VIEW**

### GENERIC MARKING DIAGRAM*
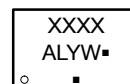
XXXX
ALYW▪

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

### RECOMMENDED SOLDERING FOOTPRINT*
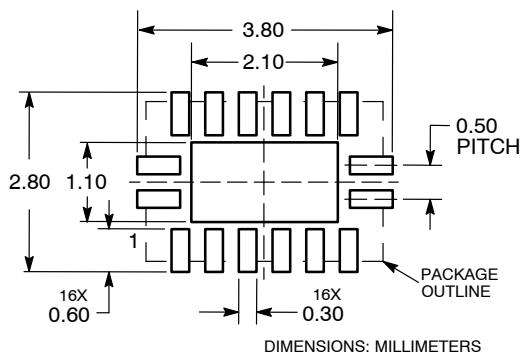
3.80

2.10

2.80    1.10

0.50 PITCH

PACKAGE OUTLINE

16X 0.60

16X 0.30

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**SOIC−16 9.90x3.90x1.50 1.27P**
**CASE 751B**
**ISSUE L**

**DATE 29 MAY 2024**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
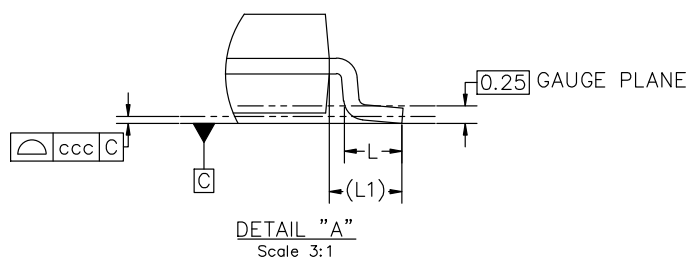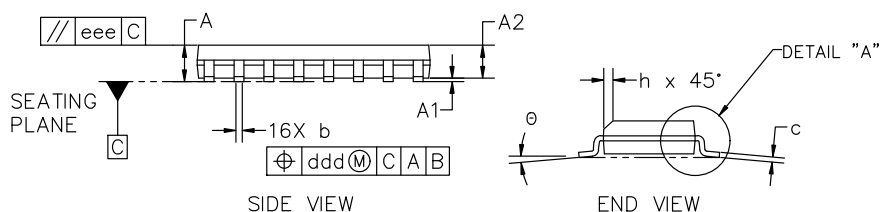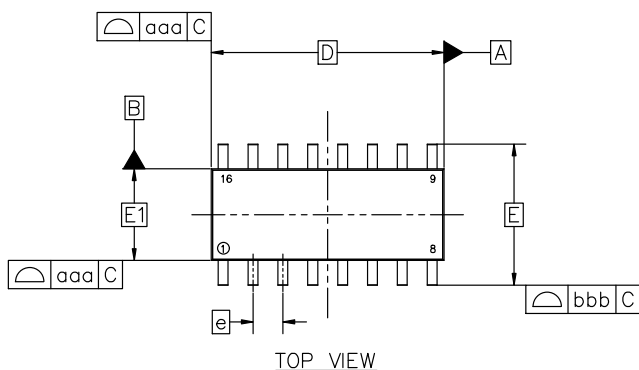
| DIM | MILLIMETERS | | |
|-----|-----|-----|-----|
| | MIN | NOM | MAX |
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 1.35 | 1.50 | 1.65 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.19 | 0.22 | 0.25 |
| D | 9.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| h | 0.25 | --- | 0.50 |
| L | 0.40 | 0.83 | 1.25 |
| L1 | 1.05 REF | | |
| Θ | 0° | --- | 7° |

| TOLERANCE OF FORM AND POSITION | |
|-----|-----|
| aaa | 0.10 |
| bbb | 0.20 |
| ccc | 0.10 |
| ddd | 0.25 |
| eee | 0.10 |

TOP VIEW

SIDE VIEW

END VIEW

DETAIL "A"
Scale 3:1

0.25 GAUGE PLANE
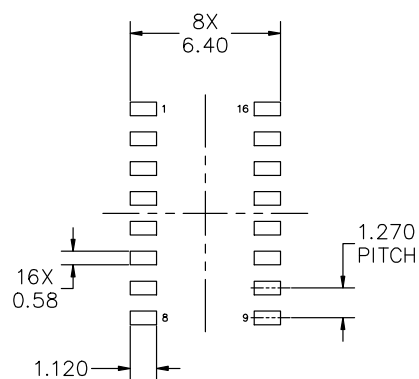
DETAIL "A"

RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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|-----|-----|-----|-----|
| **DESCRIPTION:** | **SOIC−16 9.90X3.90X1.50 1.27P** | | **PAGE 1 OF 2** |

**SOIC−16 9.90x3.90x1.50 1.27P**
CASE 751B
ISSUE L

DATE 29 MAY 2024

## GENERIC
## MARKING DIAGRAM*

```
16  ☐☐☐☐☐☐☐☐
   ┌──────────────┐
   │XXXXXXXXXXXXG │
   │XXXXXXXXXXXXX │
   │   AWLYWW     │
   └──────────────┘
1   ☐☐☐☐☐☐☐☐
```
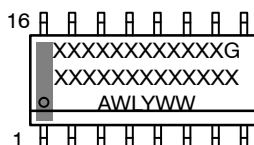
XXXXX = Specific Device Code
A     = Assembly Location
WL    = Wafer Lot
Y     = Year
WW    = Work Week
G     = Pb−Free Package

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot "▪", may
or may not be present. Some products may
not follow the Generic Marking.

| STYLE 1: | | STYLE 2: | | STYLE 3: | | STYLE 4: | |
|---|---|---|---|---|---|---|---|
| PIN 1. | COLLECTOR | PIN 1. | CATHODE | PIN 1. | COLLECTOR, DYE #1 | PIN 1. | COLLECTOR, DYE #1 |
| 2. | BASE | 2. | ANODE | 2. | BASE, #1 | 2. | COLLECTOR, #1 |
| 3. | EMITTER | 3. | NO CONNECTION | 3. | EMITTER, #1 | 3. | COLLECTOR, #2 |
| 4. | NO CONNECTION | 4. | CATHODE | 4. | COLLECTOR, #1 | 4. | COLLECTOR, #2 |
| 5. | EMITTER | 5. | CATHODE | 5. | COLLECTOR, #2 | 5. | COLLECTOR, #3 |
| 6. | BASE | 6. | NO CONNECTION | 6. | BASE, #2 | 6. | COLLECTOR, #3 |
| 7. | COLLECTOR | 7. | ANODE | 7. | EMITTER, #2 | 7. | COLLECTOR, #4 |
| 8. | COLLECTOR | 8. | CATHODE | 8. | COLLECTOR, #2 | 8. | COLLECTOR, #4 |
| 9. | BASE | 9. | CATHODE | 9. | COLLECTOR, #3 | 9. | BASE, #4 |
| 10. | EMITTER | 10. | ANODE | 10. | BASE, #3 | 10. | EMITTER, #4 |
| 11. | NO CONNECTION | 11. | NO CONNECTION | 11. | EMITTER, #3 | 11. | BASE, #3 |
| 12. | EMITTER | 12. | CATHODE | 12. | COLLECTOR, #3 | 12. | EMITTER, #3 |
| 13. | BASE | 13. | CATHODE | 13. | COLLECTOR, #4 | 13. | BASE, #2 |
| 14. | COLLECTOR | 14. | NO CONNECTION | 14. | BASE, #4 | 14. | EMITTER, #2 |
| 15. | EMITTER | 15. | ANODE | 15. | EMITTER, #4 | 15. | BASE, #1 |
| 16. | COLLECTOR | 16. | CATHODE | 16. | COLLECTOR, #4 | 16. | EMITTER, #1 |

| STYLE 5: | | STYLE 6: | | STYLE 7: | |
|---|---|---|---|---|---|
| PIN 1. | DRAIN, DYE #1 | PIN 1. | CATHODE | PIN 1. | SOURCE N-CH |
| 2. | DRAIN, #1 | 2. | CATHODE | 2. | COMMON DRAIN (OUTPUT) |
| 3. | DRAIN, #2 | 3. | CATHODE | 3. | COMMON DRAIN (OUTPUT) |
| 4. | DRAIN, #2 | 4. | CATHODE | 4. | GATE P-CH |
| 5. | DRAIN, #3 | 5. | CATHODE | 5. | COMMON DRAIN (OUTPUT) |
| 6. | DRAIN, #3 | 6. | CATHODE | 6. | COMMON DRAIN (OUTPUT) |
| 7. | DRAIN, #4 | 7. | CATHODE | 7. | COMMON DRAIN (OUTPUT) |
| 8. | DRAIN, #4 | 8. | CATHODE | 8. | SOURCE P-CH |
| 9. | GATE, #4 | 9. | ANODE | 9. | SOURCE P-CH |
| 10. | SOURCE, #4 | 10. | ANODE | 10. | COMMON DRAIN (OUTPUT) |
| 11. | GATE, #3 | 11. | ANODE | 11. | COMMON DRAIN (OUTPUT) |
| 12. | SOURCE, #3 | 12. | ANODE | 12. | COMMON DRAIN (OUTPUT) |
| 13. | GATE, #2 | 13. | ANODE | 13. | GATE N-CH |
| 14. | SOURCE, #2 | 14. | ANODE | 14. | COMMON DRAIN (OUTPUT) |
| 15. | GATE, #1 | 15. | ANODE | 15. | COMMON DRAIN (OUTPUT) |
| 16. | SOURCE, #1 | 16. | ANODE | 16. | SOURCE N-CH |

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|---|---|---|---|
| DESCRIPTION: | SOIC−16 9.90X3.90X1.50 1.27P | | PAGE 2 OF 2 |

**TSSOP−16 WB**
CASE 948F
ISSUE B

DATE 19 OCT 2006

16

1

**SCALE 2:1**

16X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T U Ⓢ V Ⓢ

⌓ | 0.15 (0.006) | T U Ⓢ

**2X L/2**

**L**

16    9

**PIN 1
IDENT.**

1    8

**B**
**−U−**

⌓ | 0.15 (0.006) | T U Ⓢ

**A**
**−V−**

**K**
**K1**

**J1**

**SECTION N−N**

**J**

N

| 0.25 (0.010) |

**M**

N

**F**

**DETAIL E**

**C**

⌓ | 0.10 (0.004)

**−T−** SEATING
PLANE

**D**    **G**    **H**

**DETAIL E**

**−W−**
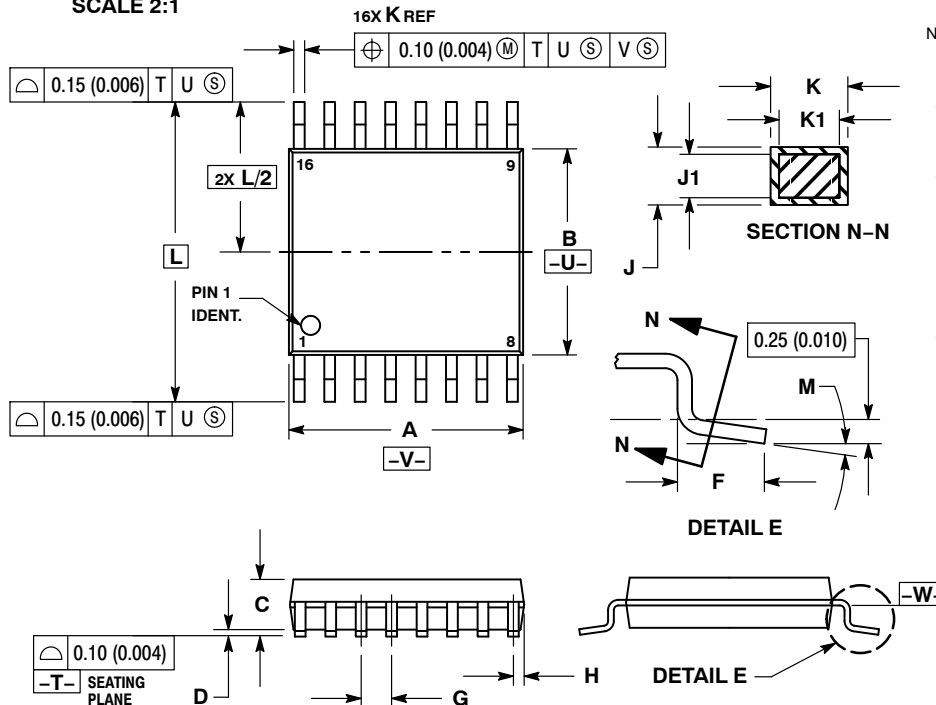
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

**RECOMMENDED
SOLDERING FOOTPRINT\***
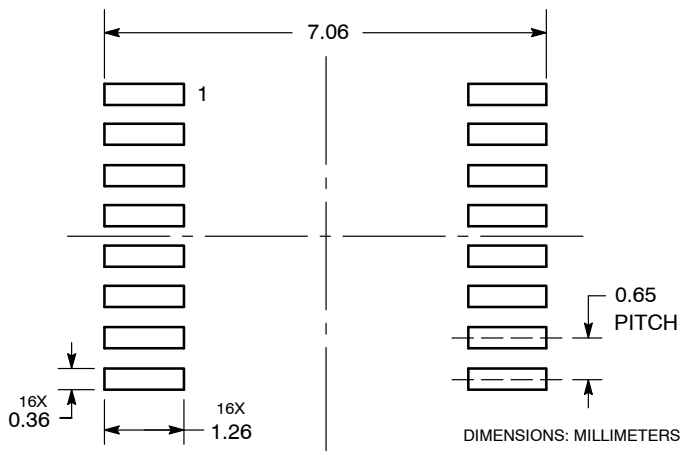
7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

**GENERIC
MARKING DIAGRAM\***

16

XXXX
XXXX
◦ ALYW

1
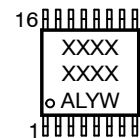
XXXX  = Specific Device Code
A      = Assembly Location
L      = Wafer Lot
Y      = Year
W      = Work Week
G or ▪ = Pb−Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪ ", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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|---|---|---|---|
| **DESCRIPTION:** | **TSSOP−16** | | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical–documentation
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