Quad 2-Input Multiplexer

MC74AC157, MC74ACT157

The MC74AC157/74ACT157 is a high−speed quad 2−input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (non−inverted) form.

The MC74AC157/74ACT157 can also be used as a function generator.

Features

- Outputs Source/Sink 24 mA
- ′ACT157 Has TTL Compatible Inputs
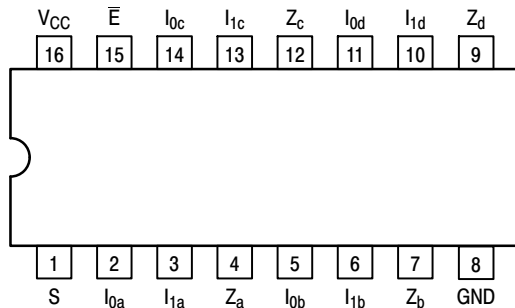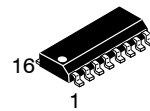- These are Pb−Free Devices

MARKING DIAGRAMS

SOIC−16
D SUFFIX
CASE 751B

```
16
XXXXXXG
AWLYWW
1
```
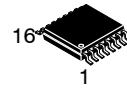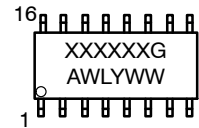
TSSOP−16
DT SUFFIX
CASE 948F

```
16
XXX
XXX
ALYW▪
1
```
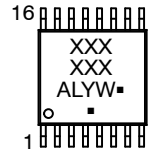
XXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

V_{CC}	$\overline{E}$	I_{0c}	I_{1c}	Z_c	I_{0d}	I_{1d}	Z_d
16	15	14	13	12	11	10	9

1	2	3	4	5	6	7	8
S	I_{0a}	I_{1a}	Z_a	I_{0b}	I_{1b}	Z_b	GND

Figure 1. Pinout: 16−Lead Packages Conductors
(Top View)

PIN NAMES

PIN	FUNCTION
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 0 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_a–Z_d	Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

TRUTH TABLE

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

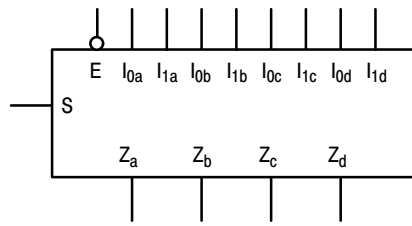# MC74AC157, MC74ACT157

Figure 2. Logic Symbol

FUNCTIONAL DESCRIPTION

The MC74AC157/74ACT157 is a quad 2−input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active−LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The MC74AC157/74ACT157 is the logic implementation of a 4−pole, 2−position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of the MC74AC157/74ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The MC74AC157/74ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.
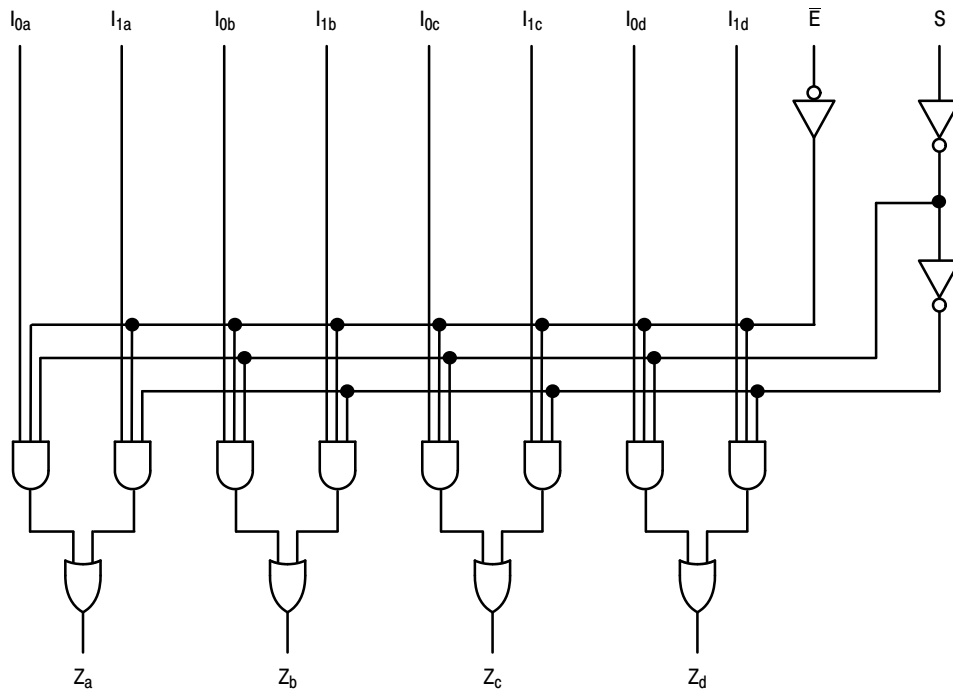
NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		-0.5 to $+6.5$	V
V_I	DC Input Voltage		$-0.5 \leq V_I \leq V_{CC} + 0.5$	V
V_O	DC Output Voltage	(Note 1)	$-0.5 \leq V_O \leq V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current		± 20	mA
I_{OK}	DC Output Diode Current		± 50	mA
I_O	DC Output Sink/Source Current		± 50	mA
I_{CC}	DC Supply Current per Output Pin		± 50	mA
I_{GND}	DC Ground Current per Output Pin		± 50	mA
T_{STG}	Storage Temperature Range		-65 to $+150$	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction temperature under Bias		$+150$	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC TSSOP	126 159	°C/W
P_D	Power Dissipation in Still Air at 25°C (Note 3)	SOIC TSSOP	995 787	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35%	UL 94 V–0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 4) Charged Device Model (Note 5)	> 2000 > 1000	V
$I_{Latch-Up}$	Latch–Up Performance Above V_{CC} and Below GND at 85°C (Note 6)		± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51–7.
3. 500 mW at 65°C; derate to 300 mW by 10 mW/ from 65°C to 85°C.
4. Tested to EIA/JESD22–A114–A.
5. Tested to JESD22–C101–A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)		0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	–	150	–	ns/V
		V_{CC} @ 4.5 V	–	40	–	
		V_{CC} @ 5.5 V	–	25	–	
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	–	10	–	ns/V
		V_{CC} @ 5.5 V	–	8.0	–	
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current – High		–	–	–24	mA
I_{OL}	Output Current – Low		–	–	24	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	74AC $T_A = -40°C$ to $+85°C$	Unit	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	$I_{OUT} = -50$ μA
		3.0 4.5 5.5	– – –	2.56 3.86 4.86	2.46 3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} -12 mA I_{OH} -24 mA -24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	$I_{OUT} = 50$ μA
		3.0 4.5 5.5	– – –	0.36 0.36 0.36	0.44 0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} 12 mA I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	$V_{OLD} = 1.65$ V Max
I_{OHD}		5.5	–	–	–75	mA	$V_{OHD} = 3.85$ V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF Min	74AC $T_A = +25°C$ $C_L = 50$ pF Typ	74AC $T_A = +25°C$ $C_L = 50$ pF Max	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Min	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Max	Unit
t_{PLH}	Propagation Delay S to Z_n	3.3 5.0	1.5 1.5	7.0 5.5	11.5 9.0	1.5 1.5	13.0 10.0	ns
t_{PHL}	Propagation Delay S to Z_n	3.3 5.0	1.5 1.5	6.5 5.0	11.0 8.5	1.5 1.0	12.0 9.5	ns
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	3.3 5.0	1.5 1.5	7.0 5.5	11.5 9.0	1.5 1.5	13.0 10.0	ns
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	3.3 5.0	1.5 1.5	6.5 5.5	11.0 9.0	1.5 1.0	12 9.5	ns
t_{PLH}	Propagation Delay I_n to Z_n	3.3 5.0	1.5 1.5	5.0 4.0	8.5 6.5	1.0 1.0	9.0 7.0	ns
t_{PHL}	Propagation Delay I_n to Z_n	3.3 5.0	1.5 1.5	5.0 4.0	8.0 6.5	1.0 1.0	9.0 7.0	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V$_{CC}$ (V)	74ACT T$_A$ = +25°C	74ACT T$_A$ = −40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits		
V$_{IH}$	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V$_{OUT}$ = 0.1 V or V$_{CC}$ − 0.1 V
V$_{IL}$	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V$_{OUT}$ = 0.1 V or V$_{CC}$ − 0.1 V
V$_{OH}$	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I$_{OUT}$ = −50 μA
		4.5 5.5	− −	3.86 4.86	3.76 4.76	V	*V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{OH}$ −24 mA −24 mA
V$_{OL}$	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I$_{OUT}$ = 50 μA
		4.5 5.5	− −	0.36 0.36	0.44 0.44	V	*V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{OL}$ 24 mA 24 mA
I$_{IN}$	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	μA	V$_I$ = V$_{CC}$, GND
ΔI$_{CCT}$	Additional Max. I$_{CC}$/Input	5.5	0.6	−	1.5	mA	V$_I$ = V$_{CC}$ − 2.1 V
I$_{OLD}$	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V$_{OLD}$ = 1.65 V Max
I$_{OHD}$		5.5	−	−	−75	mA	V$_{OHD}$ = 3.85 V Min
I$_{CC}$	Maximum Quiescent Supply Current	5.5	−	8.0	80	μA	V$_{IN}$ = V$_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS

Symbol	Parameter	V$_{CC}$* (V)	74ACT T$_A$ = +25°C C$_L$ = 50 pF			74ACT T$_A$ = −40°C to +85°C C$_L$ = 50 pF		Unit
			Min	Typ	Max	Min	Max	
t$_{PLH}$	Propagation Delay S to Z$_n$	5.0	2.0	−	9.0	1.5	10.0	ns
t$_{PHL}$	Propagation Delay S to Z$_n$	5.0	2.0	−	9.5	2.0	10.5	ns
t$_{PLH}$	Propagation Delay $\overline{E}_n$ to Z$_n$	5.0	1.5	−	10	1.5	11.5	ns
t$_{PHL}$	Propagation Delay $\overline{E}_n$ to Z$_n$	5.0	1.5	−	8.5	1.0	9.0	ns
t$_{PLH}$	Propagation Delay I$_n$ to Z$_n$	5.0	1.5	−	7.0	1.0	8.5	ns
t$_{PHL}$	Propagation Delay I$_n$ to Z$_n$	5.0	1.5	−	7.5	1.0	8.5	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value – Typ	Unit	Test Conditions
C$_{IN}$	Input Capacitance	4.5	pF	V$_{CC}$ = 5.0 V
C$_{PD}$	Power Dissipation Capacitance	50	pF	V$_{CC}$ = 5.0 V

ORDERING INFORMATION

Device Order Number	Marking	Package	Shipping†
MC74AC157DG	AC157	SOIC–16 (Pb–Free)	48 Units / Rail
MC74AC157DR2G	AC157	SOIC–16 (Pb–Free)	2500 Tape & Reel
MC74AC157DR2G–Q*	AC157	SOIC–16 (Pb–Free)	2500 Tape & Reel
MC74AC157DTR2G	AC 157	TSSOP–16 (Pb–Free)	2500 Tape & Reel
MC74ACT157DG	ACT157	SOIC–16 (Pb–Free)	48 Units / Rail
MC74ACT157DR2G	ACT157	SOIC–16 (Pb–Free)	2500 Tape & Reel
MC74ACT157DTR2G	ACT 157	TSSOP–16 (Pb–Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*–Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.
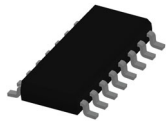
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
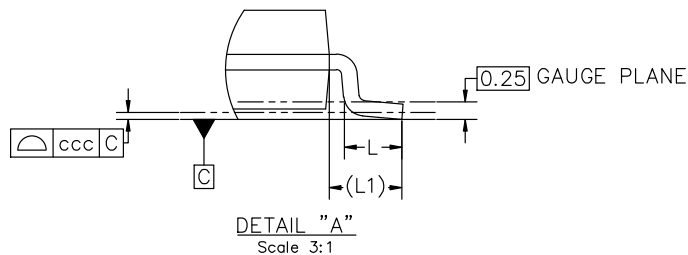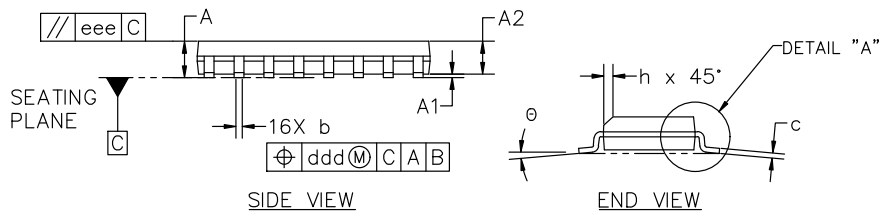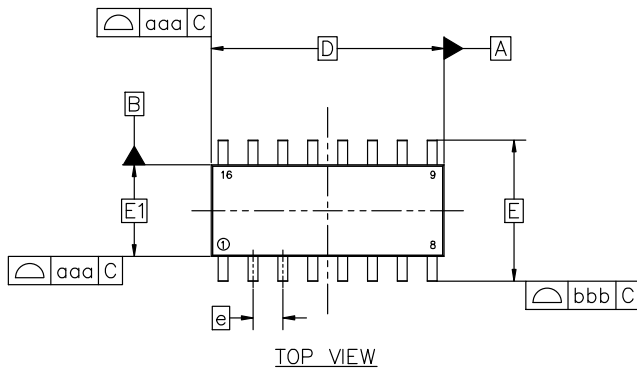
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	———	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	———	7°

TOLERANCE OF FORM AND POSITION	
aaa	0.10
bbb	0.20
ccc	0.10
ddd	0.25
eee	0.10

TOP VIEW

SIDE VIEW

END VIEW

DETAIL "A"
Scale 3:1

0.25 GAUGE PLANE

RECOMMENDED MOUNTING FOOTPRINT

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DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P		PAGE 1 OF 2

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*
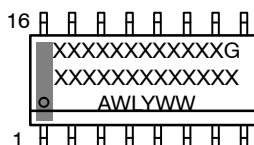
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:
PIN 1. COLLECTOR	PIN 1. CATHODE	PIN 1. COLLECTOR, DYE #1	PIN 1. COLLECTOR, DYE #1
2. BASE	2. ANODE	2. BASE, #1	2. COLLECTOR, #1
3. EMITTER	3. NO CONNECTION	3. EMITTER, #1	3. COLLECTOR, #2
4. NO CONNECTION	4. CATHODE	4. COLLECTOR, #1	4. COLLECTOR, #2
5. EMITTER	5. CATHODE	5. COLLECTOR, #2	5. COLLECTOR, #3
6. BASE	6. NO CONNECTION	6. BASE, #2	6. COLLECTOR, #3
7. COLLECTOR	7. ANODE	7. EMITTER, #2	7. COLLECTOR, #4
8. COLLECTOR	8. CATHODE	8. COLLECTOR, #2	8. COLLECTOR, #4
9. BASE	9. CATHODE	9. COLLECTOR, #3	9. BASE, #4
10. EMITTER	10. ANODE	10. BASE, #3	10. EMITTER, #4
11. NO CONNECTION	11. NO CONNECTION	11. EMITTER, #3	11. BASE, #3
12. EMITTER	12. CATHODE	12. COLLECTOR, #3	12. EMITTER, #3
13. BASE	13. CATHODE	13. COLLECTOR, #4	13. BASE, #2
14. COLLECTOR	14. NO CONNECTION	14. BASE, #4	14. EMITTER, #2
15. EMITTER	15. ANODE	15. EMITTER, #4	15. BASE, #1
16. COLLECTOR	16. CATHODE	16. COLLECTOR, #4	16. EMITTER, #1

STYLE 5:	STYLE 6:	STYLE 7:
PIN 1. DRAIN, DYE #1	PIN 1. CATHODE	PIN 1. SOURCE N-CH
2. DRAIN, #1	2. CATHODE	2. COMMON DRAIN (OUTPUT)
3. DRAIN, #2	3. CATHODE	3. COMMON DRAIN (OUTPUT)
4. DRAIN, #2	4. CATHODE	4. GATE P-CH
5. DRAIN, #3	5. CATHODE	5. COMMON DRAIN (OUTPUT)
6. DRAIN, #3	6. CATHODE	6. COMMON DRAIN (OUTPUT)
7. DRAIN, #4	7. CATHODE	7. COMMON DRAIN (OUTPUT)
8. DRAIN, #4	8. CATHODE	8. SOURCE P-CH
9. GATE, #4	9. ANODE	9. SOURCE P-CH
10. SOURCE, #4	10. ANODE	10. COMMON DRAIN (OUTPUT)
11. GATE, #3	11. ANODE	11. COMMON DRAIN (OUTPUT)
12. SOURCE, #3	12. ANODE	12. COMMON DRAIN (OUTPUT)
13. GATE, #2	13. ANODE	13. GATE N-CH
14. SOURCE, #2	14. ANODE	14. COMMON DRAIN (OUTPUT)
15. GATE, #1	15. ANODE	15. COMMON DRAIN (OUTPUT)
16. SOURCE, #1	16. ANODE	16. SOURCE N-CH

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DESCRIPTION:	**SOIC−16 9.90X3.90X1.50 1.27P**		**PAGE 2 OF 2**

onsemi™

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

16

SCALE 2:1

1

16X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

⌓ | 0.15 (0.006) | T | U Ⓢ

2X **L/2**

L

16   9

B
−U−

PIN 1
IDENT.

1   8

⌓ | 0.15 (0.006) | T | U Ⓢ

A
−V−

K
K1

J1

SECTION N−N

N

0.25 (0.010)

M

N

F

DETAIL E

C

⌓ | 0.10 (0.004)
−T− SEATING PLANE

D   **G**   **H**

DETAIL E

−W−

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	―――	1.20	―――	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

**RECOMMENDED
SOLDERING FOOTPRINT***

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

**GENERIC
MARKING DIAGRAM***

16

XXXX
XXXX
o ALYW

1
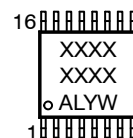
XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**TSSOP−16**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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