

# 3.3 V USB 3.1 Gen-2 10 Gbps Dual Channel / Single Port Linear Redriver

## NB7NPQ1102M

### Description

The NB7NPQ1102M is a high performance single-Port linear redriver designed for USB 3.1 Gen 1 and USB 3.1 Gen 2 applications that supports both 5 Gbps and 10 Gbps data rates. Signal integrity degrades from PCB traces, transmission cables, and inter-symbol interference (ISI). The NB7NPQ1102M compensates for these losses by engaging varying levels of equalization at the input receiver, and flat gain amplification on the output transmitter.

The NB7NPQ1102M offers programmable equalization and flat gain to optimize performance over various physical mediums.

The NB7NPQ1102M contains an automatic receiver detect function which will determine whether the output is active. The receiver detection loop will be active if the corresponding channel's signal detector is idle for a period of time. The channel will then move to Unplug Mode if a load is not detected, or it will return to Low Power Mode (Slumber mode) due to inactivity. Both the channels are independent with individual controls.

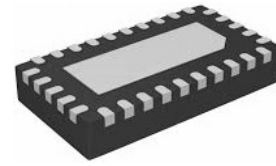
The NB7NPQ1102M comes in a 2.5 x 4.5 mm WQFN30 package and is specified to operate across the entire industrial temperature range, -40°C to 85°C.

### Features

- 3.3 V  $\pm$  0.3 V Power Supply
- 5 Gbps & 10 Gbps Serial Link with Linear Amplifier
- Device Supports USB 3.1 Gen 1 and USB 3.1 Gen 2 Data Rates
- USB 3.1 Super Speed Gen1 & Gen2 Standard Compliant
- Automatic Receiver Detection
- Integrated Input and Output Termination
- Pin Adjustable Receiver Equalization and Flat Gain
- Pin Adjustable Output Linear Swing
- 100  $\Omega$  Differential CML I/O's
- Auto Slumber Mode for Adaptive Power Management
- Hot-Plug Capable
- ESD Protection  $\pm$ 4 kV HBM
- Operating Temperature Range Industrial: -40°C to +85°C
- Package: WQFN30, 2.5 x 4.5 mm
- This is a Pb-Free Device

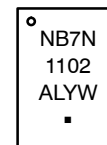
### Typical Applications

- USB3.1 Type-A and Type-C Signal Routing
- Mobile Phone and Tablet
- Computer, Laptop and Notebook
- External Storage Device
- Docking Station and Dongle
- Active Cable, Back Planes
- Gaming Console, Smart T.V



WQFN30  
CASE 510CK

### MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

### ORDERING INFORMATION

| Device           | Package             | Shipping <sup>†</sup> |
|------------------|---------------------|-----------------------|
| NB7NPQ1102MMTTWG | WQFN30<br>(Pb-Free) | 3000 / Tape<br>& Reel |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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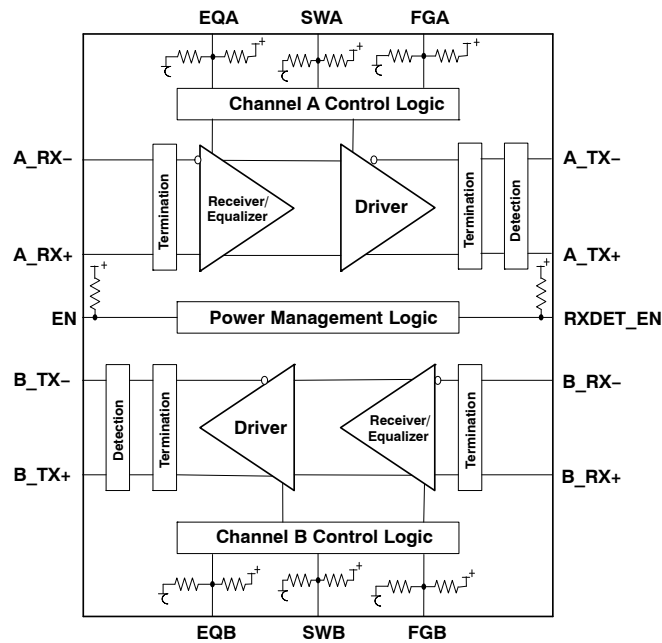


Figure 1. Logic Diagram of NB7NPQ1102M

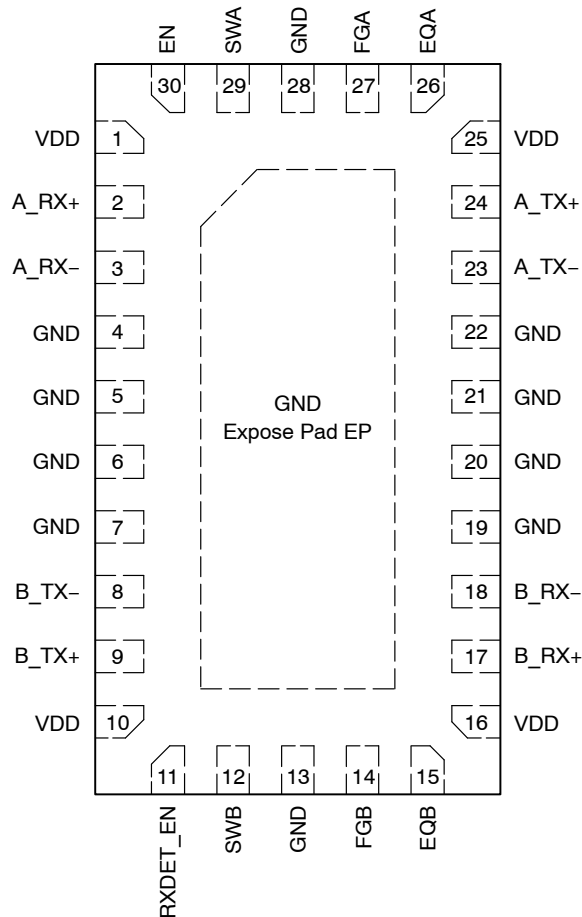


Figure 2. WQFN30 Package Pinout (Top View)

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**Table 1. PIN DESCRIPTION**

| Pin Number             | Pin Name | Type   | Description                                                                                                                                                                                                                                                                                                                                                                                          |
|------------------------|----------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 10, 16, 25          | VDD      | POWER  | 3.3 V power supply. V <sub>DD</sub> pins must be externally connected to power supply.                                                                                                                                                                                                                                                                                                               |
| 2                      | A_RX+    | INPUT  | Channel A Differential CML input pair for 5 / 10 Gbps USB signals with selectable input termination between 50 Ω to V <sub>DD</sub> or 67 kΩ to GND. Must be externally AC-coupled in system. UFP/DFP transmitter should provide this capacitor.                                                                                                                                                     |
| 3                      | A_RX-    |        |                                                                                                                                                                                                                                                                                                                                                                                                      |
| 4 – 7, 13, 19 – 22, 28 | GND      | GND    | Supply Ground. All GND pins must be externally connected to Ground.                                                                                                                                                                                                                                                                                                                                  |
| 8                      | B_TX-    | OUTPUT | Channel B Differential output for 5 / 10 Gbps USB signals. Must be externally AC-coupled in system.                                                                                                                                                                                                                                                                                                  |
| 9                      | B_TX+    |        |                                                                                                                                                                                                                                                                                                                                                                                                      |
| 11                     | RXDET_EN | INPUT  | Receiver detection enable pin. High – receiver detection is enabled, Low – receiver detection is disabled. Internal pull-up; default is High when open. The RXDET_EN pin must be powered simultaneously with V <sub>DD</sub> . After device power up, toggle the RXDET_EN pin from High-to-Low to disable RX DETECT function.                                                                        |
| 12                     | SWB      | INPUT  | Pin for control of Channel B Swing levels having an internal 100 kΩ pull up and 200 kΩ pull-down resistors. 4 state input: HIGH “H” where pin is connected to V <sub>DD</sub> , LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor Rext 68 kΩ is connected from pin to Ground. FLOAT “F” is the default setting.      |
| 14                     | FGB      | INPUT  | Pin for control of Channel B Flat Gain setting having internal 100 kΩ pull up and 200 kΩ pull-down resistors. 4 state input: HIGH “H” where pin is connected to V <sub>DD</sub> , LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor Rext 68 kΩ is connected from pin to Ground. FLOAT “F” is the default setting.    |
| 15                     | EQB      | INPUT  | Pin for control of Channel B Equalization setting having internal 100 kΩ pull up and 200 kΩ pull-down resistors. 4 state input: HIGH “H” where pin is connected to V <sub>DD</sub> , LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor Rext 68 kΩ is connected from pin to Ground. FLOAT “F” is the default setting. |
| 17                     | B_RX+    | INPUT  | Channel B Differential CML input pair for 5 / 10 Gbps USB signals with selectable input termination between 50 Ω to V <sub>DD</sub> or 67 kΩ to GND. Must be externally AC-coupled in system. UFP/DFP transmitter should provide this capacitor.                                                                                                                                                     |
| 18                     | B_RX-    |        |                                                                                                                                                                                                                                                                                                                                                                                                      |
| 23                     | A_TX-    | OUTPUT | Channel A Differential output for 5 / 10 Gbps USB signals. Must be externally AC-coupled in system.                                                                                                                                                                                                                                                                                                  |
| 24                     | A_TX+    |        |                                                                                                                                                                                                                                                                                                                                                                                                      |
| 26                     | EQA      | INPUT  | Pin for control of Channel A Equalization setting having internal 100 kΩ pull up and 200 kΩ pull-down resistors. 4 state input: HIGH “H” where pin is connected to V <sub>DD</sub> , LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor Rext 68 kΩ is connected from pin to Ground. FLOAT “F” is the default setting. |
| 27                     | FGA      | INPUT  | Pin for control of Channel A Flat Gain setting having internal 100 kΩ pull up and 200 kΩ pull-down resistors. 4 state input: HIGH “H” where pin is connected to V <sub>DD</sub> , LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor Rext 68 kΩ is connected from pin to Ground. FLOAT “F” is the default setting.    |
| 29                     | SWA      | INPUT  | Pin for control of Channel A Swing levels having internal 100 kΩ pull up and 200 kΩ pull-down resistors. 4 state input: HIGH “H” where pin is connected to V <sub>DD</sub> , LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor Rext 68 kΩ is connected from pin to Ground. FLOAT “F” is the default setting.         |
| 30                     | EN       | INPUT  | Pin for device channel Enable having an internal 300 kΩ pull-up resistor. HIGH “1” where pin is connected to V <sub>DD</sub> , LOW “0” where pin is connected to Ground. Default is “1” Pin is Enabled, Low Pin is disabled.                                                                                                                                                                         |
| EP                     | GND      | GND    | Exposed pad (EP). EP on the package bottom is thermally connected to the die for improved heat transfer out of the package. The exposed pad is electrically connected to the die and must be soldered to GND on the PC Board.                                                                                                                                                                        |

Note. If EQx, FGx, SWx, and EN are needed to be at a logic High level in the application, then they must be powered simultaneously with V<sub>DD</sub>, or later.

## Power Management

The NB7NPQ1102M has an adaptive power management feature in order to minimize power consumption. When there is no termination detected, the corresponding channel will change to low power slumber mode. Accordingly, both channels will move to low power slumber mode individually. Both the channels are independent with separate controls.

While in the low power slumber mode, the receiver signal detector will continue to monitor the input channel. If a channel is in low power slumber mode, the receiver detection loop will be active again. If a load is not detected, then the channel will move to Device Unplug Mode and continuously monitor for the load. When a load is detected, the channel will return to Low Power Slumber Mode and receiver detection will be active again per 6 ms.

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**Table 2. OPERATING MODES**

| Modes                  | RIN                            | ROUT                             |
|------------------------|--------------------------------|----------------------------------|
| Power Down Mode        | 67 k $\Omega$ to Ground        | High Z                           |
| Unplug Mode            | High Z                         | 40 k $\Omega$ to V <sub>DD</sub> |
| Low Power Slumber Mode | 50 $\Omega$ to V <sub>DD</sub> | 40 k $\Omega$ to V <sub>DD</sub> |
| Active Mode            | 50 $\Omega$ to V <sub>DD</sub> | 50 $\Omega$ to V <sub>DD</sub>   |

**Table 3. EQUALIZATION SETTINGS:**

| EQA/ EQB                                         | EQ (dB)   |               |
|--------------------------------------------------|-----------|---------------|
|                                                  | @ 2.5 GHz | @ 5 GHz       |
| Low "L" (Pin tied to Ground)                     | 5.0       | 11.5          |
| Rext "R" (68 k $\Omega$ tied from pin to Ground) | 2.7       | 7.4           |
| FLOAT "F" (Pin open)                             | 4.0       | 9.9 (Default) |
| HIGH "H" (Pin tied to V <sub>DD</sub> )          | 6.5       | 13.1          |

**Table 4. FLAT GAIN SETTING**

| FGA/ FGB                                         | FG (dB)         |
|--------------------------------------------------|-----------------|
| Low "L" (Pin tied to Ground)                     | -1.2            |
| Rext "R" (68 k $\Omega$ tied from pin to Ground) | 0               |
| FLOAT "F" (Pin open)                             | +1 .0 (Default) |
| HIGH "H" (Pin tied to V <sub>DD</sub> )          | +2.0            |

**Table 8. ATTRIBUTES**

| Parameter                                                      |                                          |                        |
|----------------------------------------------------------------|------------------------------------------|------------------------|
| ESD Protection                                                 | Human Body Model<br>Charged Device Model | $\pm 4$ kV<br>> 1.5 kV |
| Moisture Sensitivity, Indefinite Time Out of Dry pack (Note 1) |                                          | Level 1                |
| Flammability Rating                                            | Oxygen Index: 28 to 34                   | UL 94 V-O @ 0.125 in   |
| Transistor Count                                               |                                          | 40517                  |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test        |                                          |                        |

1. For additional information, see Application Note AND8003/D.

**Table 9. ABSOLUTE MAXIMUM RATINGS** Over operating free-air temperature range (unless otherwise noted)

| Parameter                                                                | Description      | Min  | Max                   | Unit |
|--------------------------------------------------------------------------|------------------|------|-----------------------|------|
| Supply Voltage (Note 2)                                                  | V <sub>DD</sub>  | -0.5 | 4.6                   | V    |
| Voltage range at any input or output terminal                            | Differential I/O | -0.5 | V <sub>DD</sub> + 0.5 | V    |
|                                                                          | LVC MOS inputs   | -0.5 | V <sub>DD</sub> + 0.5 | V    |
| Output Current                                                           |                  | -25  | +25                   | mA   |
| Power Dissipation, Continuous                                            |                  |      | 1.0                   | W    |
| Storage Temperature Range, T <sub>SG</sub>                               |                  | -65  | 150                   | °C   |
| Maximum Junction Temperature, T <sub>J</sub>                             |                  |      | 125                   | °C   |
| Junction-to-Ambient Thermal Resistance @ 500 lfm, $\theta_{JA}$ (Note 3) |                  |      | TBD                   | °C/W |
| Wave Solder, Pb-Free, T <sub>SOL</sub>                                   |                  |      | 265                   | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. All voltage values are with respect to the GND terminals.

3. JEDEC standard multilayer board - 2S2P (2 signal, 2 power).

**Table 5. SWING SETTING**

| SWA/ SWB                                         | SW (mVppd)        |
|--------------------------------------------------|-------------------|
| Low "L"<br>(Pin tied to Ground)                  | 800               |
| Rext "R" (68 k $\Omega$ tied from pin to Ground) | 1200              |
| FLOAT "F"<br>(Pin open)                          | 1000<br>(Default) |
| HIGH "H"<br>(Pin tied to V <sub>DD</sub> )       | 1100              |

**Table 6. CHANNEL ENABLE SETTING**

| EN                                         | Status            |
|--------------------------------------------|-------------------|
| Low "0"<br>(Pin tied to Ground)            | Disabled          |
| HIGH "1"<br>(Pin tied to V <sub>DD</sub> ) | Enabled (Default) |

**Table 7. RECEIVER DETECTION SETTING**

| RXDET_EN                                   | Status            |
|--------------------------------------------|-------------------|
| Low "0"<br>(Pin tied to Ground)            | Disabled          |
| HIGH "1"<br>(Pin tied to V <sub>DD</sub> ) | Enabled (Default) |

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**Table 10. RECOMMENDED OPERATING CONDITIONS** Over operating free-air temperature range (unless otherwise noted)

| Parameter        | Description                                                    | Min | Typ | Max | Unit |
|------------------|----------------------------------------------------------------|-----|-----|-----|------|
| V <sub>DD</sub>  | Main power supply                                              | 3.0 | 3.3 | 3.6 | V    |
| T <sub>A</sub>   | Operating free-air temperature<br>Industrial Temperature Range | -40 |     | +85 | °C   |
| C <sub>AC</sub>  | AC coupling capacitor                                          | 75  | 100 | 265 | nF   |
| R <sub>ext</sub> | External Resistor for input control setting "R", ± 5%          |     | 68  |     | kΩ   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 11. POWER SUPPLY CHARACTERISTICS and LATENCY**

| Symbol                   | Parameter                      | Test Conditions                                 | Min | Typ (Note 4) | Max  | Unit |
|--------------------------|--------------------------------|-------------------------------------------------|-----|--------------|------|------|
| V <sub>DD</sub>          | Supply Voltage                 |                                                 | 3.0 | 3.3          | 3.6  | V    |
| I <sub>DDActive</sub>    | Active mode current            | EN = 1, 10 Gbps, compliance test pattern        |     | 115          |      | mA   |
| I <sub>DDLPslumber</sub> | Low Power Slumber mode current | EN = 1, no input signal longer than TLP-Slumber |     | 0.4          | 0.64 | mA   |
| I <sub>DDUnplug</sub>    | Unplug mode current            | EN = 1, no output load is detected              |     | 0.36         | 0.45 | mA   |
| I <sub>DDpd</sub>        | Power-down mode current        | EN = 0                                          |     | 10           | 50   | μA   |
| tpd                      | Latency                        | From Input to Output                            |     |              | 2    | ns   |

4. TYP values use V<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25°C

**Table 12. CML RECEIVER AC/DC CHARACTERISTICS**

V<sub>DD</sub> = 3.3 V ± 0.3 V Over operating free-air temperature range (unless otherwise noted)

| Symbol                                    | Parameter                                                                                                                            | Test Conditions                                            | Min | Typ | Max | Unit   |
|-------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-----|-----|-----|--------|
| R <sub>RX-DIFF-DC</sub>                   | Differential Input Impedance (DC)                                                                                                    |                                                            | 72  | 100 | 120 | Ω      |
| R <sub>RX-SINGLE-DC</sub>                 | Single-ended Input Impedance (DC)                                                                                                    | Measured with respect to GND over a voltage of 500 mV max. | 18  |     | 30  | Ω      |
| Z <sub>RX-HIZ-DC-PD</sub>                 | Common-mode input impedance for V>0 during reset or power-down (DC)                                                                  | VCM = 0 to 500 mV                                          | 25  |     |     | kΩ     |
| V <sub>RX-CM-AC-P</sub>                   | Common mode peak voltage                                                                                                             | AC up to 5 GHz                                             |     |     | 150 | mVpeak |
| V <sub>RX-CM-DC-Active-Idle-Delta-P</sub> | Common mode peak voltage<br> AvgU0( V <sub>RX-D+</sub> +V <sub>RX-D-</sub>  )/2 - AvgU1( V <sub>RX-D+</sub> +V <sub>RX-D-</sub>  )/2 | Between U0 and U1. AC up to 5 GHz                          |     |     | 200 | mVpeak |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 13. LVCMOS CONTROL PIN CHARACTERISTICS**

V<sub>DD</sub> = 3.3 V ± 0.3 V Over operating free-air temperature range (unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------------|-----|-----|-----|------|
|--------|-----------|-----------------|-----|-----|-----|------|

## 2-LEVEL CONTROL PINS LVCMOS INPUTS (EN, RXDET\_EN)

|                 |                          |  |                        |                 |                        |    |
|-----------------|--------------------------|--|------------------------|-----------------|------------------------|----|
| V <sub>IH</sub> | DC Input Logic HIGH "1"  |  | 0.65 * V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>        | V  |
| V <sub>IL</sub> | DC Input Logic LOW "0"   |  | GND                    | GND             | 0.35 * V <sub>DD</sub> | V  |
| I <sub>IH</sub> | High-level input current |  |                        |                 | 25                     | μA |
| I <sub>IL</sub> | Low-level input current  |  | -25                    |                 |                        | μA |

## 4-LEVEL CONTROL PINS LVCMOS INPUTS (EQA/EQB, FGA/FGB, SWA/SWB)

|                 |                                   |                                                                                        |                        |                        |                        |    |
|-----------------|-----------------------------------|----------------------------------------------------------------------------------------|------------------------|------------------------|------------------------|----|
| V <sub>IH</sub> | DC Input Logic HIGH; Setting "H"  | Input pin connected to VDD                                                             | 0.92 * V <sub>DD</sub> | V <sub>DD</sub>        |                        | V  |
| V <sub>IF</sub> | DC Input Logic FLOAT; Setting "F" | Input pin FLOAT (open) (Note 5), Logic 2/3 * V <sub>DD</sub>                           | 0.59 * V <sub>DD</sub> | 0.67 * V <sub>DD</sub> | 0.75 * V <sub>DD</sub> | V  |
| V <sub>IR</sub> | DC Input Logic Rext; Setting "R"  | Rext resistor 68 kΩ must be connected between pin and GND, Logic 1/3 * V <sub>DD</sub> | 0.25 * V <sub>DD</sub> | 0.33 * V <sub>DD</sub> | 0.41 * V <sub>DD</sub> | V  |
| V <sub>IL</sub> | DC Input Logic LOW; Setting "L"   | Input pin connected to GND                                                             |                        | GND                    | 0.08 * V <sub>DD</sub> | V  |
| I <sub>IH</sub> | High-level input current          |                                                                                        |                        |                        | 50                     | μA |
| I <sub>IL</sub> | Low-level input current           |                                                                                        | -50                    |                        |                        | μA |

5. Floating refers to a pin left in an open state, with no external connections.

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**Table 14. TRANSMITTER AC/DC CHARACTERISTICS**

$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$  Over operating free-air temperature range (unless otherwise noted)

| Parameter                         |                                                                                                      | Test Conditions                                                                                                                 | Min            | Typ | Max      | Unit              |
|-----------------------------------|------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|----------------|-----|----------|-------------------|
| $V_{TX-DIFF-PP}$                  | Output differential p-p voltage swing at 100 MHz                                                     | Differential Swing<br>$ V_{TX-D+} - V_{TX-D-} $                                                                                 |                |     | 1.2      | $V_{PPd}$         |
| $R_{TX-DIFF-DC}$                  | Differential TX impedance (DC)                                                                       |                                                                                                                                 | 72             |     | 120      | $\Omega$          |
| $V_{TX-RCV-DET}$                  | Voltage change allowed during receiver detect                                                        |                                                                                                                                 |                |     | 600      | mV                |
| $C_{ac\_coupling}$                | AC coupling capacitance                                                                              |                                                                                                                                 | 75             |     | 265      | nF                |
| TTX-EYE (10 Gbps)                 | Transmitter eye, Include all jitter                                                                  | At the silicon pad. 10 Gbps                                                                                                     | 0.646          |     |          | UI                |
| TTX-EYE (5 Gbps)                  | Transmitter eye, Include all jitter                                                                  | At the silicon pad. 5 Gbps                                                                                                      | 0.625          |     |          | UI                |
| TTX-DJ-DD (10 Gbps)               | Transmitter deterministic jitter                                                                     | At the silicon pad. 10 Gbps                                                                                                     |                |     | 0.17     | UI                |
| TTX-DJ-DD (5 Gbps)                | Transmitter deterministic jitter                                                                     | At the silicon pad. 5 Gbps                                                                                                      |                |     | 0.205    | UI                |
| $C_{txparasitic}$                 | Parasitic capacitor for TX                                                                           |                                                                                                                                 |                |     | 1.1      | pF                |
| $R_{TX-DC-CM}$                    | Common-mode output impedance (DC)                                                                    |                                                                                                                                 | 18             |     | 30       | $\Omega$          |
| $V_{TX-DC-CM}$                    | Instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors     | $ V_{TX-D+} + V_{TX-D-} /2$                                                                                                     | 0              |     | 2.2      | V                 |
| $V_{TX-C}$                        | Common-mode voltage                                                                                  | $ V_{TX-D+} + V_{TX-D-} /2$                                                                                                     | $V_{DD} - 1.5$ |     | $V_{DD}$ | V                 |
| $V_{TX-CM-AC-PP-Active}$          | TX AC common-mode peak-to-peak voltage swing in active mode                                          | $V_{TX-D+} + V_{TX-D-}$ for both time and amplitude                                                                             |                |     | 100      | mV <sub>PP</sub>  |
| $V_{TX-CM-DC-Active\_Idle-Delta}$ | Common mode delta voltage<br>$ AvgU0( V_{TX-D+} + V_{TX-D-} )/2 - AvgU1( V_{TX-D+} + V_{TX-D-} )/2 $ | Between U0 to U1                                                                                                                |                |     | 200      | mV-peak           |
| $V_{TX-Idle-DIFF-AC-pp}$          | Idle mode AC common mode delta voltage $ V_{TX-D+} - V_{TX-D-} $                                     | Between TX+ and TX- in idle mode. Use the HPF to remove DC components. 1/LPF. No AC and DC signals are applied to RX terminals. |                |     | 10       | mV <sub>ppd</sub> |
| $V_{TX-Idle-DIFF-DC}$             | Idle mode DC common mode delta voltage $ V_{TX-D+} - V_{TX-D-} $                                     | Between TX+ and TX- in idle mode. Use the LPF to remove DC components. 1/HPF. No AC and DC signals are applied to RX terminals. |                |     | 10       | mV                |

## CHANNEL PERFORMANCE

|                |                                                                                      |                                          |    |                             |    |                   |
|----------------|--------------------------------------------------------------------------------------|------------------------------------------|----|-----------------------------|----|-------------------|
| Gp             | Peaking gain (Compensation at 5 GHz, relative to 100 MHz, 100 mVp-p sine wave input) | EQx = L<br>EQx = R<br>EQx = F<br>EQx = H |    | 11.5<br>7.4<br>9.9<br>13.1  |    | dB                |
|                |                                                                                      | Variation around typical                 | -3 |                             | +3 |                   |
| Gf             | Flat Gain (<100 MHz, EQx=F, SWx=F)                                                   | FGx = L<br>FGx = R<br>FGx = F<br>FGx = H |    | -1.2<br>0<br>+1.0<br>+2.0   |    | dB                |
|                |                                                                                      | Variation around typical                 | -3 |                             | +3 |                   |
| $V_{SW\_100M}$ | -1 dB compression point output swing (100MHz)                                        | SWx = L<br>SWx = R<br>SWx = F<br>SWx = H |    | 800<br>1200<br>1000<br>1100 |    | mV <sub>ppd</sub> |

**Table 14. TRANSMITTER AC/DC CHARACTERISTICS**

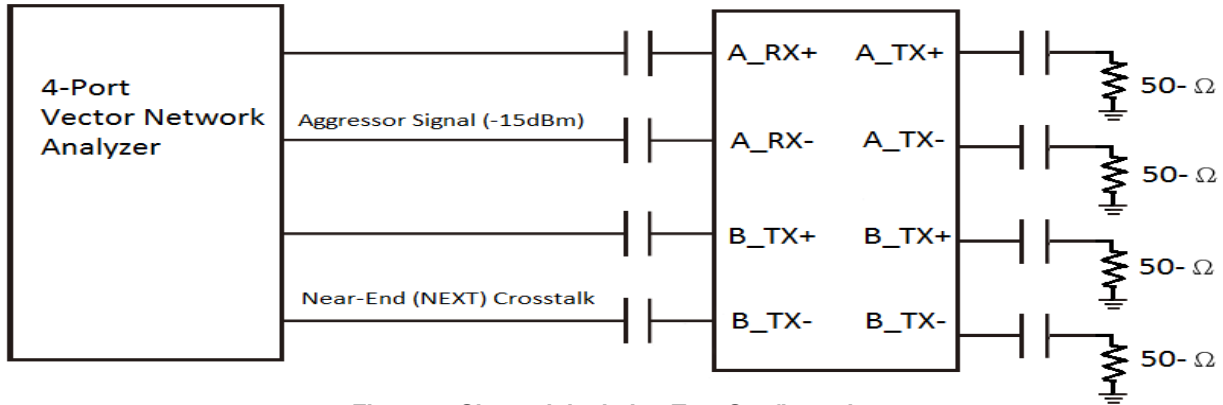
$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$  Over operating free-air temperature range (unless otherwise noted)

| Parameter                  | Test Conditions                              | Min                                      | Typ                      | Max | Unit  |
|----------------------------|----------------------------------------------|------------------------------------------|--------------------------|-----|-------|
| <b>CHANNEL PERFORMANCE</b> |                                              |                                          |                          |     |       |
| $V_{SW\_5G}$               | -1 dB compression point output swing (5 GHz) | SWx = L<br>SWx = R<br>SWx = F<br>SWx = H | 600<br>900<br>750<br>825 |     | mVppd |
| DDNEXT                     | Differential near-end crosstalk (Note 6)     | 100MHz to 5GHz, RXDET_EN = 1<br>Figure 3 | -40                      |     | dB    |

**SIGNAL AND FREQUENCY DETECTORS**

|               |                                           |                                                      |     |  |     |       |
|---------------|-------------------------------------------|------------------------------------------------------|-----|--|-----|-------|
| $V_{th\_dsm}$ | Low power slumber mode detector threshold | LFPS signal threshold in Low power Slumber mode      | 100 |  | 600 | mVppd |
| $V_{th\_am}$  | Active mode detector threshold            | Signal threshold in Active and Slumber mode (Note 8) | 45  |  | 175 | mVppd |

6. Measured using a Vector Network Analyzer (VNA) with -15 dbm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50-Ω.
7. Guaranteed by design and characterization.
8. Below the minimum is no signal  $\geq 25^\circ\text{C}$ . Above the maximum is active.



**Figure 3. Channel-isolation Test Configuration**

# NB7NPQ1102M

## Typical Application:

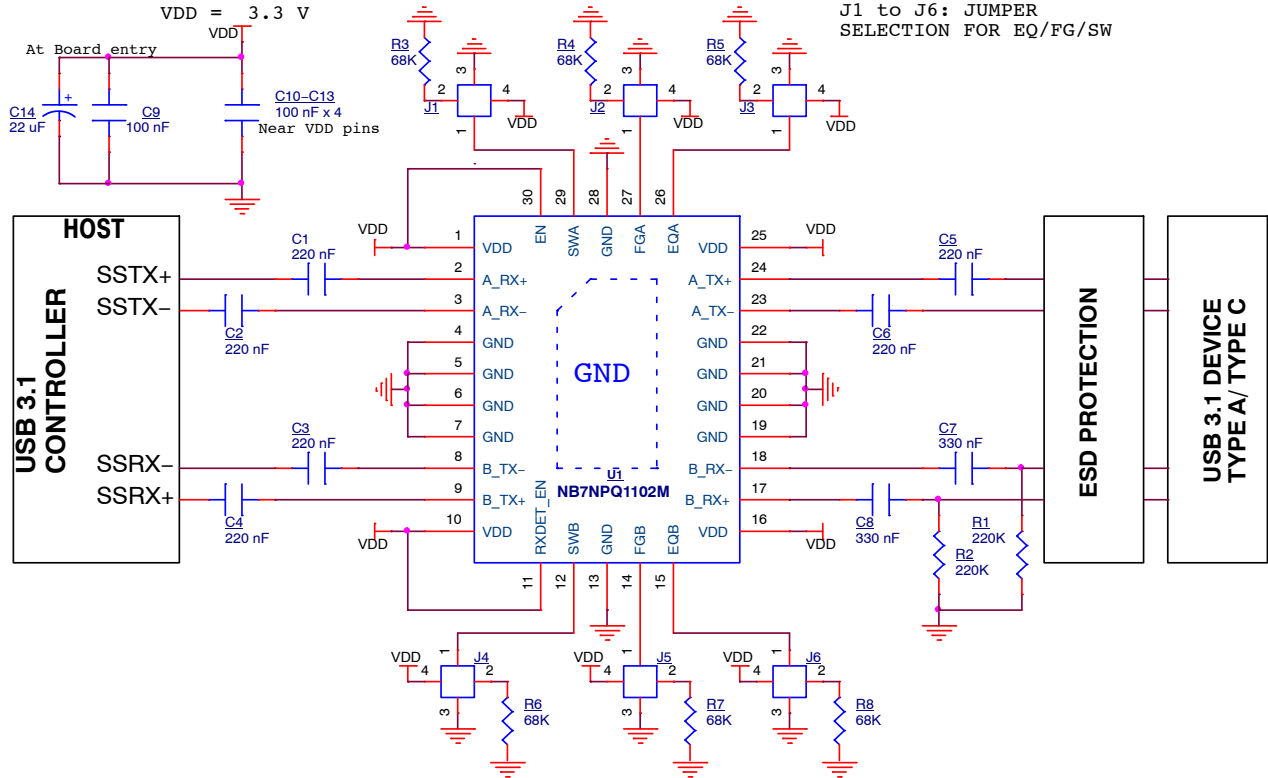


Figure 4. USB 3.1 Host Side NB7NPQ1102M Application

Table 15. DESIGN REQUIREMENTS

| Design Parameter                       | Value                                                                                                     |
|----------------------------------------|-----------------------------------------------------------------------------------------------------------|
| Supply Voltage                         | 3.3 V nominal, (3.0 V to 3.6 V)                                                                           |
| Operation Mode (Control Pin Selection) | Default FLOAT "F", adjust based on application losses. Refer Page 3 for different EQ, FG and SW settings. |
| TX AC Coupling Capacitors              | 220 nF nominal, 75 nF to 265 nF, see Figure 4                                                             |
| RX AC Coupling Capacitors              | 330 – 470 nF nominal, see Figure 4                                                                        |
| Rext                                   | 68 kΩ ± 5%                                                                                                |
| RX Pull Down Resistors at Receptacle   | 200 kΩ to 220 kΩ                                                                                          |
| Power Supply Capacitors                | 100 nF to GND close to each Vcc pin, and 22 uF to GND on the Vcc plane                                    |
| Trace loss of FR4 before NB7NPQ1102M   | Up to 13 dB losses                                                                                        |
| Trace loss of FR4 after NB7NPQ1102M    | Up To 3 dB losses. Keep as short as possible for best performance.                                        |
| DC Flat Gain Options                   | -1.2 dB, 0 dB, +1.0 dB, +2.0 dB                                                                           |
| Equalization Options                   | 7.4 to 13.1 dB                                                                                            |
| Swing Options                          | 800 to 1200 mV                                                                                            |
| Differential Trace Impedance           | 90 Ω ± 10%                                                                                                |

### Typical Layout Practices

- RX and TX pairs should maintain as close to a 90 Ω Differential impedance as possible.
- Limit the number of vias used on each data line. It is suggested that 2 or fewer are used.
- Traces should be routed as straight and symmetric as possible.
- RX and TX differential pairs should always be placed and routed on the same layer directly above a ground plane. This will help reduce EMI and noise on the data lines.
- Routing angles should be obtuse angles and kept to 135 degrees or larger.
- To minimize crosstalk, TX and RX data lines should be kept away from other high speed signals.

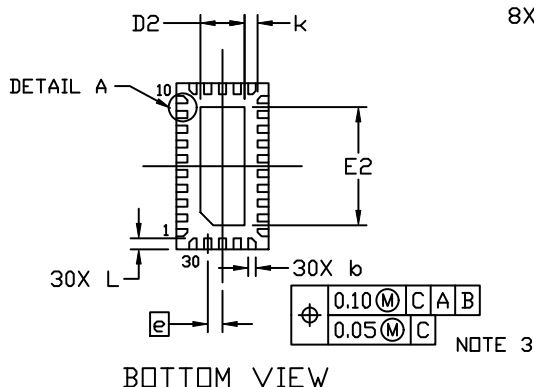
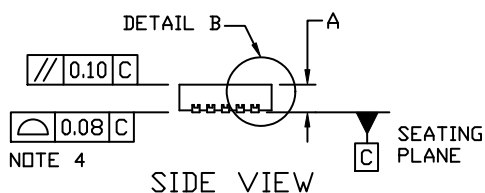
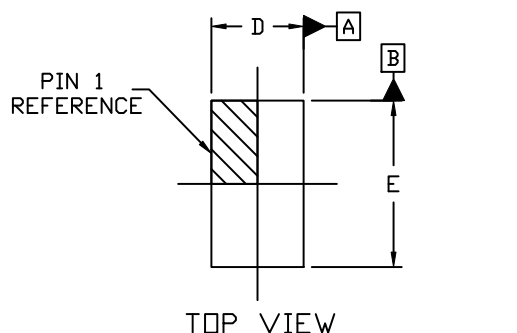


### WQFN30 2.50x4.50, 0.4P

#### CASE 510CK

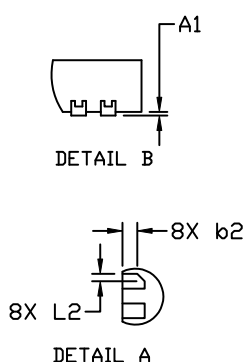
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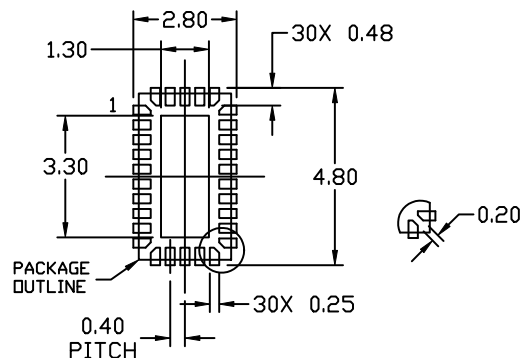


#### NOTES:

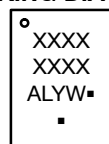
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NOM. | MAX. |
| A   | 0.70        | 0.75 | 0.80 |
| A1  | ---         | ---  | 0.05 |
| b   | 0.15        | 0.20 | 0.25 |
| b2  | 0.20 REF    |      |      |
| D   | 2.40        | 2.50 | 2.60 |
| D2  | 1.15        | 1.20 | 1.25 |
| E   | 4.40        | 4.50 | 4.60 |
| E2  | 3.15        | 3.20 | 3.25 |
| e   | 0.40 BSC    |      |      |
| K   | 0.20 REF    |      |      |
| L   | 0.25        | 0.30 | 0.35 |
| L2  | 0.10 REF    |      |      |



#### GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

#### RECOMMENDED MOUNTING FOOTPRINT

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                  |                        |                                                                                                                                                                                  |
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