THCV244A

SerDes receiver with bi-directional transceiver

1. General Description

THCV244A is designed to support 4 cameras with 1080p 30fps 16bit and 720p 60fps 16bit uncompressed video data over 15m 100ohm differential STP or single-end 50ohm coaxial cable with 4 in-line connectors between camera and processor by V-by-One® HS.

Multiple camera data input stream can be combined into one or two MIPI output stream using installed line memory and MIPI virtual channel technology.

THCV244A supports a MIPI CSI-2. Each CSI-2 data lane can transmit up to 1.2Gbps/lane.

V-by-One® HS maximum serial data rate is 4Gbps/lane. Four input lane supports HDR large amount of data or camera switch experience.

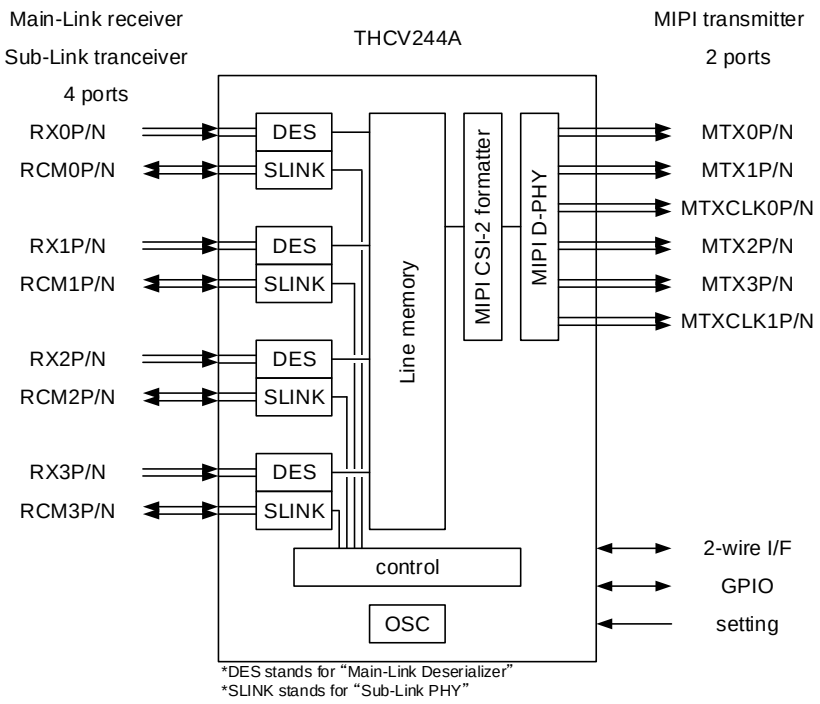
THCV244A is capable to control and monitor remote camera module from main MPU via GPIO, or 1Mbps 2-wire serial interface.

Several fault and error detection function including CRC provides hardware functional safety design.

2. Features

- MIPI CSI-2 with 1,2 or 4-lane output
- MIPI D-PHY supports 80Mbps~1.2Gbps
- MIPI Virtual channel supported
- Video formats: RAW8/10/12/14/16/20, YUV422/420, RGB888/666/565, JPEG, User-defined generic 8-bit
- V-by-One® HS 400Mbps~4Gbps x4lane
- V-by-One® HS standard version1.5
- 4 camera data integration into 1 MIPI stream
- Video stream switch and copy/distribution
- Frame sync remote supply scheme for multiple camera stream synchronization
- Wide range IO voltage from 1.7V to 3.6V
- 2-wire serial interface 1Mbps bridge function
- Remote GPIO control and monitoring
- Error detection including CRC and notification
- QFN64 9x9mm 0.5mm pitch Exp-pad package

3. Block Diagram



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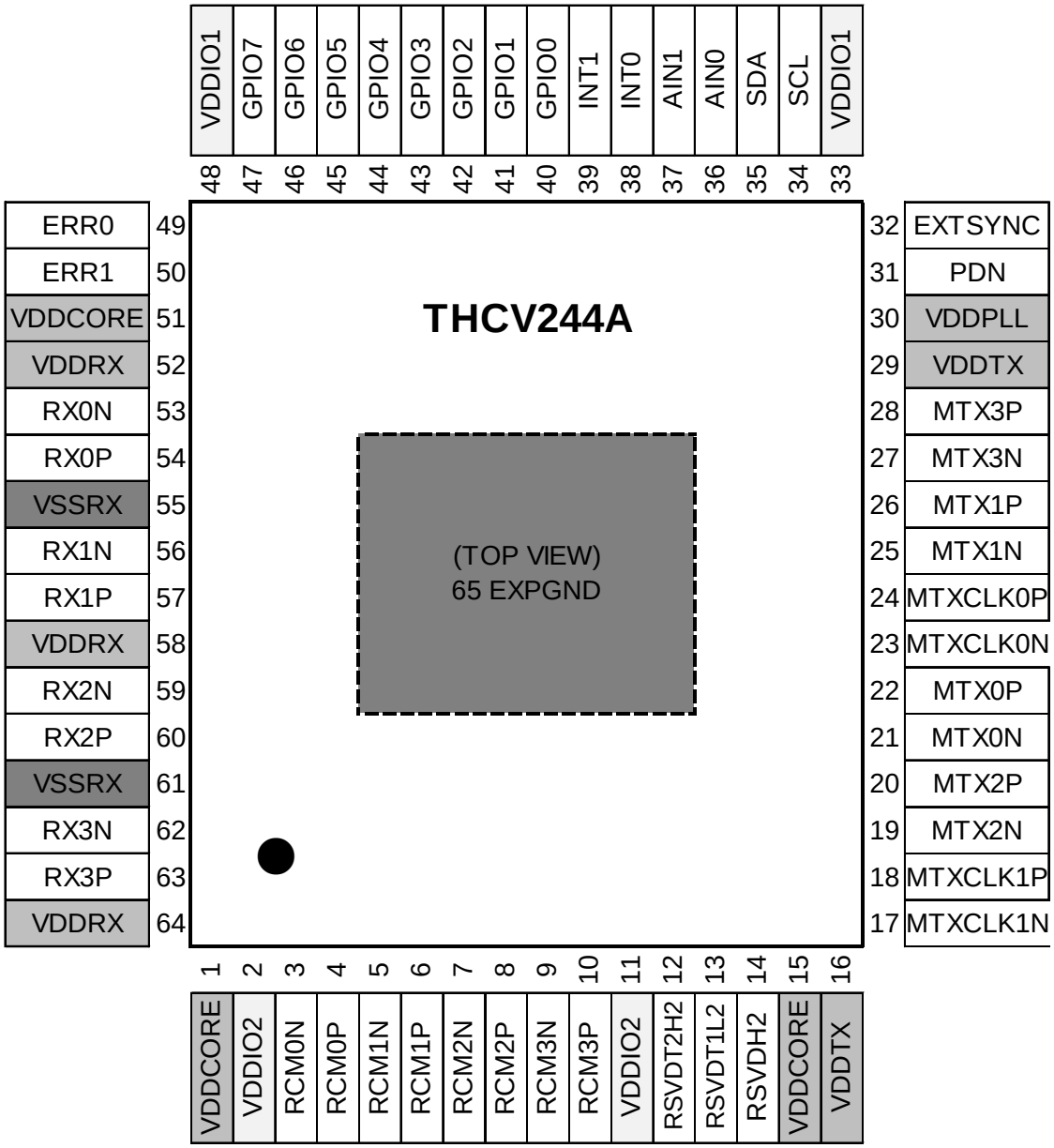
4. Pin Configuration



5. Pin Description

Pin Name	Pin #	type*	Description
RX0P/N	54, 53	CI	V-by-One® HS Input lane0
RX1P/N	57, 56	CI	V-by-One® HS Input lane1
RX2P/N	60, 59	CI	V-by-One® HS Input lane2
RX3P/N	63, 62	CI	V-by-One® HS Input lane3
RCM0P/N	4, 3	CB	CML Bi-directiona Input/Output (Sub-Link) lane0
RCM1P/N	6, 5	CB	CML Bi-directiona Input/Output (Sub-Link) lane1
RCM2P/N	8, 7	CB	CML Bi-directiona Input/Output (Sub-Link) lane2
RCM3P/N	10, 9	CB	CML Bi-directiona Input/Output (Sub-Link) lane3
MTX0P/N	22, 21	MO	MIPI differential data outputs lane0
MTX1P/N	26, 25	MO	MIPI differential data outputs lane1
MTX2P/N	20, 19	MO	MIPI differential data outputs lane2
MTX3P/N	28, 27	MO	MIPI differential data outputs lane3
MTXCLK0P/N	24, 23	MO	MIPI differential clock outputs lane0
MTXCLK1P/N	18, 17	MO	MIPI differential clock outputs lane1
RSVDT1L2	13	I	Reserved pin, Must be tied to Ground for normal operation.
RSVDT2H2	12	I	Reserved pin. Must be tied to VDDIO2 for normal operation.
PDN	31	IL	Power Down (User Power On Reset control must be reuiquired.) 0: Power Down Mode 1: Normal Operation
AIN1	37	IL	Device Address Setting for 2-wire Serial Interface [AIN1:AIN0]=00: ID=7'h0B [AIN1:AIN0]=01: ID=7'h34 [AIN1:AIN0]=10: ID=7'h77 [AIN1:AIN0]=11: ID=7'h65
AIN0	36	IL	
SCL	34	B	2-wire Serial Interface clock line
SDA	35	B	2-wire Serial Interface data line
GPIO0	40	B	General Purpose Input/Output
GPIO1	41	B	General Purpose Input/Output
GPIO2	42	B	General Purpose Input/Output
GPIO3	43	B	General Purpose Input/Output
GPIO4	44	B	General Purpose Input/Output
GPIO5	45	B	General Purpose Input/Output
GPIO6	46	B	General Purpose Input/Output
GPIO7	47	B	General Purpose Input/Output
INT0	38	O	Interrupt signal output. It must be connected w ith a pull-up resistor. 0 : Interrupt occurred 1 : Steady state
INT1	39	O	
ERR0	49	O	Internal Error / status signal monitoring output
ERR1	50	O	Internal Error / status signal monitoring output
EXTSYNC	32	B	External Sync input/output for multiple camera syncronization
RSVDH2	14	I	Reserved Pins, Must be tied to VDDIO2 for normal operation.
VDDIO1	33, 48	P	Power Supply for CMOS I/O
VDDIO2	2,11	P	Power Supply for Sub-Link I/O
VDDCORE	1,15,51	P	Power Supply for Digital Circuit
VDDRX	52,58,64	P	Power Supply for Analog Circuit
VSSRX	55,61	G	GND for Analog Circuit
VDDTX	16,29	P	Power Supply for Analog Circuit
VDDPLL	30	P	Power Supply for Analog Circuit
EXPGND	65	G	Exposed GND Pad

*type symbol ; MO=MIPI Output, CI=CML Input, CB=CML Bi-directional input/output
IL=Low Speed LVCMOS Input, I=Input, O=LVCMOS Output, B=LVCMOS Bi-directional input/output
P=Power, G=Ground

6. Functional Description

6.1. Functional Overview

THCV244A can receive CML video signal transmitted over 15m length and encode it to MIPI CSI-2 format. With High Speed CML SerDes, high reliability and robustness encoding scheme and CDR (Clock and Data Recovery) architecture, the THCV244A enables to receive RAW/YUV/RGB/JPEG/Generic8bit data through Main-Link by single 100ohm differential pair or 50ohm coaxial cable with minimal external components. In addition, THCV244A has Sub-Link which enables bi-directional transmission of 2-wire serial interface signals, GPIO signals and also HTPDN/LOCKN signals for Main-Link through the other 1-pair of CML-Line. The THCV244A system is able to watch remote devices and to control them via 2-wire serial interface or GPIOs. They also can report interrupt events caused by change of remote device statuses and internal statuses such as CRC error.

Multiple camera data input stream can be combined into one or two MIPI output stream using installed line memory and MIPI virtual channel technology.

6.2. HTPDN/LOCKN

Hot-Plug Function

HTPDN indicates Main-Link connect condition between Transmitter and Receiver. HTPDN of Transmitter side is high when Receiver is not active or not connected. Then Transmitter can enter into power down mode. HTPDN is set to Low by the Receiver when Receiver is active and connects to the Transmitter, and then Transmitter must start up and transmit CDR training pattern for link training. HTPDN is open drain output at the receiver side. Transmitter side needs Pull-up resistor.

There is an application option to omit HTPDN connection between Transmitter and Receiver. In this case, HTPDN at Transmitter side should always be at Low.

Lock Detect Function

LOCKN indicates whether CDR PLL of Main-Link is in lock status or not. LOCKN at Transmitter input is set to High by pull-up resistor when Receiver is not active or in CDR PLL training. LOCKN is set to Low by Receiver when CDR lock is completed. After that the CDR training mode finishes and then Transmitter shifts to the normal mode. LOCKN of Receiver is open drain. Transmitter side needs pull-up resistor.

When an application omits HTPDN, LOCKN signal should only be considered with HTPDN pulled low by Receiver.

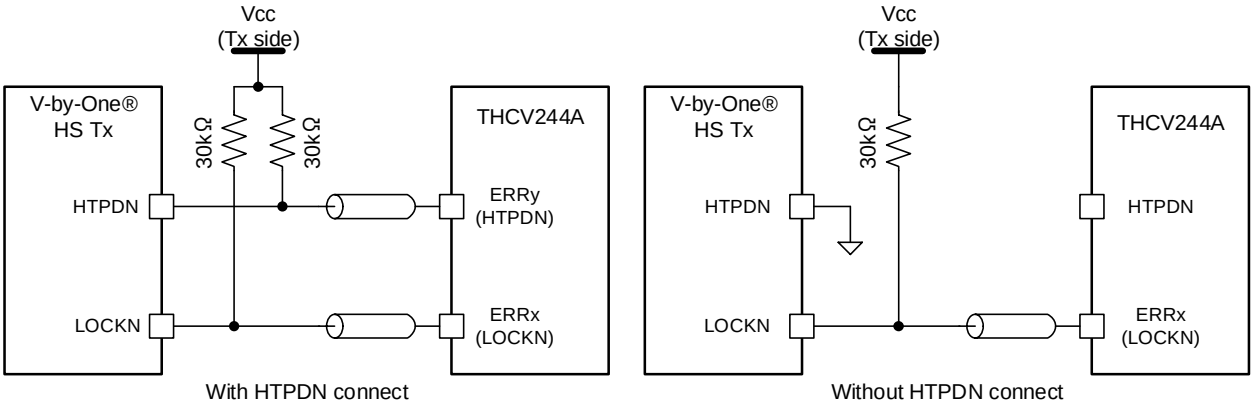


Figure 1. Physical wire connection for wired Hot-plug and Lock detect scheme

It will need same GND potential reference between transmitter and receiver device to connect HTPDN and LOCKN pins directly like above. HTPDN and LOCKN can also be transmitted via Sub-Link without physical wire connection. Assignment can be configurable by 2-wire access to internal register.

Table 1. HTPDN/LOCKN register

Address	bit	Register Name	width	R/W	Init	Description
0x0019	[7:6]	R_LOCKN_LN3_SEL	2	RW	2'h0	<this regiseter is valid when 0x0010[3]=0x1> Select the source signal to be transmitted as LOCKN and HTPDN via Sub-Link Lane3 0x0: LOCKN3 0x1: LOCKN2 or LOCKN3 0x2: LOCKN0 or LOCKN1 or LOCKN2 or LOCKN3 0x3: LOCKN and HTPDN signal level are LOW forcibly *LOCKN3: LOCKN signal of V-by-One(R) HS Lane3 (RX3P/RX3N) *HTPDN of the same lane as above set LOCKN lane is used
	[5:4]	R_LOCKN_LN2_SEL	2	RW	2'h0	<this regiseter is valid when 0x0010[2]=0x1> Select the source signal to be transmitted as LOCKN and HTPDN via Sub-Link Lane2 0x0: LOCKN2 0x1: LOCKN2 or LOCKN3 0x2: LOCKN0 or LOCKN1 or LOCKN2 or LOCKN3 0x3: LOCKN and HTPDN signal level are LOW forcibly *LOCKN2: LOCKN signal of V-by-One(R) HS Lane2 (RX2P/RX2N) *HTPDN of the same lane as above set LOCKN lane is used
	[3:2]	R_LOCKN_LN1_SEL	2	RW	2'h0	<this regiseter is valid when 0x0010[1]=0x1> Select the source signal to be transmitted as LOCKN and HTPDN via Sub-Link Lane1 0x0: LOCKN1 0x1: LOCKN0 or LOCKN1 0x2: LOCKN0 or LOCKN1 or LOCKN2 or LOCKN3 0x3: LOCKN and HTPDN signal level are LOW forcibly *LOCKN1: LOCKN signal of V-by-One(R) HS Lane1 (RX1P/RX1N) *HTPDN of the same lane as above set LOCKN lane is used
	[1:0]	R_LOCKN_LN0_SEL	2	RW	2'h0	<this regiseter is valid when 0x0010[0]=0x1> Select the source signal to be transmitted as LOCKN and HTPDN via Sub-Link Lane0 0x0: LOCKN0 0x1: LOCKN0 or LOCKN1 0x2: Reserved 0x3: LOCKN and HTPDN signal level are LOW forcibly *LOCKN0: LOCKN signal of V-by-One(R) HS Lane0 (RX0P/RX0N) *HTPDN of the same lane as above set LOCKN lane is used

6.3. V-by-One® HS input setting

THCV244A has a V-by-One® HS receiver and it can be connected a V-by-One® HS transmitter via transmission line divided by AC-coupled.

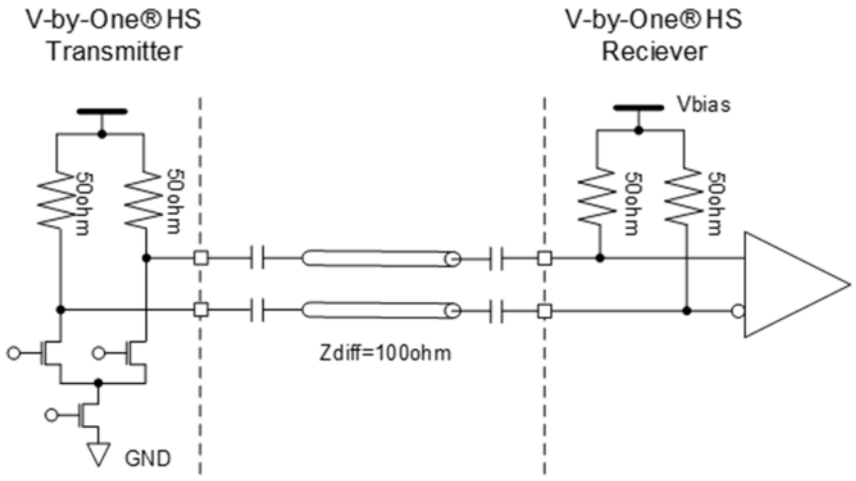


Figure 1. V-by-One® HS connection scheme (differential transmission case)

Setting of V-by-One® HS input format can be configurable by 2-wire access to internal register.

Table 2. V-by-One® HS input format setting (all lanes)

Address	bit	Register Name	width	R/W	init	Description
0x1012	[7:5]	reserved	3	-	-	-
	[4]	R_RGB565_ON_L0	1	R/W	1'h0	<this regiseter is valid only when 0x1012[3:0]=0x1> Main-Link Input Data Format Setting2 for all lane 0x0: RGB888 0x1: RGB565
	[3:0]	R_VX1_LANE_FMT0	4	R/W	4'h0	Main-Link Input Data Format Setting for all lane 0x0: MPRF (Main-Link PRivate Format) 0x1: RGB888 or RGB565 0x2: YUV422 - Normal Mode1 0x3: YUV422 - Normal Mode2 0x4: YUV422 - Normal Mode3 0x5: YUV422 - Demux Mode1 0x6: YUV422 - Demux Mode2 0x7: RAW8 - Normal Mode1 0x8: RAW8 - Normal Mode2 0x9: RAW8 - Demux Mode1 0xA: RAW10 - Normal Mode1 0xB: RAW10 - Demux Mode1 0xC: RAW10 - Demux Mode2 0xD: RAW12 - Normal Mode1 0xE: RAW12 - Demux Mode1 0xF: RAW12 - Demux Mode2

Table 3. V-by-One® HS input format setting (Lane0)

Address	bit	Register Name	width	R/W	init	Description
0x1010	[7:6]	R_MLINK_NHSEL0	2	R/W	2'h2	V-by-One® Main-Link Mode Select (for Lane0) 0x2: V-by-One® HS standard mode Other: Reserved
	[5:4]	R_MLINK_COL0	2	R/W	2'h1	V-by-One® Main-Link Byte Mode Select (for Lane0) 0x1: 3Byte mode 0x2: 4Byte mode Other: Reserved * use case setting example MPRF : 0x2 RGB888 or RGB565 : 0x1 YUV422 - Normal Mode1 : 0x1 YUV422 - Normal Mode2 : 0x1 YUV422 - Normal Mode3 : 0x1 YUV422 - Demux Mode1 : 0x2 YUV422 - Demux Mode2 : 0x2 RAW8 - Normal Mode1 : 0x1 RAW8 - Normal Mode2 : 0x1 RAW8 - Demux Mode1 : 0x2 RAW10 - Normal Mode1 : 0x1 RAW10 - Demux Mode1 : 0x2 RAW10 - Demux Mode2 : 0x1 RAW12 - Normal Mode1 : 0x1 RAW12 - Demux Mode1 : 0x2 RAW12 - Demux Mode2 : 0x1

Table 4. V-by-One® HS input format setting (Lane1)

Address	bit	Register Name	width	R/W	init	Description
0x1014	[7:6]	R_MLINK_NHSEL1	2	R/W	2'h2	V-by-One® Main-Link Mode Select (for Lane1) 0x2: V-by-One® HS standard mode Ohter: Reserved
	[5:4]	R_MLINK_COL1	2	R/W	2'h1	V-by-One® Main-Link Byte Mode Select (for Lane1) 0x1: 3Byte mode 0x2: 4Byte mode Other: Reserved * use case setting example MPRF : 0x2 RGB888 or RGB565 : 0x1 YUV422 - Normal Mode1 : 0x1 YUV422 - Normal Mode2 : 0x1 YUV422 - Normal Mode3 : 0x1 YUV422 - Demux Mode1 : 0x2 YUV422 - Demux Mode2 : 0x2 RAW8 - Normal Mode1 : 0x1 RAW8 - Normal Mode2 : 0x1 RAW8 - Demux Mode1 : 0x2 RAW10 - Normal Mode1 : 0x1 RAW10 - Demux Mode1 : 0x2 RAW10 - Demux Mode2 : 0x1 RAW12 - Normal Mode1 : 0x1 RAW12 - Demux Mode1 : 0x2 RAW12 - Demux Mode2 : 0x1

Table 5. V-by-One® HS input format setting (Lane2)

Address	bit	Register Name	width	R/W	init	Description
0x1018	[7:6]	R_MLINK_NHSEL2	2	R/W	2'h2	V-by-One® Main-Link Mode Select (for Lane2) 0x2: V-by-One® HS standard mode Other: Reserved
	[5:4]	R_MLINK_COL2	2	R/W	2'h1	V-by-One® Main-Link Byte Mode Select (for Lane2) 0x1: 3Byte mode 0x2: 4Byte mode Other: Reserved * use case setting example MPRF : 0x2 RGB888 or RGB565 : 0x1 YUV422 - Normal Mode1 : 0x1 YUV422 - Normal Mode2 : 0x1 YUV422 - Normal Mode3 : 0x1 YUV422 - Demux Mode1 : 0x2 YUV422 - Demux Mode2 : 0x2 RAW8 - Normal Mode1 : 0x1 RAW8 - Normal Mode2 : 0x1 RAW8 - Demux Mode1 : 0x2 RAW10 - Normal Mode1 : 0x1 RAW10 - Demux Mode1 : 0x2 RAW10 - Demux Mode2 : 0x1 RAW12 - Normal Mode1 : 0x1 RAW12 - Demux Mode1 : 0x2 RAW12 - Demux Mode2 : 0x1

Table 6. V-by-One® HS input format setting (Lane3)

Address	bit	Register Name	width	R/W	init	Description
0x101C	[7:6]	R_MLINK_NHSEL3	2	R/W	2'h2	V-by-One® Main-Link Mode Select (for Lane3) 0x2: V-by-One® HS standard mode Other: Reserved
	[5:4]	R_MLINK_COL3	2	R/W	2'h1	V-by-One® Main-Link Byte Mode Select (for Lane3) 0x1: 3Byte mode 0x2: 4Byte mode Other: Reserved * use case setting example MPRF : 0x2 RGB888 or RGB565 : 0x1 YUV422 - Normal Mode1 : 0x1 YUV422 - Normal Mode2 : 0x1 YUV422 - Normal Mode3 : 0x1 YUV422 - Demux Mode1 : 0x2 YUV422 - Demux Mode2 : 0x2 RAW8 - Normal Mode1 : 0x1 RAW8 - Normal Mode2 : 0x1 RAW8 - Demux Mode1 : 0x2 RAW10 - Normal Mode1 : 0x1 RAW10 - Demux Mode1 : 0x2 RAW10 - Demux Mode2 : 0x1 RAW12 - Normal Mode1 : 0x1 RAW12 - Demux Mode1 : 0x2 RAW12 - Demux Mode2 : 0x1

6.3.1. MPRF (Main-Link PRivate Format)

MPRF format encoding preserves original data packet input to V-by-One® HS transmitter and output the data packet from THCV244A. The counterpart transmitter must have installed MPRF format decoder like THCV241A because MPRF is not standard format.

Input V-by-One® HS Byte Mode is 4Byte Mode.

Video formats: RAW8/10/12/14/16/20, YUV422/420, RGB888/666/565, JPEG, and User-defined generic 8-bit are all supported with MPRF.

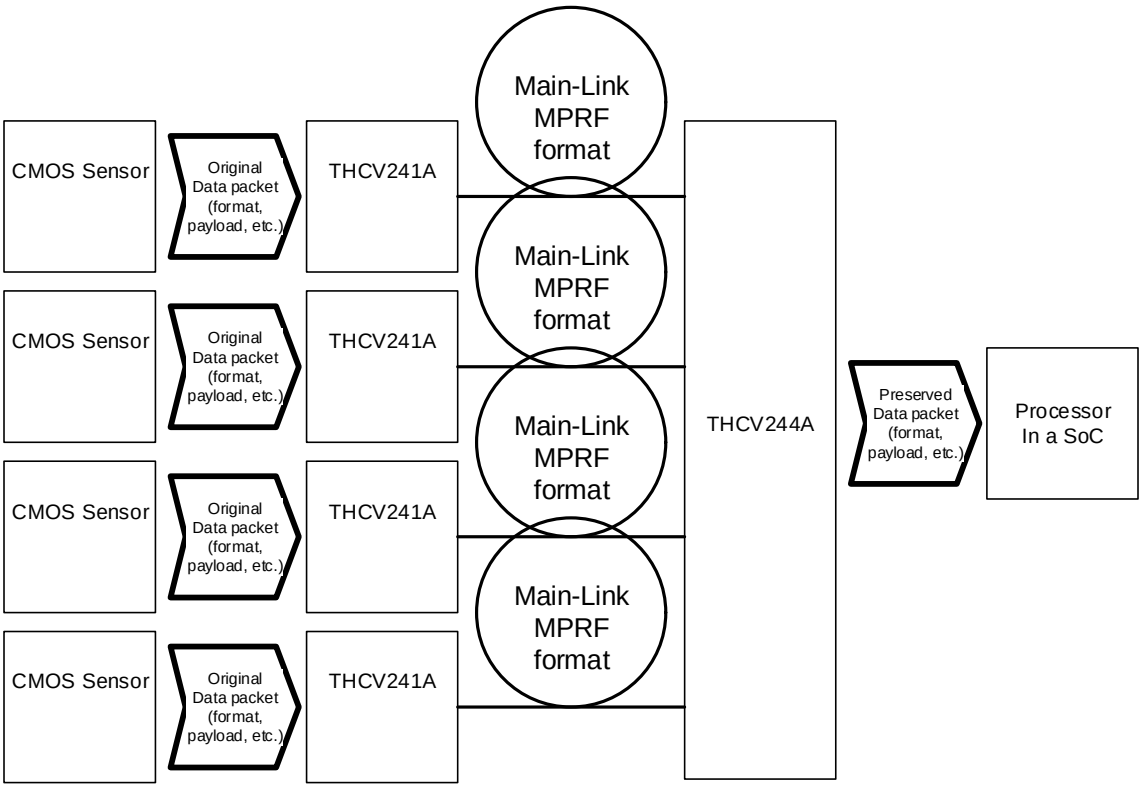


Figure 2. MPRF (Main-Link PRivate Format)

6.3.2. V-by-One® HS standard format

THCV244A input format capabilities as receiver are shown as follows. D[31:0] indicates V-by-One® HS standard version1.5 UnPacker packet definition. Data can be transmitted normally only when both transmitter and receiver are set to the same available format. Some of the THCV244A format may not be supported by particular counterpart transmitter because THCV244A prepares multiple formats that suit to multiple transmitter devices alternatives.

Table 7. V-by-One® HS input data mapping format (1/4)

Format Name	RGB888	YUV422				
Vx1HS std. Packer Packet ref.		Normal Mode1	Normal Mode2	Normal Mode3	Demux Mode1	Demux Mode2
V-by-One®HS_D[31]	0	0	0	0	Y[7](1st pixel)	Cb[7]
V-by-One®HS_D[30]	0	0	0	0	Y[6](1st pixel)	Cb[6]
V-by-One®HS_D[29]	0	0	0	0	Y[5](1st pixel)	Cb[5]
V-by-One®HS_D[28]	0	0	0	0	Y[4](1st pixel)	Cb[4]
V-by-One®HS_D[27]	0	0	0	0	Y[3](1st pixel)	Cb[3]
V-by-One®HS_D[26]	0	0	0	0	Y[2](1st pixel)	Cb[2]
V-by-One®HS_D[25]	0	0	0	0	Y[1](1st pixel)	Cb[1]
V-by-One®HS_D[24]	0	0	0	0	Y[0](1st pixel)	Cb[0]
V-by-One®HS_D[23]	B[7]	0	Cb[7]/Cr[7]	Y[7]	Cb[7]	Y[7](1st pixel)
V-by-One®HS_D[22]	B[6]	0	Cb[6]/Cr[6]	Y[6]	Cb[6]	Y[6](1st pixel)
V-by-One®HS_D[21]	B[5]	0	Cb[5]/Cr[5]	Y[5]	Cb[5]	Y[5](1st pixel)
V-by-One®HS_D[20]	B[4]	0	Cb[4]/Cr[4]	Y[4]	Cb[4]	Y[4](1st pixel)
V-by-One®HS_D[19]	B[3]	0	Cb[3]/Cr[3]	Y[3]	Cb[3]	Y[3](1st pixel)
V-by-One®HS_D[18]	B[2]	0	Cb[2]/Cr[2]	Y[2]	Cb[2]	Y[2](1st pixel)
V-by-One®HS_D[17]	B[1]	0	Cb[1]/Cr[1]	Y[1]	Cb[1]	Y[1](1st pixel)
V-by-One®HS_D[16]	B[0]	0	Cb[0]/Cr[0]	Y[0]	Cb[0]	Y[0](1st pixel)
V-by-One®HS_D[15]	G[7]	Y[7]	0	0	Y[7](2nd pixel)	Cr[7]
V-by-One®HS_D[14]	G[6]	Y[6]	0	0	Y[6](2nd pixel)	Cr[6]
V-by-One®HS_D[13]	G[5]	Y[5]	0	0	Y[5](2nd pixel)	Cr[5]
V-by-One®HS_D[12]	G[4]	Y[4]	0	0	Y[4](2nd pixel)	Cr[4]
V-by-One®HS_D[11]	G[3]	Y[3]	0	0	Y[3](2nd pixel)	Cr[3]
V-by-One®HS_D[10]	G[2]	Y[2]	0	0	Y[2](2nd pixel)	Cr[2]
V-by-One®HS_D[9]	G[1]	Y[1]	0	0	Y[1](2nd pixel)	Cr[1]
V-by-One®HS_D[8]	G[0]	Y[0]	0	0	Y[0](2nd pixel)	Cr[0]
V-by-One®HS_D[7]	R[7]	Cb[7]/Cr[7]	Y[7]	Cb[7]/Cr[7]	Cr[7]	Y[7](2nd pixel)
V-by-One®HS_D[6]	R[6]	Cb[6]/Cr[6]	Y[6]	Cb[6]/Cr[6]	Cr[6]	Y[6](2nd pixel)
V-by-One®HS_D[5]	R[5]	Cb[5]/Cr[5]	Y[5]	Cb[5]/Cr[5]	Cr[5]	Y[5](2nd pixel)
V-by-One®HS_D[4]	R[4]	Cb[4]/Cr[4]	Y[4]	Cb[4]/Cr[4]	Cr[4]	Y[4](2nd pixel)
V-by-One®HS_D[3]	R[3]	Cb[3]/Cr[3]	Y[3]	Cb[3]/Cr[3]	Cr[3]	Y[3](2nd pixel)
V-by-One®HS_D[2]	R[2]	Cb[2]/Cr[2]	Y[2]	Cb[2]/Cr[2]	Cr[2]	Y[2](2nd pixel)
V-by-One®HS_D[1]	R[1]	Cb[1]/Cr[1]	Y[1]	Cb[1]/Cr[1]	Cr[1]	Y[1](2nd pixel)
V-by-One®HS_D[0]	R[0]	Cb[0]/Cr[0]	Y[0]	Cb[0]/Cr[0]	Cr[0]	Y[0](2nd pixel)

Table 8. V-by-One® HS input data mapping format (2/4)

Format Name	RAW8		
Vx1HS std. Packer Packet ref.	Normal Mode1	Normal Mode2	Demux Mode1
V-by-One®HS_D[31]	0	0	RAW[7] (2nd pixel)
V-by-One®HS_D[30]	0	0	RAW[6] (2nd pixel)
V-by-One®HS_D[29]	0	0	RAW[5] (2nd pixel)
V-by-One®HS_D[28]	0	0	RAW[4] (2nd pixel)
V-by-One®HS_D[27]	0	0	RAW[3] (2nd pixel)
V-by-One®HS_D[26]	0	0	RAW[2] (2nd pixel)
V-by-One®HS_D[25]	0	0	RAW[1] (2nd pixel)
V-by-One®HS_D[24]	0	0	RAW[0] (2nd pixel)
V-by-One®HS_D[23]	0	RAW[7] (1st pixel)	RAW[7] (1st pixel)
V-by-One®HS_D[22]	0	RAW[6] (1st pixel)	RAW[6] (1st pixel)
V-by-One®HS_D[21]	0	RAW[5] (1st pixel)	RAW[5] (1st pixel)
V-by-One®HS_D[20]	0	RAW[4] (1st pixel)	RAW[4] (1st pixel)
V-by-One®HS_D[19]	0	RAW[3] (1st pixel)	RAW[3] (1st pixel)
V-by-One®HS_D[18]	0	RAW[2] (1st pixel)	RAW[2] (1st pixel)
V-by-One®HS_D[17]	0	RAW[1] (1st pixel)	RAW[1] (1st pixel)
V-by-One®HS_D[16]	0	RAW[0] (1st pixel)	RAW[0] (1st pixel)
V-by-One®HS_D[15]	RAW[7] (2nd pixel)	0	RAW[7] (4th pixel)
V-by-One®HS_D[14]	RAW[6] (2nd pixel)	0	RAW[6] (4th pixel)
V-by-One®HS_D[13]	RAW[5] (2nd pixel)	0	RAW[5] (4th pixel)
V-by-One®HS_D[12]	RAW[4] (2nd pixel)	0	RAW[4] (4th pixel)
V-by-One®HS_D[11]	RAW[3] (2nd pixel)	0	RAW[3] (4th pixel)
V-by-One®HS_D[10]	RAW[2] (2nd pixel)	0	RAW[2] (4th pixel)
V-by-One®HS_D[9]	RAW[1] (2nd pixel)	0	RAW[1] (4th pixel)
V-by-One®HS_D[8]	RAW[0] (2nd pixel)	0	RAW[0] (4th pixel)
V-by-One®HS_D[7]	RAW[7] (1st pixel)	RAW[7] (2nd pixel)	RAW[7] (3rd pixel)
V-by-One®HS_D[6]	RAW[6] (1st pixel)	RAW[6] (2nd pixel)	RAW[6] (3rd pixel)
V-by-One®HS_D[5]	RAW[5] (1st pixel)	RAW[5] (2nd pixel)	RAW[5] (3rd pixel)
V-by-One®HS_D[4]	RAW[4] (1st pixel)	RAW[4] (2nd pixel)	RAW[4] (3rd pixel)
V-by-One®HS_D[3]	RAW[3] (1st pixel)	RAW[3] (2nd pixel)	RAW[3] (3rd pixel)
V-by-One®HS_D[2]	RAW[2] (1st pixel)	RAW[2] (2nd pixel)	RAW[2] (3rd pixel)
V-by-One®HS_D[1]	RAW[1] (1st pixel)	RAW[1] (2nd pixel)	RAW[1] (3rd pixel)
V-by-One®HS_D[0]	RAW[0] (1st pixel)	RAW[0] (2nd pixel)	RAW[0] (3rd pixel)

Table 9. V-by-One® HS input data mapping format (3/4)

Format Name	RAW10		
Vx1HS std. Packer Packet ref.	Normal	Demux Mode1	Demux Mode2
V-by-One®HS_D[31]	0	0	0
V-by-One®HS_D[30]	0	0	0
V-by-One®HS_D[29]	0	0	0
V-by-One®HS_D[28]	0	0	0
V-by-One®HS_D[27]	0	0	0
V-by-One®HS_D[26]	0	0	0
V-by-One®HS_D[25]	0	RAW[1](1st pixel)	0
V-by-One®HS_D[24]	0	RAW[0](1st pixel)	0
V-by-One®HS_D[23]	0	RAW[9](1st pixel)	0
V-by-One®HS_D[22]	0	RAW[8](1st pixel)	0
V-by-One®HS_D[21]	0	RAW[7](1st pixel)	RAW[1](1st pixel)
V-by-One®HS_D[20]	0	RAW[6](1st pixel)	RAW[0](1st pixel)
V-by-One®HS_D[19]	0	RAW[5](1st pixel)	RAW[9](1st pixel)
V-by-One®HS_D[18]	0	RAW[4](1st pixel)	RAW[8](1st pixel)
V-by-One®HS_D[17]	0	RAW[3](1st pixel)	RAW[7](1st pixel)
V-by-One®HS_D[16]	0	RAW[2](1st pixel)	RAW[6](1st pixel)
V-by-One®HS_D[15]	0	0	RAW[5](1st pixel)
V-by-One®HS_D[14]	0	0	RAW[4](1st pixel)
V-by-One®HS_D[13]	0	0	RAW[3](1st pixel)
V-by-One®HS_D[12]	0	0	RAW[2](1st pixel)
V-by-One®HS_D[11]	0	0	0
V-by-One®HS_D[10]	0	0	0
V-by-One®HS_D[9]	RAW[1]	RAW[1](2nd pixel)	RAW[1](2nd pixel)
V-by-One®HS_D[8]	RAW[0]	RAW[0](2nd pixel)	RAW[0](2nd pixel)
V-by-One®HS_D[7]	RAW[9]	RAW[9](2nd pixel)	RAW[9](2nd pixel)
V-by-One®HS_D[6]	RAW[8]	RAW[8](2nd pixel)	RAW[8](2nd pixel)
V-by-One®HS_D[5]	RAW[7]	RAW[7](2nd pixel)	RAW[7](2nd pixel)
V-by-One®HS_D[4]	RAW[6]	RAW[6](2nd pixel)	RAW[6](2nd pixel)
V-by-One®HS_D[3]	RAW[5]	RAW[5](2nd pixel)	RAW[5](2nd pixel)
V-by-One®HS_D[2]	RAW[4]	RAW[4](2nd pixel)	RAW[4](2nd pixel)
V-by-One®HS_D[1]	RAW[3]	RAW[3](2nd pixel)	RAW[3](2nd pixel)
V-by-One®HS_D[0]	RAW[2]	RAW[2](2nd pixel)	RAW[2](2nd pixel)

Table 10. V-by-One® HS input data mapping format (4/4)

Format Name	RAW12		
Vx1HS std. Packer Packet ref.	Normal	Demux Mode1	Demux Mode2
V-by-One®HS_D[31]	0	0	0
V-by-One®HS_D[30]	0	0	0
V-by-One®HS_D[29]	0	0	0
V-by-One®HS_D[28]	0	0	0
V-by-One®HS_D[27]	0	RAW[3](1st pixel)	0
V-by-One®HS_D[26]	0	RAW[2](1st pixel)	0
V-by-One®HS_D[25]	0	RAW[1](1st pixel)	0
V-by-One®HS_D[24]	0	RAW[0](1st pixel)	0
V-by-One®HS_D[23]	0	RAW[11](1st pixel)	RAW[3](1st pixel)
V-by-One®HS_D[22]	0	RAW[10](1st pixel)	RAW[2](1st pixel)
V-by-One®HS_D[21]	0	RAW[9](1st pixel)	RAW[1](1st pixel)
V-by-One®HS_D[20]	0	RAW[8](1st pixel)	RAW[0](1st pixel)
V-by-One®HS_D[19]	0	RAW[7](1st pixel)	RAW[11](1st pixel)
V-by-One®HS_D[18]	0	RAW[6](1st pixel)	RAW[10](1st pixel)
V-by-One®HS_D[17]	0	RAW[5](1st pixel)	RAW[9](1st pixel)
V-by-One®HS_D[16]	0	RAW[4](1st pixel)	RAW[8](1st pixel)
V-by-One®HS_D[15]	0	0	RAW[7](1st pixel)
V-by-One®HS_D[14]	0	0	RAW[6](1st pixel)
V-by-One®HS_D[13]	0	0	RAW[5](1st pixel)
V-by-One®HS_D[12]	0	0	RAW[4](1st pixel)
V-by-One®HS_D[11]	RAW[3]	RAW[3](2nd pixel)	RAW[3](2nd pixel)
V-by-One®HS_D[10]	RAW[2]	RAW[2](2nd pixel)	RAW[2](2nd pixel)
V-by-One®HS_D[9]	RAW[1]	RAW[1](2nd pixel)	RAW[1](2nd pixel)
V-by-One®HS_D[8]	RAW[0]	RAW[0](2nd pixel)	RAW[0](2nd pixel)
V-by-One®HS_D[7]	RAW[11]	RAW[11](2nd pixel)	RAW[11](2nd pixel)
V-by-One®HS_D[6]	RAW[10]	RAW[10](2nd pixel)	RAW[10](2nd pixel)
V-by-One®HS_D[5]	RAW[9]	RAW[9](2nd pixel)	RAW[9](2nd pixel)
V-by-One®HS_D[4]	RAW[8]	RAW[8](2nd pixel)	RAW[8](2nd pixel)
V-by-One®HS_D[3]	RAW[7]	RAW[7](2nd pixel)	RAW[7](2nd pixel)
V-by-One®HS_D[2]	RAW[6]	RAW[6](2nd pixel)	RAW[6](2nd pixel)
V-by-One®HS_D[1]	RAW[5]	RAW[5](2nd pixel)	RAW[5](2nd pixel)
V-by-One®HS_D[0]	RAW[4]	RAW[4](2nd pixel)	RAW[4](2nd pixel)

6.4. Header/Packet/Sync Pre-processing

Setting of Header, Packet and Sync pre-processing can be configurable by 2-wire access to internal register.

Settings of Header, Packet and Sync pre-processing exist for each Main-Link input lanes respectively.

Table 11. Header/Packet/Sync pre-processing setting for Main-Link (Lane0)

Address	bit	Register Name	width	R/W	Init	Description
0x1100	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_PH_EN0	1	R/W	1'h0	MIPI Packet Header mode select for Main-Link Lane0 0x0: Packet Header is generated by register settings 0x1: Packet Header is through from Main-Link input stream
0x1101	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_CRC_EN0	1	R/W	1'h0	Main-Link CRC mode select for Main-Link Lane0 0x0: Main-Link input stream does not have CRC data 0x1: Main-Link input stream has CRC data
0x1102	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_SP_EN0	1	R/W	1'h0	MIPI Short Packet mode select for Main-Link Lane0 0x0: Main-Link input stream does not have Short Packet 0x1: Short Packet is through from Main-Link input stream
0x1103	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VVALID_MODE0	1	R/W	1'h0	MIPI Frame Start & Frame End (FS/FE) mode select for Main-Link Lane0 0x0: FS/FE data are through from Main-Link input stream 0x1: FS/FE data are generated based on the timing of the VSYNC signal
0x1104	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VSYNC_POL0	1	R/W	1'h0	<this register is valid only when 0x1103[0]=0x1> Polarity setting of VSYNC signal to generate FS/FE for Main-Link Lane0 0x0: use Low pulse VSYNC signal (FE: Falling timing, FS: Rising timing) 0x1: use High pulse VSYNC signal (FE: Rising timing, FS: Falling timing)
0x1105	[7:0]	R_VX1_WC_LOW0	8	R/W	8'h00	<this register is valid only when 0x1100[0]=0x0> MIPI Packet Header's Word Count (LSB) manual setting for Main-Link Lane0
0x1106	[7:0]	R_VX1_WC_UP0	8	R/W	8'h00	<this register is valid only when 0x1100[0]=0x0> MIPI Packet Header's Word Count (MSB) manual setting for Main-Link Lane0
0x1107	[7:0]	R_VX1_DATAID0	8	R/W	8'h00	<this register is valid only when 0x1100[0]=0x0> MIPI Packet Header's Data ID manual setting for Main-Link Lane0 * use case setting example YUV422-8bit: 0x1E RGB888: 0x24 RAW8: 0x2A RAW10: 0x2B RAW12: 0x2C
0x1108	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_MASK_ECC0	1	R/W	1'h0	Masking and Ignoring both MIPI short packet and MIPI long packet when ECC double error is detected for Main-Link Lane0 0x0: Disable 0x1: Mask Processing when ECC double error is detected
0x1109	[7:1]	reserved	7	-	7'h00	-
	[0]	reservedL	1	R/W	1'h0	must be left 0x0 (default setting)
0x110A	[7:1]	reserved	7	-	7'h00	-
	[0]	R_CRC_ERR0	1	RC	1'h0	CRC error register for Main-Link Lane0 (clear the error status after reading register automatically) 0x0: no error 0x1: detect CRC error
0x110B	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_CRCT_ERR0	1	RC	1'h0	ECC single error register for Main-Link Lane0 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC single error
0x110C	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_DOUBLE_ERR0	1	RC	1'h0	ECC double error register for Main-Link Lane0 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC double error

Table 12. Header/Packet/Sync pre-processing setting for Main-Link (Lane1)

Address	bit	Register Name	width	R/W	Init	Description
0x1200	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_PH_EN1	1	R/W	1'h0	MIPI Packet Header mode select for Main-Link Lane1 0x0: Packet Header is generated by register settings 0x1: Packet Header is through from Main-Link input stream
0x1201	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_CRC_EN1	1	R/W	1'h0	Main-Link CRC mode select for Main-Link Lane1 0x0: Main-Link input stream does not have CRC data 0x1: Main-Link input stream has CRC data
0x1202	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_SP_EN1	1	R/W	1'h0	MIPI Short Packet mode select for Main-Link Lane1 0x0: Main-Link input stream does not have Short Packet 0x1: Short Packet is through from Main-Link input stream
0x1203	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VVALID_MODE1	1	R/W	1'h0	MIPI Frame Start & Frame End (FS/FE) mode select for Main-Link Lane1 0x0: FS/FE data are through from Main-Link input stream 0x1: FS/FE data are generated based on the timing of the VSYNC signal
0x1204	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VSYNC_POL1	1	R/W	1'h0	<this register is valid only when 0x1203[0]=0x1> Polarity setting of VSYNC signal to generate FS/FE for Main-Link Lane1 0x0: use Low pulse VSYNC signal (FE: Falling timing, FS: Rising timing) 0x1: use High pulse VSYNC signal (FE: Rising timing, FS: Falling timing)
0x1205	[7:0]	R_VX1_WC_LOW1	8	R/W	8'h00	<this register is valid only when 0x1200[0]=0x0> MIPI Packet Header's Word Count (LSB) manual setting for Main-Link Lane1
0x1206	[7:0]	R_VX1_WC_UP1	8	R/W	8'h00	<this register is valid only when 0x1200[0]=0x0> MIPI Packet Header's Word Count (MSB) manual setting for Main-Link Lane1
0x1207	[7:0]	R_VX1_DATAID1	8	R/W	8'h00	<this register is valid only when 0x1200[0]=0x0> MIPI Packet Header's Data ID manual setting for Main-Link Lane1 * use case setting example YUV422-8bit: 0x1E RGB888: 0x24 RAW8: 0x2A RAW10: 0x2B RAW12: 0x2C
0x1208	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_MASK_ECC1	1	R/W	1'h0	Masking and Ignoring both MIPI short packet and MIPI long packet when ECC double error is detected for Main-Link Lane1 0x0: Disable 0x1: Mask Processing when ECC double error is detected
0x1209	[7:1]	reserved	7	-	7'h00	-
	[0]	reservedL	1	R/W	1'h0	must be left 0x0 (default setting)
0x120A	[7:1]	reserved	7	-	7'h00	-
	[0]	R_CRC_ERR1	1	RC	1'h0	CRC error register for Main-Link Lane1 (clear the error status after reading register automatically) 0x0: no error 0x1: detect CRC error
0x120B	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_CRCT_ERR1	1	RC	1'h0	ECC single error register for Main-Link Lane1 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC single error
0x120C	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_DOUBLE_ERR1	1	RC	1'h0	ECC double error register for Main-Link Lane1 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC double error

Table 13. Header/Packet/Sync pre-processing setting for Main-Link (Lane2)

Address	bit	Register Name	width	R/W	Init	Description
0x1300	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_PH_EN2	1	R/W	1'h0	MIPI Packet Header mode select for Main-Link Lane2 0x0: Packet Header is generated by register settings 0x1: Packet Header is through from Main-Link input stream
0x1301	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_CRC_EN2	1	R/W	1'h0	Main-Link CRC mode select for Main-Link Lane2 0x0: Main-Link input stream does not have CRC data 0x1: Main-Link input stream has CRC data
0x1302	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_SP_EN2	1	R/W	1'h0	MIPI Short Packet mode select for Main-Link Lane2 0x0: Main-Link input stream does not have Short Packet 0x1: Short Packet is through from Main-Link input stream
0x1303	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VVALID_MODE2	1	R/W	1'h0	MIPI Frame Start & Frame End (FS/FE) mode select for Main-Link Lane2 0x0: FS/FE data are through from Main-Link input stream 0x1: FS/FE data are generated based on the timing of the VSYNC signal
0x1304	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VSYNC_POL2	1	R/W	1'h0	<this register is valid only when 0x1303[0]=0x1> Polarity setting of VSYNC signal to generate FS/FE for Main-Link Lane2 0x0: use Low pulse VSYNC signal (FE: Falling timing, FS: Rising timing) 0x1: use High pulse VSYNC signal (FE: Rising timing, FS: Falling timing)
0x1305	[7:0]	R_VX1_WC_LOW2	8	R/W	8'h00	<this register is valid only when 0x1300[0]=0x0> MIPI Packet Header's Word Count (LSB) manual setting for Main-Link Lane2
0x1306	[7:0]	R_VX1_WC_UP2	8	R/W	8'h00	<this register is valid only when 0x1300[0]=0x0> MIPI Packet Header's Word Count (MSB) manual setting for Main-Link Lane2
0x1307	[7:0]	R_VX1_DATAID2	8	R/W	8'h00	<this register is valid only when 0x1300[0]=0x0> MIPI Packet Header's Data ID manual setting for Main-Link Lane2 * use case setting example YUV422-8bit: 0x1E RGB888: 0x24 RAW8: 0x2A RAW10: 0x2B RAW12: 0x2C
0x1308	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_MASK_ECC2	1	R/W	1'h0	Masking and Ignoring both MIPI short packet and MIPI long packet when ECC double error is detected for Main-Link Lane2 0x0: Disable 0x1: Mask Processing when ECC double error is detected
0x1309	[7:1]	reserved	7	-	7'h00	-
	[0]	reservedL	1	R/W	1'h0	must be left 0x0 (default setting)
0x130A	[7:1]	reserved	7	-	7'h00	-
	[0]	R_CRC_ERR2	1	RC	1'h0	CRC error register for Main-Link Lane2 (clear the error status after reading register automatically) 0x0: no error 0x1: detect CRC error
0x130B	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_CRCT_ERR2	1	RC	1'h0	ECC single error register for Main-Link Lane2 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC single error
0x130C	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_DOUBLE_ERR2	1	RC	1'h0	ECC double error register for Main-Link Lane2 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC double error

Table 14. Header/Packet/Sync pre-processing setting for Main-Link (Lane3)

Address	bit	Register Name	width	R/W	Init	Description
0x1400	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_PH_EN3	1	R/W	1'h0	MIPI Packet Header mode select for Main-Link Lane3 0x0: Packet Header is generated by register settings 0x1: Packet Header is through from Main-Link input stream
0x1401	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_CRC_EN3	1	R/W	1'h0	Main-Link CRC mode select for Main-Link Lane3 0x0: Main-Link input stream does not have CRC data 0x1: Main-Link input stream has CRC data
0x1402	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_SP_EN3	1	R/W	1'h0	MIPI Short Packet mode select for Main-Link Lane3 0x0: Main-Link input stream does not have Short Packet 0x1: Short Packet is through from Main-Link input stream
0x1403	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VVALID_MODE3	1	R/W	1'h0	MIPI Frame Start & Frame End (FS/FE) mode select for Main-Link Lane3 0x0: FS/FE data are through from Main-Link input stream 0x1: FS/FE data are generated based on the timing of the VSYNC signal
0x1404	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VSYNC_POL3	1	R/W	1'h0	<this register is valid only when 0x1403[0]=0x1> Polarity setting of VSYNC signal to generate FS/FE for Main-Link Lane3 0x0: use Low pulse VSYNC signal (FE: Falling timing, FS: Rising timing) 0x1: use High pulse VSYNC signal (FE: Rising timing, FS: Falling timing)
0x1405	[7:0]	R_VX1_WC_LOW3	8	R/W	8'h00	<this register is valid only when 0x1400[0]=0x0> MIPI Packet Header's Word Count (LSB) manual setting for Main-Link Lane3
0x1406	[7:0]	R_VX1_WC_UP3	8	R/W	8'h00	<this register is valid only when 0x1400[0]=0x0> MIPI Packet Header's Word Count (MSB) manual setting for Main-Link Lane3
0x1407	[7:0]	R_VX1_DATAID3	8	R/W	8'h00	<this register is valid only when 0x1400[0]=0x0> MIPI Packet Header's Data ID manual setting for Main-Link Lane3 * use case setting example YUV422-8bit: 0x1E RGB888: 0x24 RAW8: 0x2A RAW10: 0x2B RAW12: 0x2C
0x1408	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_MASK_ECC3	1	R/W	1'h0	Masking and Ignoring both MIPI short packet and MIPI long packet when ECC double error is detected for Main-Link Lane3 0x0: Disable 0x1: Mask Processing when ECC double error is detected
0x1409	[7:1]	reserved	7	-	7'h00	-
	[0]	reservedL	1	R/W	1'h0	must be left 0x0 (default setting)
0x140A	[7:1]	reserved	7	-	7'h00	-
	[0]	R_CRC_ERR3	1	RC	1'h0	CRC error register for Main-Link Lane3 (clear the error status after reading register automatically) 0x0: no error 0x1: detect CRC error
0x140B	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_CRCT_ERR3	1	RC	1'h0	ECC single error register for Main-Link Lane3 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC single error
0x140C	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_DOUBLE_ERR3	1	RC	1'h0	ECC double error register for Main-Link Lane3 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC double error

6.5. MIPI Line Start/Line End code output setting

Both Line Start (LS) code and Line End (LE) code are optional code in MIPI CSI-2. When R_NONUSE_LSLE register is set 1'b1, both inputted LS and LE data are masked and ignored. On the other hands, when R_NONUSE_LSLE register is set 1'b0, both inputted LS and LE data are transmitted normally. For a system that do not use LS/LE code, R_NONUSE_LSLE_ register must be set 1'b1 to prevent unexpected behavior.

Table 15. MIPI Line Start and Line End code setting

Address	bit	Register Name	width	R/W	init	Description
0x1013	[7:1]	ReservedL	7	R/W	7'h00	must be left 0x00 (default setting)
	[0]	R_NONUSE_LSLE	1	R/W	1'h0	Line start and Line end code use or non-use setting for all Main-LInk lane 0x0: When a system is used mipi line start and line end, must be set 0x0 (*) 0x1: When a system is not use mipi line start and line end, must be set 0x1 (*) When 0x1013[0] = 0x0, 0x1606[1:0] must be set 0x3.

6.6. PLL setting reference

PLL setting is required. PLL setting set R_PLL_SETTING[47:0] is related with Main-Link data-rate.

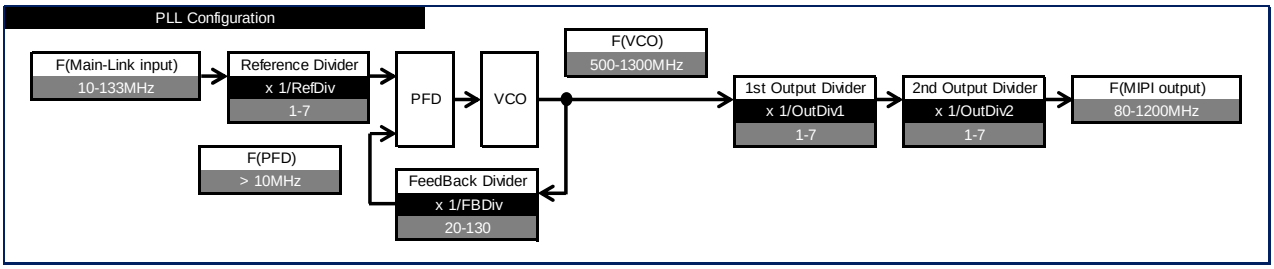


Figure 3. Reference clock supply basic method

PLL_SETTING[47:0] must be selected proper to meet below constraints.

Table 16. PLL constraints

symbol	description	min	typ	max	unit
F(IN)	PLL input pixel clock frequency	10	-	133	MHz
RefDiv	Reference Divider value	1	-	7	-
FBDiv	FeedBack Divider value	20	-	130	-
OutDiv1	1st Output Divider value (OutDiv1 must be >= OutDiv2)	1	-	7	-
OutDiv2	2nd Output Divider value (OutDiv1 must be >= OutDiv2)	1	-	7	-
F(PFD)	PFD frequency	10	-	-	MHz
F(VCO)	VCO frequency	500	-	1300	MHz
F(OUT)	PLL output pixel clock frequency	80	-	1200	MHz

Pixel clock frequency made by PLL is calculated as below.

[PCLK.input] = Pixel clock recovered on V-by-One® HS per lane = [F(Main-Link input)] = F(IN)

[F(Main-Link input)] = Main-Link data-rate per lane / (Byte mode x 8 x 10/8)

MIPI data-rate per lane (Mbps) = [F(MIPI output)] (MHz)

= MIPI High Speed mode data-rate per lane

$$F(VCO) = \frac{[F(Main\text{-}Link\ input)] \times [FBDiv]}{[RefDiv]}$$

$$[PCLK.output] = [F(MIPI\ output)] = \frac{[F(Main\text{-}Link\ input)] \times [FBDiv]}{[RefDiv] \times [OutDiv1] \times [OutDiv2]} = F(OUT)$$

$$\frac{[F(MIPI\ output)]}{[F(Main\text{-}Link\ input)]} = \frac{[FBDiv]}{[RefDiv] \times [OutDiv1] \times [OutDiv2]}$$

MIPI High Speed mode DDR output clock per lane = [F(MIPI output)] / 2 (MHz)

Table 17. PLL setting

Address	bit	Register Name	width	R/W	Init	Description
0x10 21	[7:0]	R_PLL_SETTING[47:40]	8	R/W	8'h0	PLL setting value, Feedback Divider value (integer part)
0x10 22	[7:3]	R_PLL_SETTING[39:35]	5	-	5'h0	PLL setting value (Must be set 0)
	[2:0]	R_PLL_SETTING[34:32]	3	R/W	3'h0	PLL setting value, Reference Divider value
0x10 23	[7]	R_PLL_SETTING[31]	1	-	1'h0	PLL setting value (Must be set 0)
	[6:4]	R_PLL_SETTING[30:28]	3	R/W	3'h0	PLL setting value, OutDiv1 (OutDiv1 must be >= OutDiv2)
	[3]	R_PLL_SETTING[27]	1	-	1'h0	PLL setting value (Must be set 0)
	[2:0]	R_PLL_SETTING[26:24]	3	R/W	3'h0	PLL setting value, OutDiv2 (OutDiv1 must be >= OutDiv2)
0x10 24	[7:0]	R_PLL_SETTING[23:16]	8	R/W	8'h0	PLL setting value, Feedback Divider value (decimal part MSB)
0x10 25	[7:0]	R_PLL_SETTING[15:8]	8	R/W	8'h0	PLL setting value, Feedback Divider value (decimal part)
0x10 26	[7:0]	R_PLL_SETTING[7:0]	8	R/W	8'h0	PLL setting value, Feedback Divider value (decimal part LSB)

PLL setting must fulfill below frequency ratio rule.

Table 18. PLL frequency ratio rule

Format	[F(MIPI output)] / [F(Main-Link input)] frequency ratio
MPRF	1*[Main-Link input lane#]*4*8 / [MIPI output lane#]
RGB888	3/4*[Main-Link input lane#]*4*8 / [MIPI output lane#]
YUV422 Normal	2/4*[Main-Link input lane#]*4*8 / [MIPI output lane#]
YUV422 Demux	1*[Main-Link input lane#]*4*8 / [MIPI output lane#]
RAW8 Normal	2/4*[Main-Link input lane#]*4*8 / [MIPI output lane#]
RAW8 Demux	1*[Main-Link input lane#]*4*8 / [MIPI output lane#]
RAW10 Normal	10/32*[Main-Link input lane#]*4*8 / [MIPI output lane#]
RAW10 Demux	20/32*[Main-Link input lane#]*4*8 / [MIPI output lane#]
RAW12 Normal	12/32*[Main-Link input lane#]*4*8 / [MIPI output lane#]
RAW12 Demux	24/32*[Main-Link input lane#]*4*8 / [MIPI output lane#]

Below Table is Look Up Table example for typical cases. (“PLL[*]” stands for “R_PLL_SETTING[*]”)

Table 19. PLL setting Look Up Table example

index	condition	Main-Link input	MIPI output	Distribution	F(MLINK in)	F(VCO)	F(MIPI out)	PLL[47:40]	PLL[39:32]	PLL[31:24]	PLL[23:16]	PLL[15:8]	PLL[7:0]
1	720p30fps RAW	742.5Mbps 1lane MPRF	594Mbps x1lane	off	18.5625	1188	594	0x40	0x01	0x21	0x00	0x00	0x00
3	720p30fps YUV422	750Mbps 1lane MPRF	600Mbps x1lane	off	18.75	1200	600	0x40	0x01	0x21	0x00	0x00	0x00
4	720p60fps RAW	1.114Gbps 1lane MPRF	445.5Mbps x2lane	off	27.84375	891	445.5	0x20	0x01	0x21	0x00	0x00	0x00
5	1080p30fps RAW			off	27.84375	891	445.5	0x20	0x01	0x21	0x00	0x00	0x00
6	720p60fps YUV422	1.485Gbps 1lane MPRF	594Mbps x2lane	off	37.125	1188	594	0x20	0x01	0x21	0x00	0x00	0x00
7	1080p30fps YUV422			off	37.125	1188	594	0x20	0x01	0x21	0x00	0x00	0x00
8	720p60fps YUV422	1.485Gbps 1lane MPRF	594Mbps x2lane x2	on	37.125	1188	594	0x20	0x01	0x21	0x00	0x00	0x00
9	720p120fps RAW	2.2275Gbps 1lane MPRF	891Mbps x2lane	off	55.6875	891	891	0x20	0x02	0x11	0x00	0x00	0x00
10	1080p60fps RAW			off	55.6875	891	891	0x20	0x02	0x11	0x00	0x00	0x00
11	720p120fps YUV422	2.97Gbps 1lane MPRF	594Mbps x4lane	off	74.25	1188	594	0x20	0x02	0x21	0x00	0x00	0x00
12	1080p60fps YUV422			off	74.25	1188	594	0x20	0x02	0x21	0x00	0x00	0x00
13	1080p120fps RAW	2.2275Gbps 2lane MPRF	891Mbps x4lane	off	55.6875	891	891	0x20	0x02	0x11	0x00	0x00	0x00
15	720p30fps RAW	990Mbps 1lane RAW12 Demux	594Mbps x1lane	off	24.75	594	594	0x18	0x01	0x11	0x00	0x00	0x00
17	720p30fps YUV422	1.6Gbps 1lane YUV422 Normal	640Mbps x1lane	off	40	640	640	0x20	0x02	0x11	0x00	0x00	0x00
18	720p60fps RAW	1.485Gbps 1lane RAW12 Demux	445.5Mbps x2lane	off	37.125	891	445.5	0x30	0x02	0x21	0x00	0x00	0x00
19	1080p30fps RAW			off	37.125	891	445.5	0x30	0x02	0x21	0x00	0x00	0x00
20	720p60fps YUV422	2.97Gbps 1lane YUV422 Normal	594Mbps x2lane	off	74.25	1188	594	0x20	0x02	0x21	0x00	0x00	0x00
21	1080p30fps YUV422			off	74.25	1188	594	0x20	0x02	0x21	0x00	0x00	0x00

For other example, 1080p30fps RAW8 1.5Gbps MPRF format Data stream handler Main-Link 4port (A/B/C/D) input / MIPI 2PORT2LANE (A+B / C+D) output can be available with PLL[47:40]='h20, PLL[34:32]='h01, PLL[30:28]='h1, PLL[26:24] ='h1.

6.7. Data stream handling

Setting of data stream handling can be configurable by 2-wire access to internal register.

Table 20. Data stream handler function mode setting

Address	bit	Register Name	width	R/W	Init	Description
0x1500	[7:2]	reserved	6	-	6'h00	-
	[1:0]	R_DSHNDLR_FUNC_MODE	2	R/W	2'h0	Main-Link Data Stream Handling function mode select 0x00: Data Stream Handling mode1 0x01: Data Stream Handling mode2 Others: Reserved
0x1501	[7:5]	reserved	3	-	3'h0	-
	[4:0]	R_MODE_NO	5	R/W	5'h00	Main-Link Data Stream Handling mode number

6.7.1. Data stream handling mode1

Data stream handling mode1 does not manage line memory and stream non-buffering streaming.

Video stream switch and copy/distribution can be achieved by this mode.

Table 21. Data stream handling mode1 setting

R_DSHNDLR_FUNC_MODE	R_MODE_NO	Main-Link Input				MIPI Output		Input port number	Distribution	Output port number	Output Swap
		port0	port1	port2	port3	port0	port1				
0x0	0x0	Cam A	-	-	-	Cam A		1	Off	1	-
	0x1	Cam A	-	-	-	Cam A	Cam A	1	On	2	-
	0x2	-	Cam B	-	-	Cam B		1	Off	1	-
	0x3	-	Cam B	-	-	Cam B	Cam B	1	On	2	-
	0x4	-	-	Cam C	-	Cam C		1	Off	1	-
	0x5	-	-	Cam C	-	Cam C	Cam C	1	On	2	-
	0x6	-	-	-	Cam D	Cam D		1	Off	1	-
	0x7	-	-	-	Cam D	Cam D	Cam D	1	On	2	-
	0x8	Cam A	Cam A	-	-	Cam A		1(2port)	Off	1	-
	0x9	-	-	Cam B	Cam B	Cam B		1(2port)	Off	1	-
	0xA	Cam A	Cam B	-	-	Cam A	Cam B	2	-	2	Off
	0xB	Cam A	Cam B	-	-	Cam B	Cam A	2	-	2	On

The MIPI data rates for MIPI Output port0 and port1 must be the same.

6.7.2. Data stream handling mode2

Data stream handling mode2 manage buffering of data stream with line memory. Output order is First-In-First-Out scheme. Virtual channel IDs of each Main-Link port can be re-numbered by 2-wire register control. RGB888 format is not supported on Data stream handling mode2.

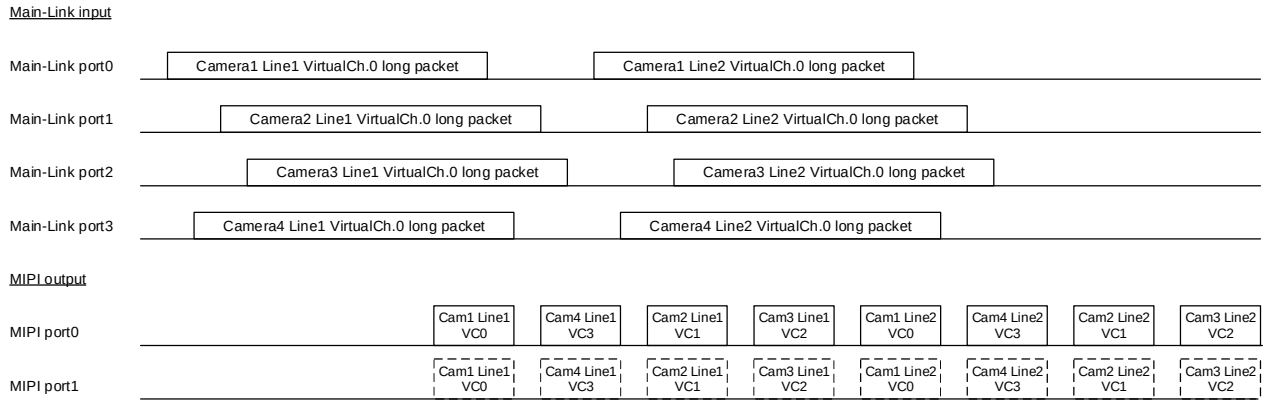


Figure 4. Data stream handling mode2 example 4port (A/B/C/D) input integration (A+B+C+D) output

Table 22. Data stream handling mode2 setting

R_DSHNDLR_FUNC_MODE	R_MODE_NO	Main-Link Input				MIPI Output		Input port number	Distribution	Output port number	Output Swap
		port0	port1	port2	port3	port0	port1				
0x1	0x00	Cam A	Cam B	-	-	A + B		2	Off	1	-
	0x01	Cam A	Cam B	-	-	A + B	A + B	2	On	2	-
	0x02	Cam A	Cam A	Cam C	-	A + C		2(3port)	Off	1	-
	0x03	Cam A	Cam A	Cam B	Cam B	A + B		2(4port)	Off	1	-
	0x04	Cam A	Cam B	Cam C	-	A + B + C		3	Off	1	-
	0x05	Cam A	Cam B	Cam C	-	A + B + C	A + B + C	3	On	2	-
	0x06	Cam A	Cam A	Cam C	Cam D	A + C + D		3(2port)	Off	1	-
	0x07	Cam A	Cam B	Cam C	-	B + C		3(2select)	Off	2	-
	0x08	Cam A	Cam B	Cam C	-	B + C	B + C	3(2select)	On	1	-
	0x09	Cam A	Cam B	Cam C	-	A + C		3(2select)	Off	2	-
	0x0A	Cam A	Cam B	Cam C	-	A + C	A + C	3(2select)	On	1	-
	0x0B	Cam A	Cam B	Cam C	Cam D	A+B+C+D		4	Off	1	-
	0x0C	Cam A	Cam B	Cam C	Cam D	A+B+C+D	A+B+C+D	4	On	2	-
	0x0D	Cam A	Cam B	Cam C	Cam D	A + D		4(2select)	Off	1	-
	0x0E	Cam A	Cam B	Cam C	Cam D	A + D	A + D	4(2select)	On	1	-
	0x0F	Cam A	Cam B	Cam C	Cam D	B + D		4(2select)	Off	1	-
	0x10	Cam A	Cam B	Cam C	Cam D	B + D	B + D	4(2select)	On	1	-
	0x11	Cam A	Cam B	Cam C	Cam D	C + D		4(2select)	Off	1	-
	0x12	Cam A	Cam B	Cam C	Cam D	C + D	C + D	4(2select)	On	1	-
	0x13	Cam A	Cam B	Cam C	-	A + B	C	3	-	2	Off
	0x14	Cam A	Cam B	Cam C	-	C	A + B	3	-	2	On
	0x15	Cam A	Cam B	Cam C	Cam D	A + B	C + D	4	-	2	Off
	0x16	Cam A	Cam B	Cam C	Cam D	C + D	A + B	4	-	2	On
	0x17	Cam A	Cam B	Cam C	Cam D	A + B + C	D	4	-	2	Off
	0x18	Cam A	Cam B	Cam C	Cam D	D	A + B + C	4	-	2	On

In case of Data stream handling mode2, Virtual Channel ID on each V-by-One® HS input lanes are recognized and re-numbering according to register setting into integrated interleaved MIPI output stream.

Table 23. Data stream handling mode2 Virtual channel renumbering setting

Address	bit	Register Name	width	R/W	Init	Description
0x150B	[7:0]	R_MODE2_VC_REQCTRL0	8	R/W	8'hE4	<this register is valid only when 0x1500[1:0]=0x1> renumbering Virtual Channel (VC) for Lane0 [7:6] exchanging VC number from inputted VC3 [5:4] exchanging VC number from inputted VC2 [3:2] exchanging VC number from inputted VC1 [1:0] exchanging VC number from inputted VC0
0x150C	[7:0]	R_MODE2_VC_REQCTRL1	8	R/W	8'hE4	<this register is valid only when 0x1500[1:0]=0x1> renumbering Virtual Channel (VC) for Lane1 [7:6] exchanging VC number from inputted VC3 [5:4] exchanging VC number from inputted VC2 [3:2] exchanging VC number from inputted VC1 [1:0] exchanging VC number from inputted VC0
0x150D	[7:0]	R_MODE2_VC_REQCTRL2	8	R/W	8'hE4	<this register is valid only when 0x1500[1:0]=0x1> renumbering Virtual Channel (VC) for Lane2 [7:6] exchanging VC number from inputted VC3 [5:4] exchanging VC number from inputted VC2 [3:2] exchanging VC number from inputted VC1 [1:0] exchanging VC number from inputted VC0
0x150E	[7:0]	R_MODE2_VC_REQCTRL3	8	R/W	8'hE4	<this register is valid only when 0x1500[1:0]=0x1> renumbering Virtual Channel (VC) for Lane3 [7:6] exchanging VC number from inputted VC3 [5:4] exchanging VC number from inputted VC2 [3:2] exchanging VC number from inputted VC1 [1:0] exchanging VC number from inputted VC0

6.8. MIPI Virtual Channel

When MIPI PH (Packet Header) is intake from V-by-One® HS on Data stream handling mode1, MIPI Virtual Channel information in PH is also bridged from V-by-One® HS at the same time.

On the other hands with Data stream handling mode2, Virtual Channel information on each V-by-One® HS input lanes are recognized and re-labeled according to register setting into integrated interleaved MIPI output stream.

6.9. MIPI output setting

Setting of MIPI output can be configurable by 2-wire access to internal register.

Table 24. MIPI output setting (1/3)

Address	bit	Register Name	width	R/W	Init	Description
0x1600	[7:5]	Reserved	3	-	3'h0	-
	[4:0]	R_ANALOG	5	R/W	5'h00	[4] MIPI Power Down 0x0: Power Down 0x1: Normal operation [3] MIPI Soft Reset 0x0: Reset 0x1: Normal operation [2] ReservedL (must be set 0x0) [1] ReservedH (must be set 0x1) [0] ReservedL (must be set 0x0)
0x1601	[7:0]	ReservedX	8	R/W	8'h1B	must be left as default 0x1B
0x1602	[7:0]	R_TX_LANE_SEL0	8	R/W	8'hE4	MIPI Tx Lane assignment select (*each bit setting) [7:6] MTX3P/N (MTX3) (*) [5:4] MTX2P/N (MTX2) (*) [3:2] MTX1P/N (MTX1) (*) [1:0] MTX0P/N (MTX0) (*) 0x0: 1st Byte output 0x1: 2nd Byte output 0x2: 3rd Byte output (or 1st Byte on 2PORT mode) 0x3: 4th Byte output (or 2nd Byte on 2PORT mode) * use case setting example 1PORT1LANE: 0xE4 (Port0:MTX0) 1PORT2LANE: 0xE4 (Port0:MTX0, MTX1) 1PORT4LANE: 0xE4 (Port0:MTX0, MTX1, MTX2, MTX3) 2PORT1LANE: 0x72 (Port0:MTX1, Port1:MTX0) 0x63 (Port0:MTX1, Port1:MTX2) 0x36 (Port0:MTX3, Port1:MTX0) 2PORT2LANE: 0x72 (Port0:MTX3,MTX1, Port1:MTX0,MTX2)
0x1603	[7:2]	Reserved	6	-	6'h00	-
	[1:0]	R_TX_LANE_SEL1	2	R/W	2'h0	<this register is valid when 0x1605[2:0]=0x4 or 0x5> MIPI Tx Lane assignment select for Port1 on 2PORT mode * use case setting example 2PORT1LANE: 0x0 (Port1:MTX0) 2PORT1LANE: 0x2 (Port1:MTX2) 2PORT2LANE: 0x0 (Port1:MTX0,MTX2)
0x1604	[7:0]	ReservedX	8	R/W	8'h3F	must be left as default 0x3F

Table 25. MIPI output setting (2/3)

Address	bit	Register Name	width	R/W	Init	Description
0x1605	[7]	Reserved	1	-	1'h0	-
	[6:0]	R_LANE_EN	7	R/W	7'h2B	[6:5] MIPI Data lane Enable (*each bit setting) [6] Data Port1 (*) [5] Data Port0 (*) 0x0: OFF 0x1: ON [4:3] MIPI CLK lane Enable (*each bit setting) [4] CLK Port1 (*) [3] CLK Port0 (*) 0x0: OFF 0x1: ON [2:0] MIPI Configuration 0x0 (=0b000): 1PORT1LANE 0x1 (=0b001): 1PORT2LANE 0x3 (=0b011): 1PORT4LANE 0x4 (=0b100): 2PORT1LANE 0x5 (=0b101): 2PORT2LANE Other:Reserved * use case setting example 1PORT1LANE: 0x28 (=0b0101_000) 1PORT2LANE: 0x29 (=0b0101_001) 1PORT4LANE: 0x2B (=0b0101_011) 2PORT1LANE: 0x7C (=0b1111_100) 2PORT2LANE: 0x7D (=0b1111_101)
0x1606	[7:2]	ReservedX	6	R/W	6'h10	must be set 0x13
	[1:0]	R_MODE_SET	2	R/W	2'h0	clock continous mode select (*each bit setting) [1] clock continous mode select for Port1 (*) [0] clock continous mode select for Port0 (*) 0x0:OFF (HS clock off and become LP mode during V-Blanking term) 0x1:ON (HS clock permanently on) (*) When 0x1013[0] = 0x0, 0x1606[1:0] must be set 0x3.
0x1607	[7:0]	ReservedX	8	R/W	8'hE4	must be left 0xE4 (default setting)
0x1608	[7:4]	Reserved	4	-	4'h0	-
	[3:0]	ReservedX	4	R/W	4'hE	must be left 0xE (default setting)
0x161f	[7:4]	Reserved	4	-	4'h0	-
	[3:0]	R_REQ_SEL	4	R/W	4'h0	MIPI Tx Lane Port assignment (*each bit setting) [3] MTX3P/N (MTX3) (*) [2] MTX2P/N (MTX2) (*) [1] MTX1P/N (MTX1) (*) [0] MTX0P/N (MTX0) (*) 0: Port0 1: Port1 * use case setting example 1PORT mode: 0x0 (=0b0000) 2PORT mode: 0x5 (=0b0101) (Port0:MTX3,MTX1, Port1:MTX0,MTX2)

Table 26. MIPI output setting (3/3)

Address	bit	Register Name	width	R/W	Init	Description
0x1609	[7:0]	R_TX_CLK_PREPARE0	8	R/W	8'h04	CLK lane Prepare period setting Port0 Adjustable delay value in units of "8 × tTBIT × R_TX_CLK_PREPARE0"
0x160a	[7:0]	R_TX_CLK_ZERO0	8	R/W	8'h1D	CLK lane ZERO period setting Port0 Adjustable delay value in units of "8 × tTBIT × R_TX_CLK_ZERO0"
0x160b	[7:0]	R_TX_CLK_TRAIL0	8	R/W	8'h07	CLK lane TRAIL period setting Port0 Adjustable delay value in units of "8 × tTBIT × R_TX_CLK_TRAIL0"
0x160c	[7:0]	reservedX	8	R/W	8'h02	must be left 0x2 (default setting)
0x160d	[7:0]	R_TX_CLK_POST0	8	R/W	8'h0C	CLK lane POST period setting Port0 Adjustable delay value in units of "8 × tTBIT × R_TX_CLK_POST0"
0x160e	[7:0]	R_TX_THS_EXIT0	8	R/W	8'h0B	CLK and Data lane EXIT period setting Port0 Adjustable delay value in units of "8 × tTBIT × R_TX_THS_EXIT0"
0x160f	[7:0]	R_TX_TLPX0	8	R/W	8'h05	CLK and Data lane TLPX period setting Port0 Adjustable delay value in units of "8 × tTBIT × R_TX_TLPX0"
0x1610	[7:0]	R_TX_THS_PREPARE0	8	R/W	8'h04	Data lane Prepare period setting Port0 Adjustable delay value in units of "8 × tTBIT × R_TX_THS_PREPARE0"
0x1611	[7:0]	R_TX_THS_ZERO0	8	R/W	8'h10	Data lane ZERO period setting Port0 Adjustable delay value in units of "8 × tTBIT × R_TX_THS_ZERO0"
0x1612	[7:0]	R_TX_THS_TRAIL0	8	R/W	8'h07	Data lane TRAIL period setting Port0 Adjustable delay value in units of "8 × tTBIT × R_TX_THS_TRAIL0"
0x1613	[7:0]	reservedX	8	R/W	8'h40	must be left 0x40 (default setting)
0x1614	[7:0]	R_TX_CLK_PREPARE1	8	R/W	8'h04	CLK lane Prepare period setting Port1 Adjustable delay value in units of "8 × tTBIT × R_TX_CLK_PREPARE1"
0x1615	[7:0]	R_TX_CLK_ZERO1	8	R/W	8'h1D	CLK lane ZERO period setting Port1 Adjustable delay value in units of "8 × tTBIT × R_TX_CLK_ZERO1"
0x1616	[7:0]	R_TX_CLK_TRAIL1	8	R/W	8'h07	CLK lane TRAIL period setting Port1 Adjustable delay value in units of "8 × tTBIT × R_TX_CLK_TRAIL1"
0x1617	[7:0]	reservedX	8	R/W	8'h02	must be left 0x2 (default setting)
0x1618	[7:0]	R_TX_CLK_POST1	8	R/W	8'h0C	CLK lane POST period setting Port1 Adjustable delay value in units of "8 × tTBIT × R_TX_CLK_POST1"
0x1619	[7:0]	R_TX_THS_EXIT1	8	R/W	8'h0B	CLK and Data lane EXIT period setting Port1 Adjustable delay value in units of "8 × tTBIT × R_TX_THS_EXIT1"
0x161a	[7:0]	R_TX_TLPX1	8	R/W	8'h05	CLK and Data lane TLPX period setting Port1 Adjustable delay value in units of "8 × tTBIT × R_TX_TLPX1"
0x161b	[7:0]	R_TX_THS_PREPARE1	8	R/W	8'h04	Data lane Prepare period setting Port1 Adjustable delay value in units of "8 × tTBIT × R_TX_THS_PREPARE1"
0x161c	[7:0]	R_TX_THS_ZERO1	8	R/W	8'h10	Data lane ZERO period setting Port1 Adjustable delay value in units of "8 × tTBIT × R_TX_THS_ZERO1"
0x161d	[7:0]	R_TX_THS_TRAIL1	8	R/W	8'h07	Data lane TRAIL period setting Port1 Adjustable delay value in units of "8 × tTBIT × R_TX_THS_TRAIL1"
0x161e	[7:0]	reservedX	8	R/W	8'h40	must be left 0x40 (default setting)

MTX0P/N and MTX2P/N can be assigned to be MIPI 2nd port (port1).

The frequency of MIPI 2nd port clock lane is the same as that of MIPI 1st port clock lane.

The MIPI clock frequency output from MTXCLK0 and MTXCLK1 is the same frequency. It is not possible to output a different frequency.

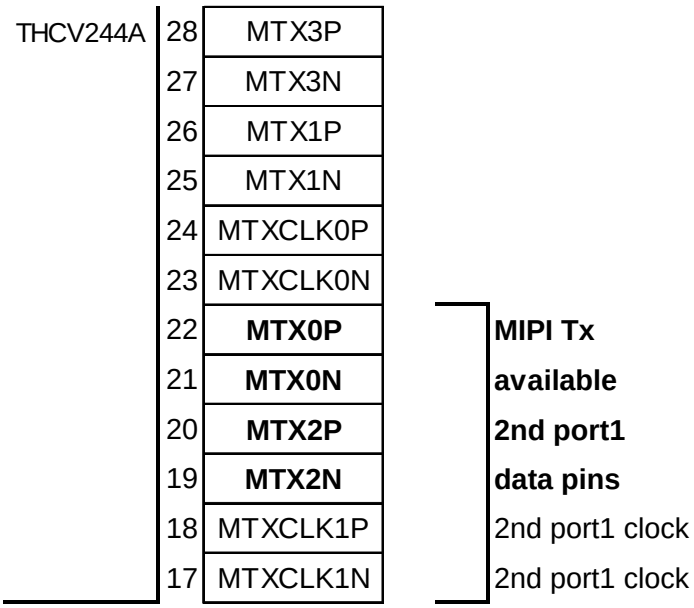


Figure 5. MIPI 2nd port available pins

Setting of MIPI 2port output examples are shown below.

Table 27. MIPI 2port output setting example

R_TX_LANE_SEL0				R_TX_LANE_SEL1	R_LANE_EN			R_REQ_SEL				MIPI Physical pin order output assignment					
lane3	lane2	lane1	lane0	port1 select	port enable	clk enable	config	lane3	lane2	lane1	lane0	lane3	lane1		lane0	lane2	
[7:6]	[5:4]	[3:2]	[1:0]	[1:0]	[6:5]	[4:3]	[2:0]	[3]	[2]	[1]	[0]	MTX3P/N	MTX1P/N	MTXCLK0P/N	MTX0P/N	MTX2P/N	MTXCLK1P/N
01	11	00	10	00	11	11	101	0	1	0	1	port0 2nd Byte	port0 1st Byte	port0 clock	port1 1st Byte	port1 2nd Byte	port1 clock
01	10	00	11	10	11	11	101	0	1	0	1	port0 2nd Byte	port0 1st Byte	port0 clock	port1 2nd Byte	port1 1st Byte	port1 clock
00	11	01	10	00	11	11	101	0	1	0	1	port0 1st Byte	port0 2nd Byte	port0 clock	port1 1st Byte	port1 2nd Byte	port1 clock
01	11	00	10	00	11	11	100	0	1	0	1	No output	port0 1st Byte	port0 clock	port1 1st Byte	No output	port1 clock
01	10	00	11	10	11	11	100	0	1	0	1	No output	port0 1st Byte	port0 clock	No output	port1 1st Byte	port1 clock
00	11	01	10	00	11	11	100	0	1	0	1	port0 1st Byte	No output	port0 clock	port1 1st Byte	No output	port1 clock
other settings												forbidden					

6.10. 2-wire serial interface

6.10.1. 2-wire serial I/F slave Device ID

To use GPIO (General Purpose Input/Output), fault/error detection, and interrupt function, 2-wire serial I/F enables to access registers. AIN<1:0> pin determines 2-wire slave Device ID setting.

Table 28. 2-wire serial I/F Device ID select by AIN pin

Pin Name	Description
AIN1	Device Address Setting for 2-wire Serial Interface [AIN1:AIN0]=00: ID=7'h0B [AIN1:AIN0]=01: ID=7'h34 [AIN1:AIN0]=10: ID=7'h77 [AIN1:AIN0]=11: ID=7'h65
AIN0	

As an additional method, 2-wire slave Device ID setting can be changed from default value by register setting.

Table 29. 2-wire serial I/F Device ID select by register setting

Address	bit	Register Name	width	R/W	Init	Description
0x0030	[7:0]	R_2WIRE_SADR	8	RW	8'h00	2-wire slave device address setting [7] 2-wire slave device address control 0x0: 2-wire slave device addr. is set by AIN1 and AIN0 pin 0x1: 2-wire slave device addr. is set by following register [6:0] <this regiseter is valid when 0x0030[1:0]=0x1> [6:0] 2-wire slave device address value for register control

6.10.2. 2-wire serial Read/Write access to local Register

HOST MPU can directly access THCV244A local register by 2-wire serial I/F.

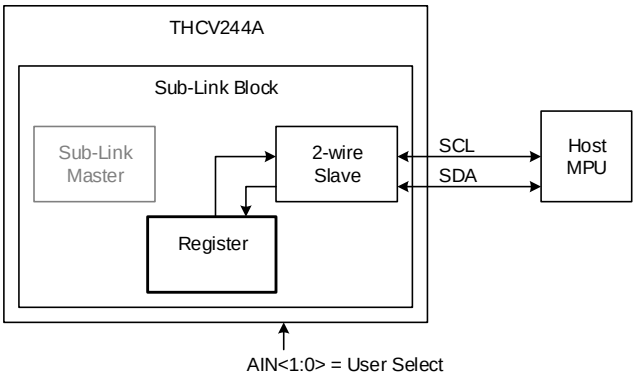


Figure 6. Host to THCV244A local register access configuration

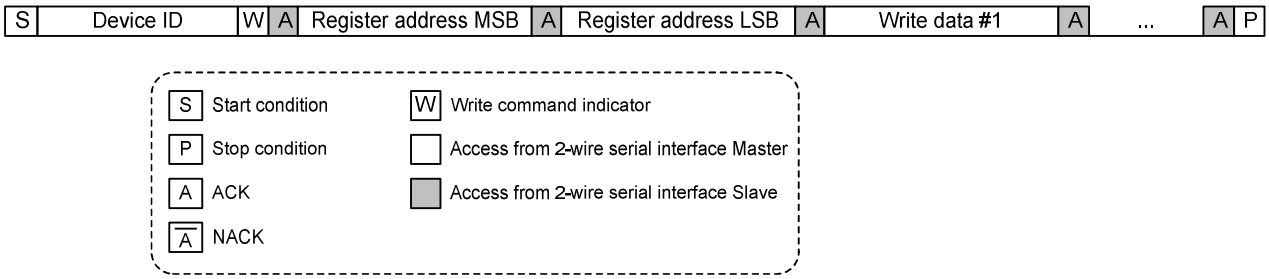


Figure 7. 2-wire serial I/F write to THCV244A local register protocol

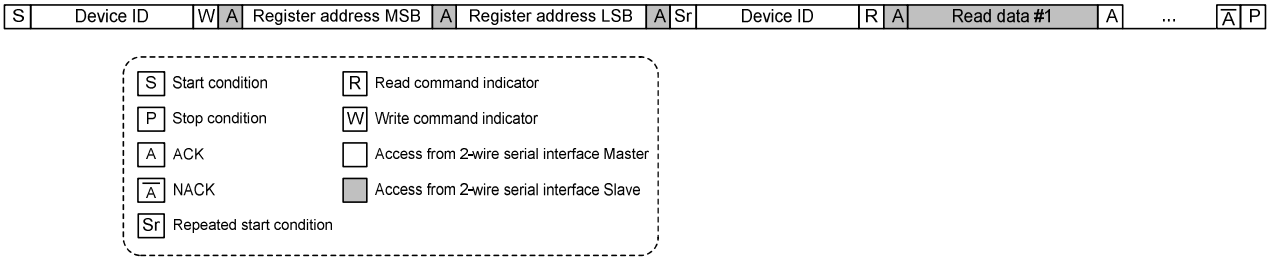


Figure 8. 2-wire serial I/F read to THCV244A local register protocol

6.11. 2-wire serial I/F Watch Dog Timer

2-wire Watch Dog Timer (WDT) is installed to monitor status.

Table 30. 2-wire WDT setting

Address	bit	Register Name	width	R/W	Init	Description
0x003B	[7:5]	reserved	3	-	-	-
	[4]	R_2WIRE_WD_EN	1	RW	1'h1	2-wire I/F Watch Dog Timer (WDT) Enable 0x0: Disable 0x1: Enable
	[3:1]	reserved	3	-	-	-
	[0]	R_2WIRE_WD_OFFSET	1	RW	1'h1	<this register is valid only when 0x003B[4]=0x1> 2-wire I/F WDT Offset Time 0x1: 0x7FF (=d2047) 0x0: 0x3FF (=d1023)
0x003C	[7:0]	R_2WIRE_WD_TIM	8	RW	8'hFF	<this register is valid only when 0x003B[4]=0x1> 2-wire I/F WDT time =64×{R_2WIRE_WD_TIM<7:0>+1}×{2WIRE_WDT_OffsetTime}×tOSC

6.12. Register Auto Checksum diagnosis

Register values checksum is continuously calculated as R_CKSUM_RVAL.

Table 31. Register Auto Checksum diagnosis control and monitoring

Address	bit	Register Name	width	R/W	Init	Description
0x0008	[7:1]	reserved	7	-	-	-
	[0]	R_CKSUM_EN	1	RW	1'h0	Internal Register AutoCheckSum Enable 0x0: Disable 0x1: Enable
0x0009	[7:0]	R_CKSUM_TIM	8	RW	8'h13	<this regiseters is valid only when 0x0008[0]=0x1> Internal Register AutoCheckSum check interval =1024×64×(R_CKSUM_TIM<7:0>+1) × tOSC
0x000A	[7:0]	R_CKSUM_VAL	8	RW	8'h00	<this regiseters is valid only when 0x0008[0]=0x1> Internal Register AutoCheckSum expected target value
0x000B	[7:0]	R_CKSUM_RVAL	8	R	-	<this regiseters is valid only when 0x0008[0]=0x1> Internal Register AutoCheckSum read value

6.13. Sub-Link setting

THCV244A is Sub-Link Master and connectable to Sub-Link Slave device such as THCV241A.

Sub-Link Polling interval is controllable from about 20us to 800us, that may have relationships on fault/error detection, interrupt, or other GPIO transfer time designed on application. SSR (Sub-Link Status Read) interval determines recovery quickness from 2-wire serial remote communication completion.

Table 32. Sub-Link Master protocol basic setting

0x0004	[7:3]	reserved	5	-	-	-
	[2:0]	R_SLINK_MODE	3	RW	3'h1	Sub-Link basic protocol setting as Sub-Link Master 0x1: 2-wire Set & Trigger mode1 0x3: 2-wire Pass Through mode1 Other: Reserved
0x0010	[7:4]	R_SLINK_EN	4	RW	4'h0	Sub-Link Enable (*each bit setting) [7] Sub-Link Enable for Lane3 (*) [6] Sub-Link Enable for Lane2 (*) [5] Sub-Link Enable for Lane1 (*) [4] Sub-Link Enable for Lane0 (*) 0x0: Sub-Link Disable 0x1: Sub-Link Enable
	[3:0]	R_SLINK_POL_EN	4	RW	4'hF	Sub-Link Polling Enable (*each bit setting) [3] Sub-Link Polling Enable for Lane3 (*) [2] Sub-Link Polling Enable for Lane2 (*) [1] Sub-Link Polling Enable for Lane1 (*) [0] Sub-Link Polling Enable for Lane0 (*) 0x0: Polling Disable 0x1: Polling Enable
0x0011	[7:4]	reservedX	4	RW	4'hF	must be left 0xF (default setting)
	[3:0]	R_SLINK_WD_EN	4	RW	4'hF	Sub-Link Watch Dog Timer (WDT) Enable (*each bit setting) [3] Sub-Link WDT Enable for Lane3 (*) [2] Sub-Link WDT Enable for Lane2 (*) [1] Sub-Link WDT Enable for Lane1 (*) [0] Sub-Link WDT Enable for Lane0 (*) 0x0: WDT Disable 0x1: WDT Enable
0x001A	[7:5]	reserved	3	-	-	-
	[4]	R_SLINK_POL_OFSET_EN	1	RW	1'h0	<this regiseter is valid when 0x0010[*n*]=0x1, *n*=0,1,2,3> Enable of shifting the Sub-Link Polling output timing 0x0: Disable 0x1: Enable The Polling output timing of Sub-Link Lane1 is delayed by Sub-Link Polling interval x 1/4 from the Sub-Link Lane0. Lane2 is delayed by Sub-Link Polling interval x 2/4 from the Sub-Link Lane0. Lane3 is delayed by Sub-Link Polling interval x 3/4 from the Sub-Link Lane0.
	[3:2]	reserved	2	-	-	-
	[1:0]	R_SLINK_POL_TIM_UP	2	RW	2'h0	<this regiseter is valid when 0x0010[*n*]=0x1, *n*=0,1,2,3> Sub-Link Polling interval setting (min. 0x018, about 20us)
0x001B	[7:0]	R_SLINK_POL_TIM_DN	8	RW	8'h7C	<this regiseter is valid when 0x0010[*n*]=0x1, *n*=0,1,2,3> Sub-Link Polling interval time=64×(256×R_SLINK_POL_TIM_UP<1:0> +R_SLINK_POL_TIM_DN<7:0>+1)×tOSC *No Polling when R_SLINK_POL_TIM_UP=0x0 and R_SLINK_POL_TIM_DN=0x0
0x001C	[7:2]	reserved	6	-	-	-
	[1:0]	R_SLINK_SSR_TIM_UP	2	RW	2'h0	Sub-Link SSR interval setting
0x001D	[7:0]	R_SLINK_SSR_TIM_DN	8	RW	8'hF9	Sub-Link SSR interval time=64×(256×R_SLINK_SSR_TIM_UP<1:0> +R_SLINK_SSR_TIM_DN<7:0>+1)×tOSC *No SSR when R_SLINK_SSR_TIM_UP=0x0 and R_SLINK_SSR_TIM_DN=0x0

To use GPIO (General Purpose Input/Output) pin, fault/error detection and interrupt function, “2-wire Set&Trigger mode1” and “2-wire Pass Through mode1” enables remote register access. THCV244A, Sub-Link Master device has 2-wire serial slave block and can connect to HOST MPU. On the other hand, the counterpart Sub-Link Slave device has 2-wire serial master block and can connect to remote side 2-wire serial slave devices.

HOST MPU can access register of Sub-Link Master device, Sub-Link Slave device and remote side 2-wire serial slave devices.

6.13.1. Sub-Link 2-wire Set and Trigger mode (2-wire Normal mode)

HOST MPU can access to Sub-Link Slave’s register via THCV244A as Sub-Link Master only by THCV244A internal local register control and monitoring on 2-wire Set&Trigger mode1.

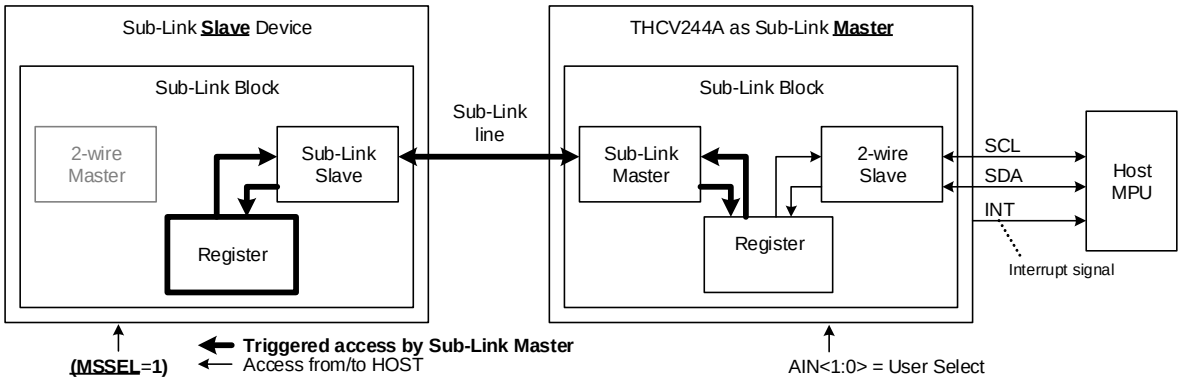


Figure 9. Host MPU to Sub-Link Slave Register via THCV244A access configuration

HOST MPU can access to remote side 2-wire serial slave register via THCV244A as Sub-Link Master only by THCV244A internal local register control and monitoring on 2-wire Set&Trigger mode1.

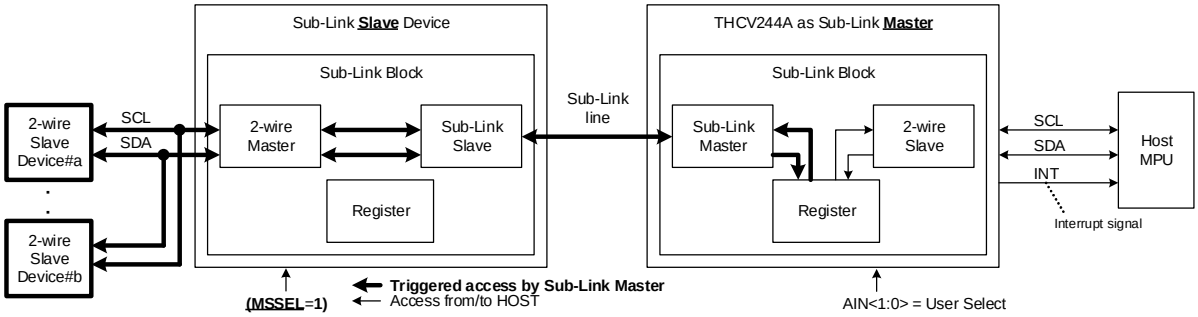


Figure 10. Host MPU to remote 2-wire slave devices via THCV244A access configuration

In principle, when Sub-Link bridges 2-wire serial interface communication from Sub-Link Master to Sub-Link Slave or remote side 2-wire serial slave devices, time lag occurs between HOST MPU side 2-wire serial access and Sub-Link Slave internal bus access or remote side 2-wire serial access.

R_2WIRE_CLKSEN (Sub-Link Master side register, 0x00E2 bit0) selects whether 2-wire serial slave of Sub-Link Master perform clock stretching.

When R_2WIRE_CLKSEN = 1, Sub-Link Master device waits HOST MPU until Sub-Link Slave register access or remote side 2-wire serial slave register access complete by clock stretching.

When R_2WIRE_CLKSEN = 0, Sub-Link Master device informs HOST MPU that Sub-Link Slave register access or remote side 2-wire serial register access has completed by interruption (detectable on INT pin) without clock stretching.

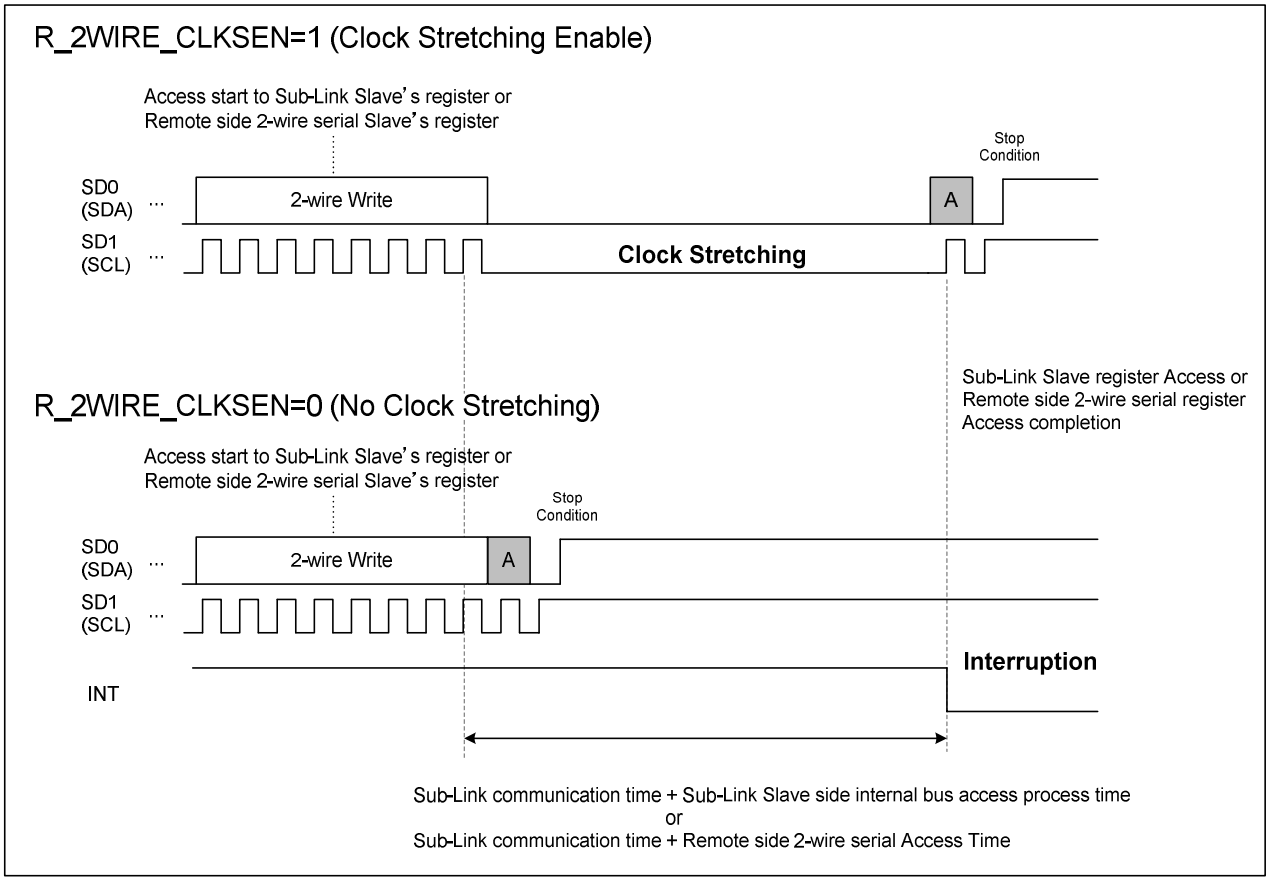


Figure 11. Sub-Link Master 2-wire slave clock stretching operation

Table 33. 2-wire serial I/F Set& Trigger mode remote access control and monitoring local registers (1/2)

Address	bit	Register Name	width	R/W	Init	Description
0x00D0	[7:0]	R_2WIRE_DATA0	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #0
0x00D1	[7:0]	R_2WIRE_DATA1	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #1
0x00D2	[7:0]	R_2WIRE_DATA2	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #2
0x00D3	[7:0]	R_2WIRE_DATA3	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #3
0x00D4	[7:0]	R_2WIRE_DATA4	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #4
0x00D5	[7:0]	R_2WIRE_DATA5	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #5
0x00D6	[7:0]	R_2WIRE_DATA6	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #6
0x00D7	[7:0]	R_2WIRE_DATA7	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #7
0x00D8	[7:0]	R_2WIRE_DATA8	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #8
0x00D9	[7:0]	R_2WIRE_DATA9	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #9
0x00DA	[7:0]	R_2WIRE_DATA10	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #10
0x00DB	[7:0]	R_2WIRE_DATA11	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #11
0x00DC	[7:0]	R_2WIRE_DATA12	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #12
0x00DD	[7:0]	R_2WIRE_DATA13	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #13
0x00DE	[7:0]	R_2WIRE_DATA14	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #14
0x00DF	[7:0]	R_2WIRE_DATA15	8	RW	8'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #15
0x00E0	[7:1]	R_2WIRE_DEVADR	7	RW	7'h00	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote access target device address. if target addr. = self addr.; access to Sub-Link slave internal registers, else; access to remote side 2-wire serial slave devices externally connected to Sub-Link slave
	[0]	R_2WIRE_WR	1	RW	1'h0	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote access write or read select 0x0: Write 0x1: Read
0x00E1	[7]	reserved	1	-	-	-
	[6:4]	R_2WIRE_WADR_BYTE	3	RW	3'h0	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote device's sub address (Word Address, register address) Byte width. Sub Address Byte width = R_2WIRE_WADR_BYTE<2:0>+1 0x0: 1Byte (= 8bit) sub address 0x1: 2Byte (=16bit) sub address Other : Reserved
	[3:0]	R_2WIRE_DATA_BYTE	4	RW	4'h0	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote access data Byte number. Byte Number = R_2WIRE_DATA_BYTE + 1 (e.g. 0x2 for 3Byte burst) [Write rule] R_2WIRE_WADR_BYTE+R_2WIRE_DATA_BYTE < 'd16 [Read rule] R_2WIRE_DATA_BYTE < 'd16

Table 34. 2-wire serial I/F Set& Trigger mode remote access control and monitoring local registers (2/2)

Address	bit	Register Name	width	R/W	Init	Description
0x00E2	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_CLKSEN	1	RW	1'h0	<this regiseter is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F local response clock stretching Enable 0x0: Sub-Link Master (2-wire slave) No clock stretching 0x1: Sub-Link Master (2-wire slave) clock stretching Enable *2-wire Pass Through mode (R_SLINK_MODE=0x3) forces clock stretching Enable
0x00E3	[7:2]	reserved	6	-	-	-
	[1:0]	R_2WIRE_RD_LANE_SEL	2	RW	2'h0	<this regiseter is valid when 0x0004[2:0]=0x1 or 0x3> Sub-Link read transaction lane select 0x0: Read from Sub-Link Lane0 0x1: Read from Sub-Link Lane1 0x2: Read from Sub-Link Lane2 0x3: Read from Sub-Link Lane3
0x00E4	[7:4]	reserved	4	-	-	-
	[3:0]	R_2WIRE_WR_LANE_SEL	4	RW	4'hF	<this regiseter is valid only when 0x0004[2:0]=0x1> Sub-Link Write transaction lane select (multiple lanes can be written at the same time) (*each bit setting) [3] Write for Sub-Link Lane3 (*) [2] Write for Sub-Link Lane2 (*) [1] Write for Sub-Link Lane1 (*) [0] Write for Sub-Link Lane0 (*) 0x0: Disable 0x1: Enable
0x00E5	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_START	1	W	-	<this regiseter is valid only when 0x0004[2:0]=0x1> 0x1: 2-wire serial I/F remote access start trigger

6.13.2. Sub-Link 2-wire Pass Through mode

Sub-Link Master 2-wire Pass Through mode1 can bridge original local 2-wire commands to remote side.

2-wire Pass Through mode1 uses 2-wire slave clock stretching scheme at local Sub-Link Master side. Host MCU 2-wire master must be no problem with clock stretching wait from 2-wire slave.

Sub-Link Slave side processing protocol “Divided write/read” scheme divides 2-wire commands into determined data Byte groups. Each data Byte groups are sent separately on remote side. Burst write/read access target Sub-Address (Word-Address) is interpreted so that subsequent Sub-Address (Word-Address) from 2nd group is automatically and properly incremented. As shown below, remote side 2-wire accesses are independent each other by determined Byte, which are defined in R_2WIREPT_WA_BYTE and R_2WIREPT_DATA_BYTE at R_2WIREPT1_PASS_MODE[1]=1.

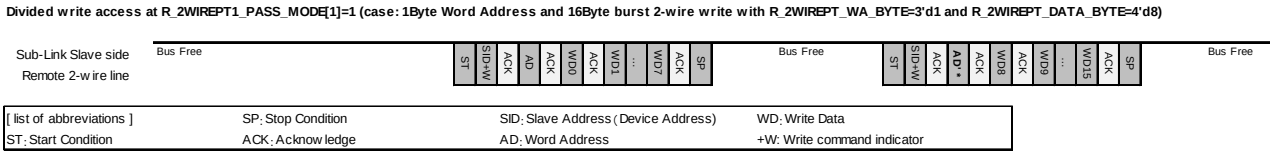


Figure 12. 2-wire Pass Through mode1 Sub-Link Slave command Divided scheme

On address processing protocol “Assigned address & rename”, THCV244A 2-wire slave respond only to 2-wire device address defined in R_2WIREPT1_PASS_ADRxy1 (x=Lane0/1/2/3, y=0/1/2/3) for remote Pass Through operation. Otherwise, 2-wire commands are ignored except THCV244A itself address. The device address can be renamed before remote send. The counterpart Sub-Link Slave internal register access is available with R_2WIREPT1_PASS_ADRINx (x=Lane0/1/2/3) setting.

On address processing protocol “All Through”, THCV244A 2-wire slave respond basically all 2-wire device address for remote Pass Through operation except THCV244A itself address. Additionally, Defined addresses in R_2WIREPT2_NOPASS_ADRxz (x=Lane0/1/2/3, z=0/1/2/3/4/5/6/7) can be ignored by THCV244A.

Table 35. 2-wire serial I/F Pass Through mode remote access common setting

Address	bit	Register Name	width	R/W	Init	Description
0x0031	[7:2]	reserved	6	-	-	-
	[1:0]	R_2WIREPT_MODE	2	RW	2'h0	<this regiseter is valid only when 0x0004[2:0]=0x3> Sub-Link 2WIRE Pass Through mode setting [1]Pass Through processing protocol on Sub-Link Slave 0x0: Reserved 0x1: Divided Write & Divided Read Transaction address and data Byte number are set as R_2WIREPT_WA_BYTE and R_2WIREPT_DATA_BYTE. [0]Pass Through 2WIRE device addrress processing 0x0: Address rename (rule as R_2WIREPT1_PASS_ADRxy0/1. x is Lane0 or Lane1, y=<3:0>) 0x1: All Through (exception definition of address to ignore as R_2WIREPT2_NOPASS_ADRxz. x is Lane0 or Lane1, z=<7:0>)
0x0032	[7]	reserved	1	-	-	-
	[6:4]	R_2WIREPT_WA_BYTE	3	RW	3'h0	<this register is valid only when 0x0031[1]=0x1> Sub-Link 2WIRE Pass Through Divided Write/Read Sub Address (Word Address) Byte number setting Byte Number = R_2WIREPT_WA_BYTE + 1 0x0: 1Byte (= 8bit) sub address 0x1: 2Byte (=16bit) sub address Other: Reserved
	[3:0]	R_2WIREPT_DATA_BYTE	4	RW	4'h0	Sub-Link 2WIRE Pass Through Divided Write/Read data Byte number per a transaction setting, Byte Number = R_2WIREPT_DATA_BYTE + 1 (e.g. 0x2 for 3Byte per a transaction) *R_2WIREPT_WA_BYTE + R_2WIREPT_DATA_BYTE < d14 is required.

Table 36. 2-wire serial I/F Pass Through mode remote access common setting (Lane0)

Address	bit	Register Name	width	R/W	Init	Description
0x0040	[7:0]	R_2WIREPT1_PASS_ADR000	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane0 #0
0x0041	[7:0]	R_2WIREPT1_PASS_ADR001	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane0 #0
0x0042	[7:0]	R_2WIREPT1_PASS_ADR010	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane0 #1
0x0043	[7:0]	R_2WIREPT1_PASS_ADR011	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane0 #1
0x0044	[7:0]	R_2WIREPT1_PASS_ADR020	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane0 #2
0x0045	[7:0]	R_2WIREPT1_PASS_ADR021	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane0 #2
0x0046	[7:0]	R_2WIREPT1_PASS_ADR030	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane0 #3
0x0047	[7:0]	R_2WIREPT1_PASS_ADR031	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane0 #3
0x0048	[7:0]	R_2WIREPT2_NOPASS_ADR00	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #0
0x0049	[7:0]	R_2WIREPT2_NOPASS_ADR01	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #1
0x004A	[7:0]	R_2WIREPT2_NOPASS_ADR02	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #2
0x004B	[7:0]	R_2WIREPT2_NOPASS_ADR03	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #3
0x004C	[7:0]	R_2WIREPT2_NOPASS_ADR04	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #4
0x004D	[7:0]	R_2WIREPT2_NOPASS_ADR05	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #5
0x004E	[7:0]	R_2WIREPT2_NOPASS_ADR06	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #6
0x004F	[7:0]	R_2WIREPT2_NOPASS_ADR07	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #7
0x0050	[7:0]	R_2WIREPT1_PASS_ADRIN0	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through counterpart Sub-Link Slave internal register access dedicated address for Lane0

Table 37. 2-wire serial I/F Pass Through mode remote access common setting (Lane1)

Address	bit	Register Name	width	R/W	Init	Description
0x0060	[7:0]	R_2WIREPT1_PASS_ADR100	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane1 #0
0x0061	[7:0]	R_2WIREPT1_PASS_ADR101	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane1 #0
0x0062	[7:0]	R_2WIREPT1_PASS_ADR110	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane1 #1
0x0063	[7:0]	R_2WIREPT1_PASS_ADR111	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane1 #1
0x0064	[7:0]	R_2WIREPT1_PASS_ADR120	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane1 #2
0x0065	[7:0]	R_2WIREPT1_PASS_ADR121	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane1 #2
0x0066	[7:0]	R_2WIREPT1_PASS_ADR130	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane1 #3
0x0067	[7:0]	R_2WIREPT1_PASS_ADR131	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane1 #3
0x0068	[7:0]	R_2WIREPT2_NOPASS_ADR10	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #0
0x0069	[7:0]	R_2WIREPT2_NOPASS_ADR11	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #1
0x006A	[7:0]	R_2WIREPT2_NOPASS_ADR12	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #2
0x006B	[7:0]	R_2WIREPT2_NOPASS_ADR13	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #3
0x006C	[7:0]	R_2WIREPT2_NOPASS_ADR14	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #4
0x006D	[7:0]	R_2WIREPT2_NOPASS_ADR15	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #5
0x006E	[7:0]	R_2WIREPT2_NOPASS_ADR16	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #6
0x006F	[7:0]	R_2WIREPT2_NOPASS_ADR17	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #7
0x0070	[7:0]	R_2WIREPT1_PASS_ADRIN1	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through counterpart Sub-Link Slave internal register access dedicated address for Lane1

Table 38. 2-wire serial I/F Pass Through mode remote access common setting (Lane2)

Address	bit	Register Name	width	R/W	Init	Description
0x0080	[7:0]	R_2WIREPT1_PASS_ADR200	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane2 #0
0x0081	[7:0]	R_2WIREPT1_PASS_ADR201	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane2 #0
0x0082	[7:0]	R_2WIREPT1_PASS_ADR210	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane2 #1
0x0083	[7:0]	R_2WIREPT1_PASS_ADR211	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane2 #1
0x0084	[7:0]	R_2WIREPT1_PASS_ADR220	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane2 #2
0x0085	[7:0]	R_2WIREPT1_PASS_ADR221	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane2 #2
0x0086	[7:0]	R_2WIREPT1_PASS_ADR230	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane2 #3
0x0087	[7:0]	R_2WIREPT1_PASS_ADR231	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane2 #3
0x0088	[7:0]	R_2WIREPT2_NOPASS_ADR20	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane2 #0
0x0089	[7:0]	R_2WIREPT2_NOPASS_ADR21	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane2 #1
0x008A	[7:0]	R_2WIREPT2_NOPASS_ADR22	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane2 #2
0x008B	[7:0]	R_2WIREPT2_NOPASS_ADR23	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane2 #3
0x008C	[7:0]	R_2WIREPT2_NOPASS_ADR24	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane2 #4
0x008D	[7:0]	R_2WIREPT2_NOPASS_ADR25	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane2 #5
0x008E	[7:0]	R_2WIREPT2_NOPASS_ADR26	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane2 #6
0x008F	[7:0]	R_2WIREPT2_NOPASS_ADR27	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane2 #7
0x0090	[7:0]	R_2WIREPT1_PASS_ADRIN2	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through counterpart Sub-Link Slave internal register access dedicated address for Lane2

Table 39. 2-wire serial I/F Pass Through mode remote access common setting (Lane3)

Address	bit	Register Name	width	R/W	Init	Description
0x00A0	[7:0]	R_2WIREPT1_PASS_ADR300	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane3 #0
0x00A1	[7:0]	R_2WIREPT1_PASS_ADR301	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane3 #0
0x00A2	[7:0]	R_2WIREPT1_PASS_ADR310	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane3 #1
0x00A3	[7:0]	R_2WIREPT1_PASS_ADR311	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane3 #1
0x00A4	[7:0]	R_2WIREPT1_PASS_ADR320	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane3 #2
0x00A5	[7:0]	R_2WIREPT1_PASS_ADR321	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane3 #2
0x00A6	[7:0]	R_2WIREPT1_PASS_ADR330	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane3 #3
0x00A7	[7:0]	R_2WIREPT1_PASS_ADR331	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane3 #3
0x00A8	[7:0]	R_2WIREPT2_NOPASS_ADR30	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane3 #0
0x00A9	[7:0]	R_2WIREPT2_NOPASS_ADR31	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane3 #1
0x00AA	[7:0]	R_2WIREPT2_NOPASS_ADR32	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane3 #2
0x00AB	[7:0]	R_2WIREPT2_NOPASS_ADR33	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane3 #3
0x00AC	[7:0]	R_2WIREPT2_NOPASS_ADR34	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane3 #4
0x00AD	[7:0]	R_2WIREPT2_NOPASS_ADR35	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane3 #5
0x00AE	[7:0]	R_2WIREPT2_NOPASS_ADR36	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane3 #6
0x00AF	[7:0]	R_2WIREPT2_NOPASS_ADR37	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane3 #7
0x00B0	[7:0]	R_2WIREPT1_PASS_ADRIN3	8	RW	8'h00	<this regiseters is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through counterpart Sub-Link Slave internal register access dedicated address for Lane3

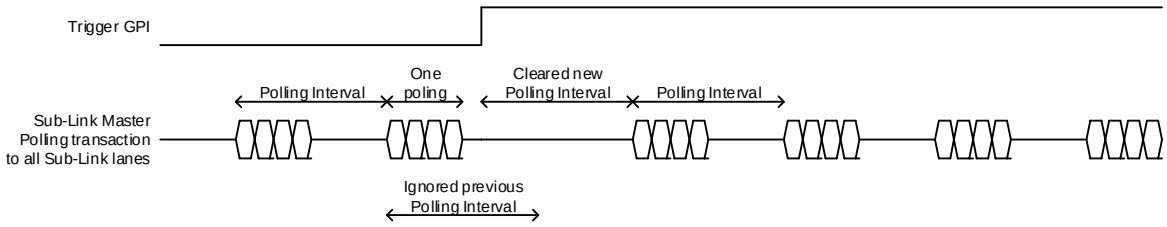
6.13.3. Sub-Link transaction time accuracy Improvement

Sub-Link Polling timing can be controllable by GPI input. All Sub-Link lane transaction timing can be arranged.

Table 40. Sub-Link transaction time accuracy control

Address	bit	Register Name	width	R/W	Init	Description
0x0016	[7:6]	reserved	2	-	-	-
	[5:4]	R_POL_TIM_CLR_EN	2	RW	2'h0	<this regiseter is valid when 0x0010[*n*]=0x1, *n*=0,1,2,3> Polling Timer Clear/Mask setting 0x1: The polling timer is cleared when the inputted GPIO changes 0x2: The polling timer masked when inputted GPIO signal is high, and the polling transmission is outputted after inputted GPIO signal is falling.
	[3]	reserved	1	-	-	-
	[2:0]	R_GPI_TRG_SEL	3	RW	3'h0	<this regiseter is valid when 0x0010[*n*]=0x1, *n*=0,1,2,3> Polling Timer Clear/Mask GPIO signal select 0x0: GPIO0 (this setting is valid only when 0x1004[3:0]=0x3) 0x1: GPIO1 (this setting is valid only when 0x1004[7:4]=0x3) Other: Reserved

Polling Timer Clear



Polling Timer Mask

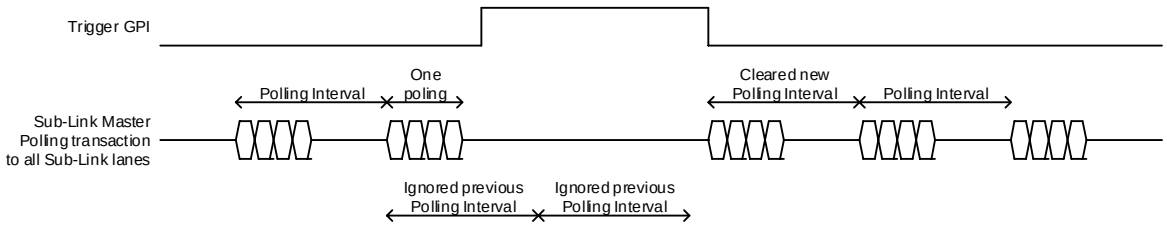


Figure 13. Sub-Link transaction time accuracy control

6.14. GPIO setting

Setting of GPIO can be configurable by 2-wire access to internal register.

Table 41. GPIO setting (1/2)

Address	bit	Register Name	width	R/W	init	Description
0x1001	[7:4]	R_GPIO7_MODE	4	R/W	4'h0	GPIO7 I/O Mode 0x0: Disable 0x1: Programable GPO (Output Low) 0x2: Programable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
	[3:0]	R_GPIO6_MODE	4	R/W	4'h0	GPIO6 I/O Mode 0x0: Disable 0x1: Programable GPO (Output Low) 0x2: Programable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
0x1002	[7:4]	R_GPIO5_MODE	4	R/W	4'h0	GPIO5 I/O Mode 0x0: Disable 0x1: Programable GPO (Output Low) 0x2: Programable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
	[3:0]	R_GPIO4_MODE	4	R/W	4'h0	GPIO4 I/O Mode 0x0: Disable 0x1: Programable GPO (Output Low) 0x2: Programable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved

Table 42. GPIO setting (2/2)

Address	bit	Register Name	width	R/W	init	Description
0x1003	[7:4]	R_GPIO3_MODE	4	R/W	4'h0	GPIO3 I/O Mode 0x0: Disable 0x1: Programable GPO (Output Low) 0x2: Programable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
	[3:0]	R_GPIO2_MODE	4	R/W	4'h0	GPIO2 I/O Mode 0x0: Disable 0x1: Programable GPO (Output Low) 0x2: Programable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
0x1004	[7:4]	R_GPIO1_MODE	4	R/W	4'h0	GPIO1 I/O Mode 0x0: Disable 0x1: Programable GPO (Output Low) 0x2: Programable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
	[3:0]	R_GPIO0_MODE	4	R/W	4'h0	GPIO0 I/O Mode 0x0: Disable 0x1: Programable GPO (Output Low) 0x2: Programable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved

6.14.1. Register GPIO

GPIO output control are available with register.

6.14.2. GPIO as secondary 2-wire port

GPIO port can be secondary 2-wire port, which can accommodate dual 2-wire access from two processors.

If two 2-wire commands are inputted at the same time, the earlier command can be communicated and the later command are kept wait by clock stretching scheme.

6.14.3. Through GPIO Sub-Link Polling input/output

Local GPIO input is continuously reflected to remote GPIO output via Sub-Link polling. Bridging data are sampled every Sub-Link polling, whose basic interval is controlled by register R_SLINK_POL_TIM_UP/_DN. Remote 2-wire access may become long transaction and could lengthen Through GPIO polling reflection interval.

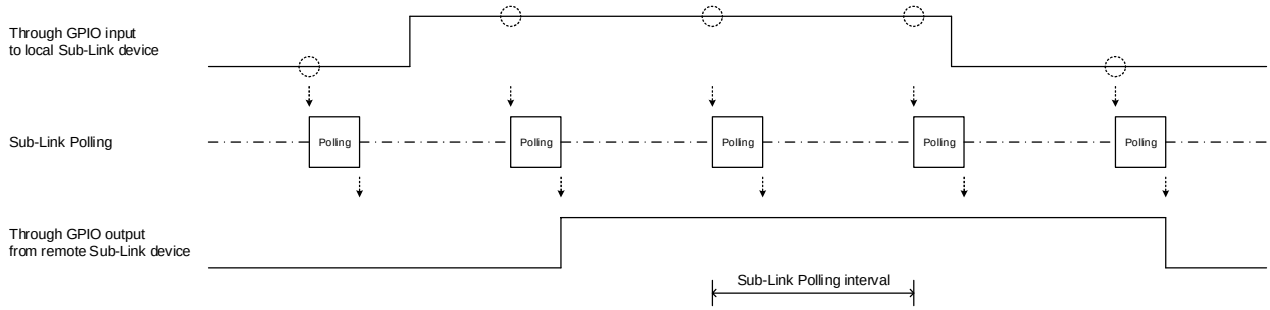


Figure 14. Through GPIO bridge sampling

As default setting with THCV231 as Sub-Link Slave communication (THCV244A as Sub-Link Master), GPIO1 Sub-Link Polling bridges input to THCV231's GPIO4 through mode and GPIO0 Sub-Link Polling bridges input to THCV231's GPIO3 through mode respectively.

As default setting with THCV241A as Sub-Link Slave communication (THCV244A as Sub-Link Master), GPIO0/1 are dedicated to GPI to Sub-Link Lane0. GPIO2/3 are dedicated to GPI to Sub-Link Lane1. GPIO2/3 are also dedicated to GPO from selected Sub-Link Lane.

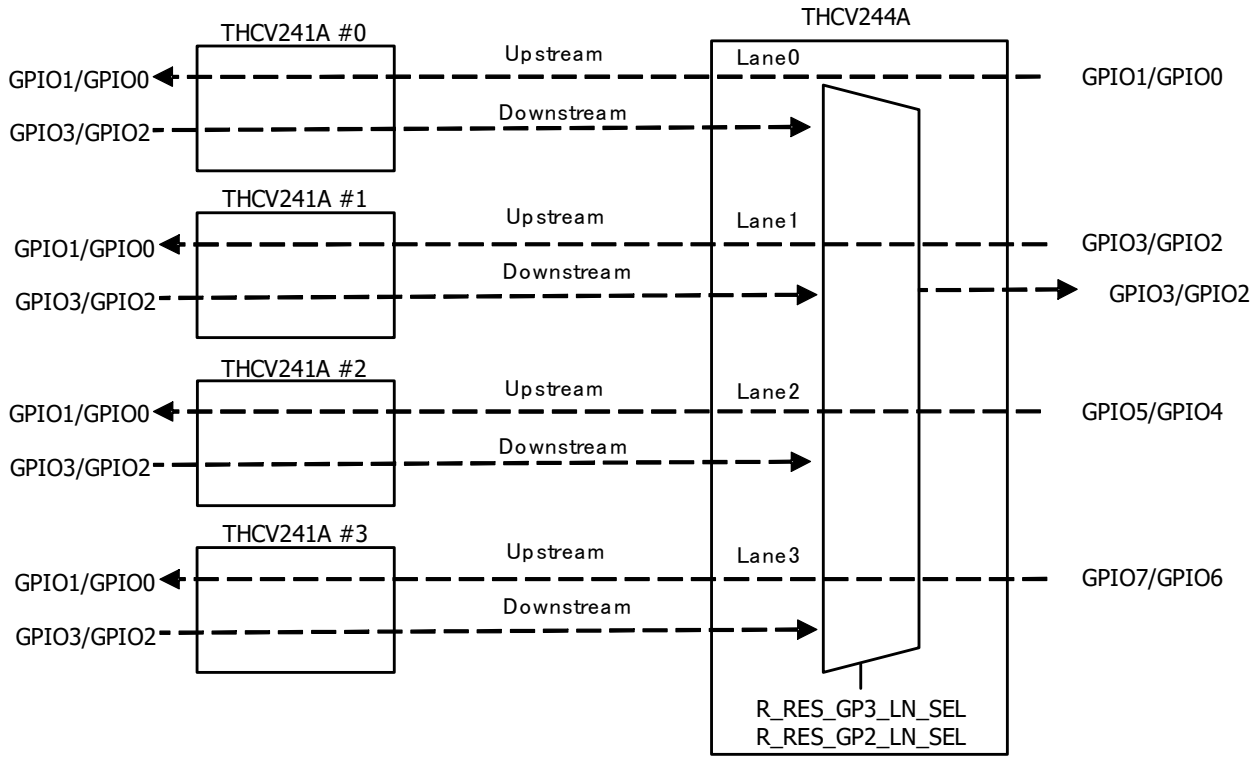


Figure 15. Through GPIO via Sub-Link transaction assignment with THCV241A

Remote UART bridge is supported with Sub-Link Polling GPIO input/output. Remote UART Tx and Rx bridge baud rate is supposed to be designed against Sub-Link Polling interval to accommodate deterministic jitter caused by intermittent Sub-Link communication timing.

6.15. Internal Error / status signal monitoring ERR0/ERR1 pin output

Internal error or status signal can be monitored as external ERR0/ERR1 pin output by register setting.

Table 43. Internal Error / status signal monitoring ERR0/ERR1 pin output setting

Address	bit	Register Name	width	R/W	init	Description
0x1005	[7:4]	R_ERR1_MODE	4	R/W	4'h0	ERR1 I/O Mode 0x0: Disable 0x1: OpenDrain Output Mode 0x2: Push/Pull Output Mode Other: Reserved
	[3:0]	R_ERR0_MODE	4	R/W	4'h0	ERR0 I/O Mode 0x0: Disable 0x1: OpenDrain Output Mode 0x2: Push/Pull Output Mode Other: Reserved
0x100C	[7:0]	R_ERR1_SEL	8	R/W	8'h00	ERR1 Pin Output Signal Select
0x100D	[7:0]	R_ERR0_SEL	8	R/W	8'h00	ERR0 Pin Output Signal Select

Table 44. IC Internal selectable Error / status signal (1/3)

R_ERR1/0_SEL[7:0]	Error signal	Description
0x00	0 Fixed	
0x01	1 Fixed	
0x02	Vx1_LOCKN_ALL	OR operated of all operating lanes, LOCKN signal
0x03	Vx1_HTPDN_ALL	OR operated of all operating lanes, HTPDN signal
0x04	Vx1_FBETOUT_LATCH_ALL	OR operated of all operating lanes, field-bet latched result
0x05	Vx1_FBETOUT_REAL_ALL	OR operated of all operating lanes, field-bet real result
0x06	Vx1_PERR_ALL	OR operated of all operating lanes, protocol error
0x07	MLINK_CRCERR_ALL	OR operated of all operating lanes, crc error
0x08	Vx1_CLOCKSTP_ALL	clock stop detector of all lanes
0x09	MLINK_VDSK_OK_ALL	Vsync synchronization OK flag of all lanes
0x0A	MLINK_VDSK_NG_ALL	Vsync synchronization NG flag of all lanes
0x0B	Reserved	
0x0C	Reserved	
0x0D	SLINK_PERR_ALL	OR operated of all operating lanes, protocol error
0x0E	SLINK_TMOUT_ALL	OR operated of all operating lanes, time out error
0x0F	SLINK_FBETOUT	OR operated of all operating lanes, sub-link field-bet result
0x10	Vx1_LOCKN0	lane0 LOCKN signal
0x11	Vx1_LOCKN1	lane1 LOCKN signal
0x12	Vx1_LOCKN2	lane2 LOCKN signal
0x13	Vx1_LOCKN3	lane3 LOCKN signal
0x14	Vx1_HTPDN0	lane0 HTPDN signal
0x15	Vx1_HTPDN1	lane1 HTPDN signal
0x16	Vx1_HTPDN2	lane2 HTPDN signal
0x17	Vx1_HTPDN3	lane3 HTPDN signal
0x18	Vx1_BETOUT_LATCH0	lane0 field-bet latched result
0x19	Vx1_BETOUT_LATCH1	lane1 field-bet latched result
0x1A	Vx1_BETOUT_LATCH2	lane2 field-bet latched result
0x1B	Vx1_BETOUT_LATCH3	lane3 field-bet latched result
0x1C	Vx1_BETOUT_REAL0	lane0 field-bet real result
0x1D	Vx1_BETOUT_REAL1	lane1 field-bet real result
0x1E	Vx1_BETOUT_REAL2	lane2 field-bet real result
0x1F	Vx1_BETOUT_REAL3	lane3 field-bet real result

Table 45. IC Internal selectable Error / status signal (2/3)

R_ERR1/0_SEL[7:0]	Error signal	Description
0x20	Vx1_PERR0	lane0, protocol error
0x21	Vx1_PERR1	lane1, protocol error
0x22	Vx1_PERR2	lane2, protocol error
0x23	Vx1_PERR3	lane3, protocol error
0x24	MLINK_CRCERR0	lane0, crc error
0x25	MLINK_CRCERR1	lane1, crc error
0x26	MLINK_CRCERR2	lane2, crc error
0x27	MLINK_CRCERR3	lane3, crc error
0x28	MLINK_VSYNC0	lane0, Vsync signal
0x29	MLINK_VSYNC1	lane1, Vsync signal
0x2A	MLINK_VSYNC2	lane2, Vsync signal
0x2B	MLINK_VSYNC3	lane3, Vsync signal
0x2C	MLINK_HSYNC0	lane0, Hsync signal
0x2D	MLINK_HSYNC1	lane1, Hsync signal
0x2E	MLINK_HSYNC2	lane2, Hsync signal
0x2F	MLINK_HSYNC3	lane3, Hsync signal
0x30	MLINK_DE0	lane0, DE signal
0x31	MLINK_DE1	lane1, DE signal
0x32	MLINK_DE2	lane2, DE signal
0x33	MLINK_DE3	lane3, DE signal
0x34	MLINK_CLK0	lane0, clock signal
0x35	MLINK_CLK1	lane1, clock signal
0x36	MLINK_CLK2	lane2, clock signal
0x37	MLINK_CLK3	lane3, clock signal
0x38	MIPI_BYTECLK	CSI byte clock signal
0x39	OSCCLK	internal oscilltor clock signal
0x3A	Reserved	
0x3B	Reserved	
0x3C	Reserved	
0x3D	Reserved	
0x3E	Reserved	
0x3F	Reserved	

Table 46. IC Internal selectable Error / status signal (3/3)

R_ERR1/0_SEL[7:0]	Error signal	Description
0x40	MLINK_FS0	lane0, Frame Start
0x41	MLINK_FS1	lane1, Frame Start
0x42	MLINK_FS2	lane2, Frame Start
0x43	MLINK_FS3	lane3, Frame Start
0x44	MLINK_FE0	lane0, Frame End
0x45	MLINK_FE1	lane1, Frame End
0x46	MLINK_FE2	lane2, Frame End
0x47	MLINK_FE3	lane3, Frame End
0x48	MLINK_VDSK_NG0	lane0, Vsync synchronization NG flag
0x49	MLINK_VDSK_NG1	lane1, Vsync synchronization NG flag
0x4A	MLINK_VDSK_NG2	lane2, Vsync synchronization NG flag
0x4B	MLINK_VDSK_NG3	lane3, Vsync synchronization NG flag
0x4C	TOP_CKSUM_ERR	register checksum error
0x4D	Reserved	
0x4E	Reserved	
0x4F	Reserved	
0x50	Reserved	
0x51	Reserved	
0x52	Reserved	
0x53	Reserved	
0x54	SLINK_PERR0	lane0, protocol error
0x55	SLINK_PERR1	lane1, protocol error
0x56	SLINK_PERR2	lane2, protocol error
0x57	SLINK_PERR3	lane3, protocol error
0x58	SLINK_TMOUT0	lane0, time out error
0x59	SLINK_TMOUT1	lane1, time out error
0x5A	SLINK_TMOUT2	lane2, time out error
0x5B	SLINK_TMOUT3	lane3, time out error

6.16. Internal Error / status signal monitoring register

Internal error or status signal can be monitored as register read value.

Error count register can be cleared by particular register write “1” access.

Table 47. Internal Error / status signal monitoring register (1/2)

Address	bit	Register Name	width	R/W	Init	Description
0x00F1	[7:1]	reserved	7	-	-	-
	[0]	R_SLINK_FBETERR_CLR	1	W	-	<this register is valid only when 0x1035[4]=0x1> Sub-Link FieldBET error count clear 0x1: Clear
0x00F2	[7:0]	R_SLINK_FBETERR_NUM_UP	8	R	-	<this register is valid only when 0x1035[4]=0x1> Sub-Link FieldBET error count parameter
0x00F3	[7:0]	R_SLINK_FBETERR_NUM_DN	8	R	-	<this register is valid only when 0x1035[4]=0x1> Sub-Link FieldBET error count =256×R_SLINK_FBETERR_NUM_UP<7:0> ＋R_SLINK_FBETERR_NUM_DN<7:0>

Table 48. Internal Error / status signal monitoring register (2/2)

Address	bit	Register Name	width	R/W	init	Description
0x174F	[7:4]	R_MLINK_CRC_ERRCLR	4	W	-	Main-Link CRC Error Counter Clear <0x174F[7] register is valid only when 0x1401[0]=0x1> [7] Main-Link CRC Error Counter Clear for Lane3 0x1: Clear <0x174F[6] register is valid only when 0x1301[0]=0x1> [6] Main-Link CRC Error Counter Clear for Lane2 0x1: Clear <0x174F[5] register is valid only when 0x1201[0]=0x1> [5] Main-Link CRC Error Counter Clear for Lane1 0x1: Clear <0x174F[4] register is valid only when 0x1101[0]=0x1> [4] Main-Link CRC Error Counter Clear for Lane0 0x1: Clear
	[3:0]	R_MLINK_BET_ERRCLR	4	W	-	Main-Link BET Error Counter Clear <0x174F[3] register is valid only when 0x1035[3]=0x1> [3] Main-Link BET Error Counter Clear for Lane3 0x1: Clear <0x174F[2] register is valid only when 0x1035[2]=0x1> [2] Main-Link BET Error Counter Clear for Lane2 0x1: Clear <0x174F[1] register is valid only when 0x1035[1]=0x1> [1] Main-Link BET Error Counter Clear for Lane1 0x1: Clear <0x174F[0] register is valid only when 0x1035[0]=0x1> [0] Main-Link BET Error Counter Clear for Lane0 0x1: Clear
0x1750	[7:0]	MLINK0_CRC_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1101[0]=0x1> Main-Link(Lane0) CRC Error Number (Upper Byte)
0x1751	[7:0]	MLINK0_CRC_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1101[0]=0x1> Main-Link(Lane0) CRC Error Number (Lower Byte)
0x1752	[7:0]	MLINK1_CRC_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1201[0]=0x1> Main-Link(Lane1) CRC Error Number (Upper Byte)
0x1753	[7:0]	MLINK1_CRC_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1201[0]=0x1> Main-Link(Lane1) CRC Error Number (Lower Byte)
0x1754	[7:0]	MLINK2_CRC_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1301[0]=0x1> Main-Link(Lane2) CRC Error Number (Upper Byte)
0x1755	[7:0]	MLINK2_CRC_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1301[0]=0x1> Main-Link(Lane2) CRC Error Number (Lower Byte)
0x1756	[7:0]	MLINK3_CRC_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1401[0]=0x1> Main-Link(Lane3) CRC Error Number (Upper Byte)
0x1757	[7:0]	MLINK3_CRC_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1401[0]=0x1> Main-Link(Lane3) CRC Error Number (Lower Byte)
0x1758	[7:0]	MLINK0_BET_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1035[0]=0x1> Main-Link(Lane0) BET Error Number (Upper Byte)
0x1759	[7:0]	MLINK0_BET_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1035[0]=0x1> Main-Link(Lane0) BET Error Number (Lower Byte)
0x175A	[7:0]	MLINK1_BET_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1035[1]=0x1> Main-Link(Lane1) BET Error Number (Upper Byte)
0x175B	[7:0]	MLINK1_BET_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1035[1]=0x1> Main-Link(Lane1) BET Error Number (Lower Byte)
0x175C	[7:0]	MLINK2_BET_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1035[2]=0x1> Main-Link(Lane2) BET Error Number (Upper Byte)
0x175D	[7:0]	MLINK2_BET_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1035[2]=0x1> Main-Link(Lane2) BET Error Number (Lower Byte)
0x175E	[7:0]	MLINK3_BET_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1035[3]=0x1> Main-Link(Lane3) BET Error Number (Upper Byte)
0x175F	[7:0]	MLINK3_BET_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1035[3]=0x1> Main-Link(Lane3) BET Error Number (Lower Byte)

6.17. Interrupt monitoring

Interrupt (INT1/0) detects occurrence of internal error or status signal and then, latch the detected state.

Interrupt factor can be cleared by particular register write “1” access. (*They are indicated as “R_INTC_*”)

Interrupt factor can be masked to “0” fixed by particular register appropriate write access.

INT interrupt function is supposed to be cleared before start monitoring any desired status because INT status may change at power on condition and THCV244A internal boot up procedure.

Table 49. Interrupt monitoring

Register	Address	bit	Description
R_INTR_MLRX	0x1710/ 0x1718	7	Main-Link protocol error for Lane3
		6	Main-Link protocol error for Lane2
		5	Main-Link protocol error for Lane1
		4	Main-Link protocol error for Lane0
		3	Main-Link RX LOCKN=L to H detection flag for Lane3
		2	Main-Link RX LOCKN=L to H detection flag for Lane2
		1	Main-Link RX LOCKN=L to H detection flag for Lane1
		0	Main-Link RX LOCKN=L to H detection flag for Lane0
R_INTR_MODE	0x1711/ 0x1719	7	Vsync synchronization OK flag of all lanes
		6	All Main-Link RX LOCKN=H detection flag
R_INTR_DSHNDLR		5	Data Stream Handler Distribution error
		4	Reserved
R_INTR_FMT		3	Main-Link RX CRC error1 for Lane3
		2	Main-Link RX CRC error1 for Lane2
		1	Main-Link RX CRC error1 for Lane1
		0	Main-Link RX CRC error1 for Lane0
R_INTR_CSI	0x1712/ 0x171A	1	MIPI CSI-2 status error for port1
		0	MIPI CSI-2 status error for port0
	0x1713/ 0x171B	6	MIPI CSI-2 general error
		5	Reserved
		4	Reserved
		3	Reserved
		2	Reserved
		1	Reserved
		0	Reserved
R_INTR_BDC2Q	0x1714/ 0x171C	1	Internal Register AutoCheckSum error flag
		0	Reserved
	0x1715/ 0x171D	7	Sub-Link Slave side 2-wire access complete flag for Lane3
		6	Sub-Link Slave side 2-wire access complete flag for Lane2
		5	Sub-Link Slave side 2-wire access complete flag for Lane1
		4	Sub-Link Slave side 2-wire access complete flag for Lane0
		3	Sub-Link Slave side interrupt detection flag for Lane3
		2	Sub-Link Slave side interrupt detection flag for Lane2
		1	Sub-Link Slave side interrupt detection flag for Lane1
		0	Sub-Link Slave side interrupt detection flag for Lane0
	0x1716/ 0x171E	7	Sub-Link protocol error for Lane3
		6	Sub-Link protocol error for Lane2
		5	Sub-Link protocol error for Lane1
		4	Sub-Link protocol error for Lane0
R_INTR_DSHNDLR		3	Data Stream Hander error2 for Lane3
		2	Data Stream Hander error2 for Lane2
		1	Data Stream Hander error2 for Lane1
		0	Data Stream Hander error2 for Lane0

As a register, interrupt detected state is “1” and cleared state is “0”. When multiple interrupt sources are activated, the OR operated result is indicated as IC external INT1/0 pin output.

As an external INT1/0 pin output, open drain output interrupt detected state is “Low” and cleared state is “Hi-Z”, while INT1/0 pin CMOS push-pull output interrupt detected state is “Low” and cleared state is “High”.

Table 50. INT1/0 pin output control

Address	bit	Register Name	width	R/W	init	Description
0x1006	[7:4]	R_INT1_MODE	4	R/W	4'h0	INT1 I/O Mode 0x0: Disable 0x1: OpenDrain Output Mode 0x2: Push/Pull Output Mode Other: Reserved
	[3:0]	R_INT0_MODE	4	R/W	4'h0	INT0 I/O Mode 0x0: Disable 0x1: OpenDrain Output Mode 0x2: Push/Pull Output Mode Other: Reserved

INT1/0 interrupt function is supposed to be cleared before start monitoring any desired status because INT1/0 status may have been changed before monitoring activation.

6.18. Multiple camera synchronization Frame Vsync supply

Frame VSYNC can be supplied from THCV244A to Sub-Link Slave GPO.

EXTSYNC input or internally generated VSYNC become supply source. Settings are configurable by 2-wire access to internal register. When internal VSYNC is selected, generated VSYNC is not only sent to remote Sub-Link Slave but also output from EXTSYNC pin.

Internal VSYNC uses two clock source, internal oscillator clock and video pixel clock from Main-Link input. At the beginning of internal VSYNC generation operation, oscillator clock is used to supply VSYNC. After Main-Link video source is received stable, internal VSYNC generation source is switched to video pixel clock from selected Main-Link input. When Main-Link video pixel clock input is lost, internal VSYNC generator again uses internal oscillator clock until Main-Link video pixel clock input is regained.

Table 51. Multiple camera synchronization Frame Vsync supply setting (1/3)

Address	bit	Register Name	width	R/W	init	Description
0x1007	[7:4]	reserved	4	-	-	-
	[3:0]	R_EXTSYNC_MODE	4	R/W	4'h0	EXTSYNC I/O Mode 0x0: Disable 0x1: Normal Mode (Controlled by Sub-Link Register) Other: Reserved

Table 52. Multiple camera synchronization Frame Vsync supply setting (2/3)

Address	bit	Register Name	width	R/W	Init	Description
0x0020	[7:5]	reserved	3	-	-	-
	[4]	R_VS_PHASE_EN	1	RW	1'h0	<this regiseter is valid only when 0x0020[1:0]=0x2> Enable of shifting the Internal VSYNC output timing 0x0: Disable 0x1: Enable (*) (*) 0x002E register is related for output timing
	[3:2]	reserved	2	-	-	-
	[1:0]	R_VS_MODE	2	RW	2'h0	<this regiseter is valid when 0x0010[*n*]=0x1, *n*=0,1,2,3> multiple camera synchronization Frame VSYNC supply mode setting 0x1: Select external VSYNC signal from EXTSYNC pin (*) 0x2: Select internal VSYNC signal and output for EXTSYNC pin (**) Other: Disable (*) 0x1007 register is related to this mode (**) set this mode after setting both 0x0021 and 0x0023 - 0x002E registers
0x0021	[7:5]	reserved	3	-	-	-
	[4]	ReservedL	1	RW	1'h0	must be left 0x0 (default setting)
	[3:1]	reserved	3	-	-	-
	[0]	R_VS_POL	1	RW	1'h0	<this regiseter is valid only when 0x0020[1:0]=0x2> Internal VSYNC Pulse Polarity 0x0: Low Pulse 0x1: High Pulse
0x0022	[7]	reserved	1	-	-	-
	[6:4]	R_VS_GPI_SEL	3	RW	3'h0	<this regiseter is valid when 0x0020[1:0]=0x1 or 0x2> Select a assignment bit for Frame VSYNC signal to send 0x0: a bit of Sub-Link for GPIO0 0x1: a bit of Sub-Link for GPIO1 Other: Reserved
	[3:2]	ReservedL	2	RW	2'h0	Must be set 0x0
	[1:0]	R_VS_LANE_SEL	2	RW	2'h0	<this regiseter is valid when 0x0020[1:0]=0x1 or 0x2> Select Sub-Link Lane for Frame VSYNC signal to send (*each bit setting) [3]:Sub-Link Lane3 (*) [2]:Sub-Link Lane2 (*) [1]:Sub-Link Lane1 (*) [0]:Sub-Link Lane0 (*) 0x0: no send 0x1: send Frame VSYNC signal
0x0023	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSOSC_LINE_UP	4	RW	4'h0	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC clock number / line by oscillator setting
0x0024	[7:0]	R_VSOSC_LINE_DN	8	RW	8'h0F	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC clock number / line by oscillator = (256×R_VSOSC_LINE_UP<3:0> +R_VSOSC_LINE_DN<7:0>+1)×tOSC *Clock / line is 1 when R_VSOSC_LINE_UP=0x0 and R_VSOSC_LINE_DN=0x0
0x0025	[7:0]	R_VSOSC_WIDTH	8	RW	8'h00	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse width line number by oscillator setting Line Number = R_VSOSC_WIDTH + 1 (e.g. 0x00 for 1line)
0x0026	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSOSC_TIM_UP	4	RW	4'h0	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse interval line number by oscillator setting
0x0027	[7:0]	R_VSOSC_TIM_DN	8	RW	8'h0F	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse interval line number by oscillator = (256×R_VSOSC_TIM_UP<3:0> +R_VSOSC_TIM_DN<7:0>+1)×tOSC *Interval line is 2 when R_VSOSC_TIM_UP=0x0 and R_VSOSC_TIM_DN=0x0

Table 53. Multiple camera synchronization Frame Vsync supply setting (3/3)

Address	bit	Register Name	width	R/W	Init	Description
0x0028	[7:2]	reserved	6	-	-	-
	[1:0]	R_VS_PCLK_SEL	2	RW	2'h0	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC generation base pixel clock domain select 0x0: select source clock (CLK_I) from Main-Link Lane0 0x1: select source clock (CLK_I) from Main-Link Lane1 0x2: select source clock (CLK_I) from Main-Link Lane2 0x3: select source clock (CLK_I) from Main-Link Lane3 Other: Reserved
0x0029	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSP_LINE_UP	4	RW	4'h0	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC clock number / line by base pixel clock setting
0x002A	[7:0]	R_VSP_LINE_DN	8	RW	8'h0F	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC clock number / line by base pixel clock = (256× R_VSP_LINE_UP<3:0> +R_VSP_LINE_DN<7:0>+1)×CLK_I *Clock / line is 1 when R_VSP_LINE_UP=0x0 and R_VSP_LINE_DN=0x0
0x002B	[7:0]	R_VSP_WIDTH	8	RW	8'h04	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse width line number by base pixel clock setting Line Number = R_VSP_WIDTH + 1 (e.g. 0x00 for 1line)
0x002C	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSP_TIM_UP	4	RW	4'h0	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse interval line number setting
0x002D	[7:0]	R_VSP_TIM_DN	8	RW	8'h0F	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse interval line number = (256×R_VSP_TIM_UP<3:0> +R_VSP_TIM_DN<7:0>+1) Internal VSYNC pulse interval frame period by base pixel clock = (256×R_VSP_TIM_UP<3:0> +R_VSP_TIM_DN<7:0>+0x1)× (256×R_VSP_LINE_UP<3:0> +R_VSP_LINE_DN<7:0>+0x1)×CLK_I *Interval line is 2 when R_VSP_TIM_UP=0x0 and R_VSP_TIM_DN=0x0 *For setting or reset of this register, R_VS_MODE is supposed to be disable
0x002E	[7:0]	R_VS_PHASE_WIDTH	8	RW	8'h01	<this register is valid only when 0x0020[1:0]=0x2> The internal VSYNC output timing of Sub-Link Lane1 is delayed by "16 × R_VS_PHASE_WIDTH × CLK_I" from Sub-Link Lane0. (e.g. 0x00 is 16×CLK_I)

6.19. Power On Sequence

Power On Sequence must be controlled appropriate.

For Power On Reset, PDN input must be low at the moment when VDDCORE (VDD12) reach operating condition voltage. As a note, PDN pin itself does not belongs to VDDCORE (VDD12) but to VDDIO1 (VDDH). PDN Power On Reset control is mandatory.

MIPI, PLL and V-by-One® HS block are reset state at power on default and require Reset Release.

V-by-One® HS Soft Reset / PLL Soft Reset => MIPI Soft Reset is proper. See below detail.

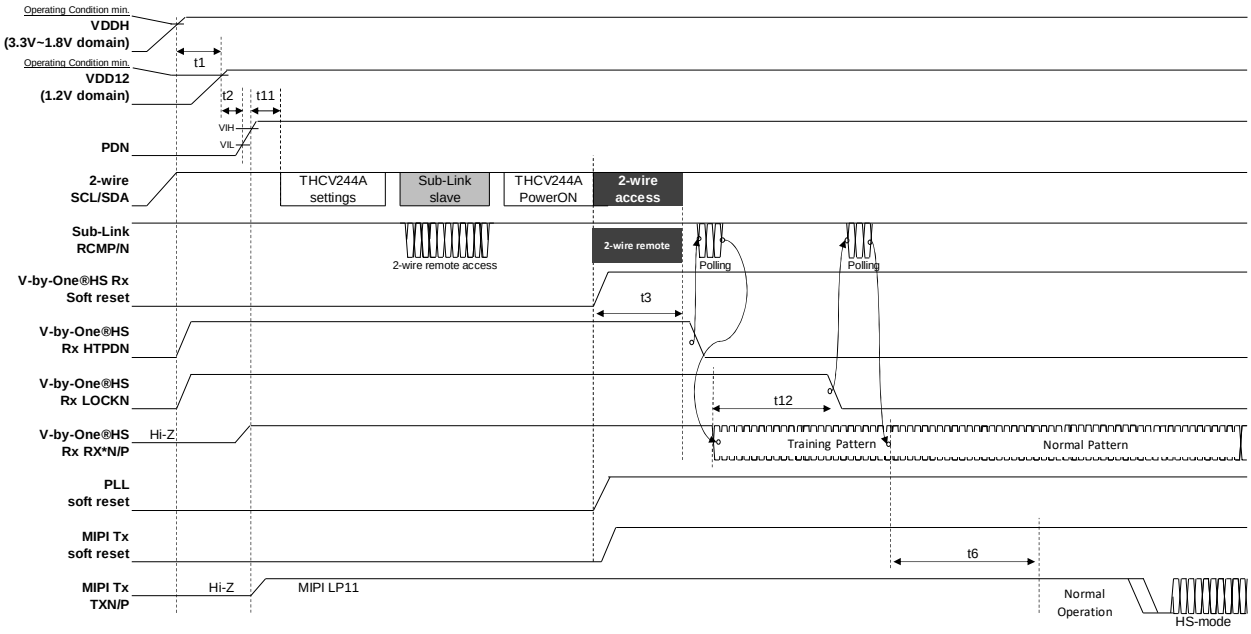


Figure 16. Power On Sequence procedure

Table 54. Power On Sequence specification

symbol	description	min.	typ.	max.	unit
t1	Required wait from VDDH assert to VDD12 assert	0	-	-	us
t2	Required wait from Power On to PDN High control	1000	-	-	us
t11	Required wait from PDN High to Register Access	300	-	-	us
t3	Time of V-by-One®HS Rx soft reset High to HTPDN Low	-	-	10	us
t12	Time of Training Pattern Input to LOCKN Low	-	-	980	us
t6	Time of V-by-One®HS Normal operation input to MIPI normal operation output	-	-	50+ 1frame	us

The first MIPI output from Power On waits vertical blanking period and starts output; therefore, MIPI normal operation may be hold for maximum 1frame, which depends on used video format.

6.20. Lock / Re-Lock Sequence

Lock and re-lock sequence are as follows. V-by-One® HS automatically shifts into lock status from initial status or unlock status caused by external noise under appropriate parameter set condition.

THCV244A LOCK Sequence

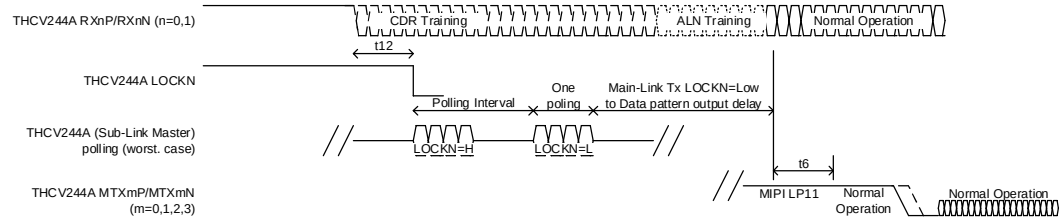


Figure 17. Lock Sequence

THCV244A Re-LOCK Sequence

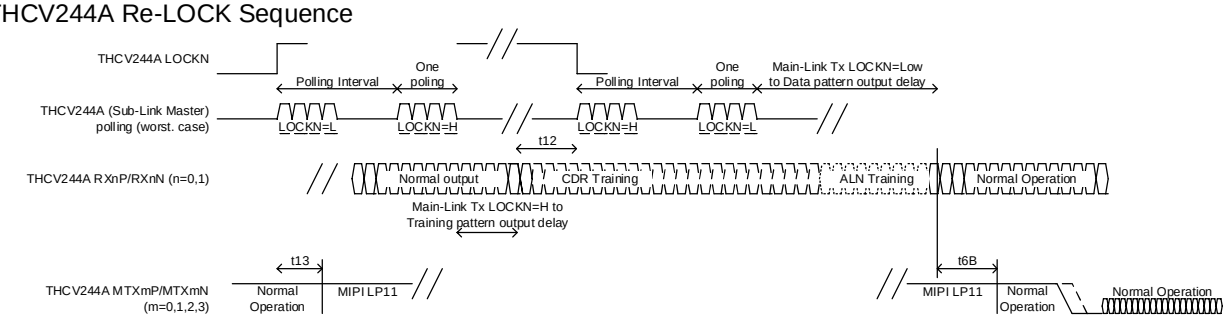


Figure 18. Re-Lock Sequence

Table 55. Lock / Re-Lock Sequence specification

symbol	description	min.	typ.	max.	unit
t13	Time of LOCKN=H to MIPI Stand-by LP11 output	-	-	98	us
t6B	Time of V-by-One®HS Normal operation re-input to MIPI normal operation re-output	-	-	50	us

7. Absolute Maximum Ratings

Table 56. Absolute Maximum Ratings*

Parameter	min.	typ.	max.	Unit
Supply Voltage (VDDIO1,VDDIO2)	-0.3	-	4	V
Supply Voltage (VDDCORE,VDDRX,VDDTX,VDDPLL)	-	-	1.6	V
LVCMOS Input Voltage (1.2V domain)	-0.3	-	VDDRX+0.3 *2	V
LVCMOS Input Voltage (VDDIO1 domain)	-0.3	-	VDDIO1+0.3 *1	V
LVCMOS Output Voltage	-0.3	-	VDDIO1+0.3 *1	V
LVCMOS Bi-directional buffer Input Voltage	-0.3	-	VDDIO1+0.3 *1	V
LVCMOS Bi-directional buffer Output Voltage	-0.3	-	VDDIO1+0.3 *1	V
LVCMOS Input Voltage (VDDIO2 domain)	-0.3	-	VDDIO2+0.3 *1	V
CML Receiver Voltage	-0.3	-	VDDRX+0.3 *2	V
MIPI Transmitter Voltage	-0.3	-	VDDTX+0.3 *2	V
CML Bi-directional buffer Input Voltage	-0.3	-	VDDIO2+0.3 *1	V
CML Bi-directional buffer Output Voltage	-0.3	-	VDDIO2+0.3 *1	V
Output Current	-30	-	30	mA
Storage Temperature	-55	-	125	°C
Junction Temperature	-	-	125	°C
Reflow Peak Temperature/time	-	-	26	°C/sec
Maximum Power Dissipation @ +25°C	-	-	3.9	W

*1 Max. must be below 4V at the same time

*2 Max. must be below 1.6V at the same time

* "Absolute Maximum Ratings" are values of safety limit for a device beyond which a device safety cannot be guaranteed.

They do not imply that a device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

8. Recommended Operating Conditions

Table 57. Recommended Operating Conditions

Symbol	Parameter	min.	typ.	max.	Unit
VDDH	Supply Voltage (VDDIO1, VDDIO2)	1.7	-	3.6	V
VDD12	Supply Voltage 1.2V (VDDCORE, VDDRX, VDDTX, VDDPLL)	1.1	-	1.3	V
Ta	Operating Ambient Temperature	-40	-	105	°C

9. Consumption Current

Table 58. Consumption Current at Power Down

symbol	parameter	condition	min.	typ.	max.	unit
ICCS33	Power Down Supply Current	PDN=0, VDDH=3.6V	-	0.1	-	mA
ICCS12		PDN=0, VDD12=1.3V	-	8	-	mA

Table 59. Consumption Current of VDDH

symbol	parameter	condition	min.	typ.	max.	unit
ICCWH_33_1	VDDIO1/2=3.3V	Sub-Link 1lane active	-	16	20	mA
ICCWH_33_2		Sub-Link 2lane active	-	32	38	mA
ICCWH_33_3		Sub-Link 3lane active	-	48	55	mA
ICCWH_33_4		Sub-Link 4lane active	-	64	73	mA
ICCWH_18_1	VDDIO1/2=1.8V	Sub-Link 1lane active	-	14	17	mA
ICCWH_18_2		Sub-Link 2lane active	-	27	32	mA
ICCWH_18_3		Sub-Link 3lane active	-	41	46	mA
ICCWH_18_4		Sub-Link 4lane active	-	55	61	mA

Table 60. Consumption Current of VDD12 at Data stream handling mode1

Symbol	port.in#	port.out#	video format	input	output	min.	typ.	max.	Unit
Iccw12_01	1	1	quasi-1080p low fps	400Mbps x1lane	320Mbps x1lane	-	49	111	mA
Iccw12_02					80Mbps x4lane	-	49	109	mA
Iccw12_157	2		quasi-1080p high fps	4Gbps x2lane selected	800Mbps x4lane	-	177	251	mA
Iccw12_03	1	1	720p30fps RAW	742.5Mbps x1lane	594Mbps x1lane	-	60	123	mA
Iccw12_04			720p30fps YUV422	1Gbps x1lane	600Mbps x1lane	-	64	126	mA
Iccw12_05			720p60fps RAW	1.11375Gbps x1lane	445.5Mbps x2lane	-	65	128	mA
Iccw12_06			1080p30fps RAW			-	65	128	mA
Iccw12_07			720p60fps YUV422	1.485Gbps x1lane	594Mbps x2lane	-	75	139	mA
Iccw12_08			1080p30fps YUV422			-	75	139	mA
Iccw12_09		2			594Mbps x2lane x2port Dist.	-	89	158	mA
Iccw12_10		1	720p120fps RAW	2.2275Gbps x1lane	891Mbps x2lane	-	93	160	mA
Iccw12_11			1080p60fps RAW			-	95	161	mA
Iccw12_12					445.5Mbps x4lane	-	85	150	mA
Iccw12_13			720p120fps YUV422	2.97Gbps x1lane	594Mbps x4lane	-	98	165	mA
Iccw12_14			1080p60fps YUV422			-	100	166	mA
Iccw12_15					1188Mbps x2lane	-	113	184	mA
Iccw12_153		2			1188Mbps x2lane x2port Dist.	-	135	224	mA
Iccw12_B12		1	1080p120fps RAW	2.2275Gbps x2lane	891Mbps x4lane	-	149	238	mA
Iccw12_B13			1080p120fps YUV422	3Gbps x2lane	1200Mbps x4lane	-	184	276	mA
Iccw12_31	2	2	720p30fps RAW	742.5Mbps x1lane x2port	594Mbps x1lane x2port	-	89	148	mA
Iccw12_33			720p30fps YUV422	750Mbps x1lane x2port	600Mbps x1lane x2port	-	90	148	mA
Iccw12_34			720p60fps RAW	1.11375Gbps x1lane x2port	445.5Mbps x2lane x2port	-	102	165	mA
Iccw12_35			1080p30fps RAW			-	102	164	mA
Iccw12_36			720p60fps YUV422	1.485Gbps x1lane x2port	594Mbps x2lane x2port	-	120	186	mA
Iccw12_37			1080p30fps YUV422			-	121	186	mA
Iccw12_38			720p120fps RAW	2.2275Gbps x1lane x2port	891Mbps x2lane x2port	-	151	219	mA
Iccw12_39			1080p60fps RAW			-	153	226	mA
Iccw12_402			720p120fps YUV422	2.97Gbps x1lane x2port	1188Mbps x2lane x2port	-	184	258	mA
Iccw12_412			1080p60fps YUV422			-	188	266	mA

Table 61. Consumption Current of VDD12 at Data stream handling mode2

Symbol	port.in#	port.out#	video format	input	output	min.	typ.	max.	Unit
Iccw12_51	2	1	quasi-1080p low fps	400Mbps x1lane x2port	640Mbps x1lane	-	73	140	mA
Iccw12_52	2				160Mbps x4lane	-	66	132	mA
Iccw12_53	4		quasi-1080p high fps	1.5Gbps x1lane x4port	1200Mbps x4lane	-	199	286	mA
Iccw12_61	2	1	720p30fps RAW	742.5Mbps x1lane x2port	594Mbps x2lane	-	84	153	mA
Iccw12_62	2	1	720p30fps YUV422	750Mbps 1lane x2port	600Mbps x2lane	-	84	154	mA
Iccw12_63	3	1		750Mbps 1lane x3port	900Mbps x2lane	-	115	192	mA
Iccw12_64	4	1		750Mbps 1lane x4port	600Mbps x4lane	-	132	209	mA
Iccw12_65	4	1		750Mbps 1lane x4port	1.2Gbps x2lane	-	147	230	mA
Iccw12_66	4	2	720p30fps YUV422 dist	750Mbps 1lane x4port	1.2Gbps x2lane x2port Dist.	-	165	259	mA
Iccw12_68	2	1	720p60fps RAW	1.11375Gbps 1lane x2port	891Mbps x2lane	-	105	177	mA
Iccw12_69	3	1		1.11375Gbps 1lane x3port	668.25Mbpx x4lane	-	129	207	mA
Iccw12_70	4	1		1.11375Gbps 1lane x4port	891Mbps x4lane	-	165	244	mA
Iccw12_72	2	1	1080p30fps RAW	1.11375Gbps 1lane x2port	891Mbps x2lane	-	105	174	mA
Iccw12_813	4	2		1.11375Gbps 1lane x4port	891Mbps x2lane x2port	-	172	253	mA
Iccw12_73	2	1	720p60fps YUV422	1.485Gbps 1lane x2port	594Mbps x4lane	-	113	187	mA
Iccw12_74	3	1		1.485Gbps 1lane x3port	891Mbps x4lane	-	153	235	mA
Iccw12_75	4	1		1.485Gbps 1lane x4port	1188Mbps x4lane	-	195	281	mA
Iccw12_76	2	1	1080p30fps YUV422	1.485Gbps 1lane x2port	594Mbps x4lane	-	114	184	mA
Iccw12_77	2	1	720p120fps RAW	2.2275Gbps x1lane x2port	891Mbps x4lane	-	142	221	mA
Iccw12_78	2	1	1080p60fps RAW	2.2275Gbps x1lane x2port	891Mbps x4lane	-	144	219	mA
Iccw12_79	2	1	720p120fps YUV422	2.97Gbps x1lane x2port	1188Mbps x4lane	-	173	257	mA
Iccw12_80	2	1	1080p60fps YUV422	2.97Gbps x1lane x2port	1188Mbps x4lane	-	176	255	mA

10. DC Specifications

10.1. LVCMOS DC Specifications

Table 62. LVCMOS DC Specifications

symbol	parameter	pin type	condition	min.	typ.	max.	unit
IIH	LVCMOS Input Leak Current High	IL	VIN=VDDIO1	-	-	10	uA
IIL	LVCMOS Input Leak Current Low	IL	VIN=GND	-10	-	-	uA
VIH	LVCMOS High Level Input Voltage	B	VDDIO1=1.7~2.0V	0.65*VDDIO1	-	VDDIO1	V
			VDDIO1=2.0~3.0V	0.70*VDDIO1	-	VDDIO1	V
			VDDIO1=3.0~3.6V	2.0	-	VDDIO1	V
		IL	VDDIO1=1.7~3.6V	0.70*VDDIO1	-	VDDIO1	V
VIL	LVCMOS Low Level Input Voltage	B	VDDIO1=1.7~2.0V	0	-	0.35*VDDIO1	V
			VDDIO1=2.0~3.0V	0	-	0.30*VDDIO1	V
			VDDIO1=3.0~3.6V	0	-	0.8	V
		IL	VDDIO1=1.7~3.6V	0	-	0.30*VDDIO1	V
VOH	LVCMOS High Level Output Voltage	B,O	IOH=-1mA	VDDIO1-0.45	-	VDDIO1	V
VOL	LVCMOS Low Level Output Voltage	B,O	IOL=1mA	0	-	0.45	V

10.2. CML Receiver DC Specifications

Table 63. CML Receiver DC Specifications

symbol	parameter	condition	min.	typ.	max.	unit
VRTH	CML Differential Input High Threshold	-	-	-	50	mV
VRTL	CML Differential Input Low Threshold	-	-50	-	-	mV
IRIH	CML Input Leak Current High	PDN=L, RXP/N=VDDRX	-	-	±15	uA
IRIL	CML Input Leak Current Low	PDN=L, RXP/N=GND	-	-	±15	uA
IRRIH	CML Input Current High	RXP/N=VDDRX	-	-	1.6	mA
IRRIL	CML Input Current Low	RXP/N=GND	-4.6	-	-	mA
RRIN	CML Differential Input Resistance	-	80	100	120	ohm

10.3. CML Bi-directional Buffer DC Specifications

Table 64. CML Bi-directional Buffer DC Specifications

symbol	parameter	condition	min.	typ.	max.	unit
VBTH	CML Bi-Directional Buffer Differential Input High Threshold	R_BDCZ_HYS=0	-	-	50	mV
		R_BDCZ_HYS=1	-	-	150	mV
VBTL	CML Bi-Directional Buffer Differential Input Low Threshold	R_BDCZ_HYS=0	-50	-	-	mV
		R_BDCZ_HYS=1	-150	-	-	mV
VBIC	CML Bi-Directional Buffer Input Terminated Common Voltage	R_BDCZ_TERM_**= 2'b00 R_BDCZ_DRIVE_**= 2'b00	-	VDDIO2-300	-	mV
IBIH	CML Bi-Directional Buffer Output Leak Current High	RCMP/N=VDDIO2	-10	-	10	uA
IBIL	CML Bi-Directional Buffer Output Leak Current Low	RCMP/N=GND	-10	-	10	uA
VBOD	CML Bi-Directional Buffer Differential Output Voltage	R_BDCZ_TERM_**=2'b10 R_BDCZ_DRIVE_**=2'b10 Diff. 100ohm terminated	200	300	400	mV
VBOC	CML Bi-Directional Buffer Common Output Voltage	R_BDCZ_TERM_**=2'b00 R_BDCZ_DRIVE_**=2'b00	-	VDDIO2-300	-	mV
IBOZ	CML Bi-Directional Buffer TRI-STATE Current	PDN=L	-10	-	10	uA
RTERM	CML Bi-Directional Buffer Termination Registance	R_BDCZ_TERM_**=2'b10	-	50	-	ohm
		R_BDCZ_TERM_**=2'b01	-	100	-	ohm
		R_BDCZ_TERM_**=2'b00	-	200	-	ohm
IDRIVE	CML Bi-Directional Buffer Drive Current	R_BDCZ_DRIVE_**=2'b10	-	12	-	mA
		R_BDCZ_DRIVE_**=2'b01	-	6	-	mA
		R_BDCZ_DRIVE_**=2'b00	-	3	-	mA

10.4. MIPI Transmitter DC Specifications

Table 65. MIPI Transmitter DC Specifications

symbol	parameter	condition	min.	typ.	max.	unit
VTCMTX	HS-mode statics Common-mode Voltage	ZID=80~125ohm	150	200	250	mV
|VTOD|	HS-mode Differential Voltage	ZID=100ohm	140	200	270	mV
VTOHHS	HS-mode High Level Output Voltage	ZID=100ohm	-	-	350	mV
VTOHLP	LP-mode High Level Output Voltage	-	1.1	-	1.3	V
VTOLLP	LP-mode Low Level Output Voltage	-	-0.05	-	0.05	V
ZTOLP	LP-mode Output Impedance	-	110	-	-	ohm

11. AC Specifications

11.1. General AC Specifications

Table 66. General AC Specifications

symbol	parameter	condition	min.	typ.	max.	unit
tDL	Data Latency	MainLink 1Gbps, Data stream handling mode1, 0x1502 - 0x1505 registers are set default value.	typ.-98	16,000	typ.+98	ns

11.2. CML Receiver AC Specifications

Table 67. CML Receiver AC Specifications

symbol	parameter	condition	min.	typ.	max.	unit
tRBIT	Unit Interval	-	250	-	2500	ps
fRBIT		-	0.4	-	4	Gbps

11.3. CML B-directional Buffer AC Specifications

Table 68. CML B-directional Buffer AC Specifications

symbol	parameter	condition	min.	typ.	max.	unit
tBUI	Bi-Directional CML Buffer Unit Interval	-	128.7	137.5	172.7	ns

11.4. 2-wire serial Slave AC Specifications

Table 69. 2-wire serial Slave AC Specifications

symbol	parameter	condition	min.	typ.	max.	unit
tOSC	Cycle of internal oscillator clock	-	11.7	12.5	15.7	ns
fSCL	SCL clock frequency	-	-	-	1000	kHz
tHD;STA	Hold time (repeated) START condition	-	0.26	-	-	us
tLOW	LOW period of the SCL clock	-	0.5	-	-	us
tHIGH	HIGH period of the SCL clock	-	0.26	-	-	us
tSU;STA	Set-up time for a repeated START condition	-	0.26	-	-	us
tHD;DAT	Data hold time: output	-	0	2*tOSC	-	us
	Data hold time: input	-	0	-	-	ns
tSU;DAT	Data setup time: output	-	50	-	-	ns
	Data setup time: input	-	50	-	-	ns
tr	Rise time of both SDA and SCL signals	-	-	-	120(*1)	ns
tf	Fall time of both SDA and SCL signals	pull-up:2.5kΩ, bus capacitance : 400pF	-	-	120	ns
tSU;STO	Setup time for STOP condition	-	0.26	-	-	ns
tBUF	Bus free time between a STOP and START condition	-	0.5	-	-	us
tSP	Pulse width of spikes which must be suppressed by the input filter	-	-	-	50	ns
tPDS	Required wait time from PDN0 high to START condition	-	300	-	-	us

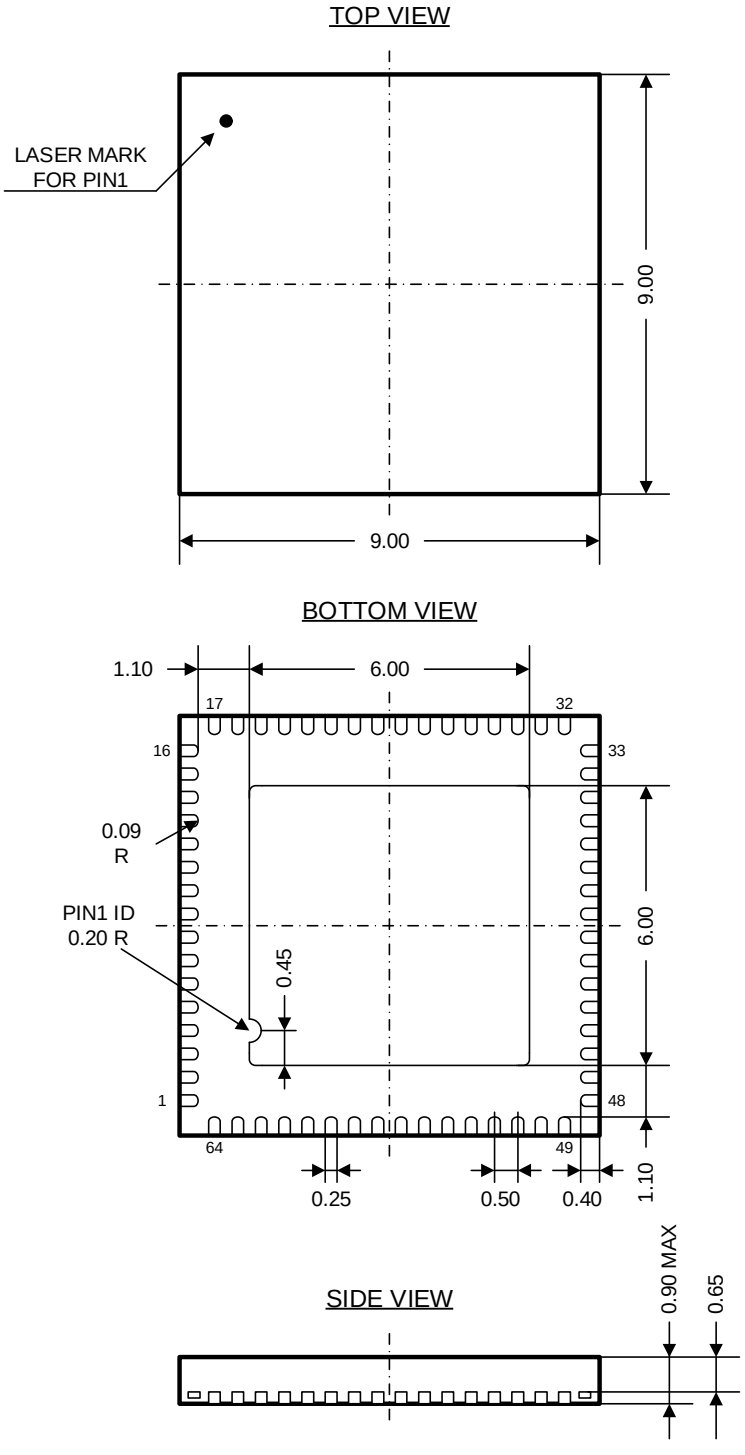
*1 Please adjust Pull-up resistor and bus capacitance to meet the spec value.

11.5. MIPI Transmitter AC Specifications

Table 70. MIPI Transmitter AC Specifications

symbol	parameter	condition	min.	typ.	max.	unit
tTBIT	Tx Unit Interval	-	0.833	-	12.5	ns
fTBIT		-	80	-	1200	Mbps
tCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lanes has transitioned to LP Mode.	tTBIT = 1200Mbps R_TX_CLK_POST* = 0x0F	60+52*tTBIT	-	-	ns
		tTBIT = 600Mbps R_TX_CLK_POST* = 0x0A				
tCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	tTBIT = 1200Mbps	8	-	-	tTBIT
		tTBIT = 600Mbps	4	-	-	
tCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	tTBIT = 1200Mbps R_TX_CLK_PREPARE* = 0x06	38	-	95	ns
		tTBIT = 600Mbps R_TX_CLK_PREPARE* = 0x03				
tCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	tTBIT = 1200Mbps R_TX_CLK_TRAIL* = 0x0C	60	-	-	ns
		tTBIT = 600Mbps R_TX_CLK_TRAIL* = 0x07				
tCLK-PREPARE + tCLK-ZERO	tCLK-PREPARE + Time that the transmitter drives the HS-0 state prior starting the Clock.	tTBIT = 1200Mbps R_TX_CLK_PREPARE* = 0x06 R_TX_CLK_ZERO* = 0x29	300	-	-	ns
		tTBIT = 600Mbps R_TX_CLK_PREPARE* = 0x03 R_TX_CLK_ZERO* = 0x13				
tEOT	Transmitted time interval from the start of tHS-TRAIL or tCLK-TRAIL, to the stat of the LP-11 state following a HS burst.	tTBIT = 1200Mbps R_TX_CLK_TRAIL* = 0x0C R_TX_THS_TRAIL* = 0x0C	-	-	105+12*tTBIT	ns
		tTBIT = 600Mbps R_TX_CLK_TRAIL* = 0x07 R_TX_THS_TRAIL* = 0x07				
tHS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	tTBIT = 1200Mbps R_TX_THS_EXIT* = 0x04	100	-	-	ns
		tTBIT = 600Mbps R_TX_THS_EXIT* = 0x00				
tHS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	tTBIT = 1200Mbps R_TX_THS_PREPARE*= 0x06	40+4*tTBIT	-	85+6*tTBIT	ns
		tTBIT = 600Mbps R_TX_THS_PREPARE*= 0x03				
tHS-PREPARE + tHS-ZERO	tHS-PREPARE + Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	tTBIT = 1200Mbps R_TX_THS_PREPARE* = 0x06 R_TX_THS_ZERO* = 0x10	145+10*tTBIT	-	-	ns
		tTBIT = 600Mbps R_TX_THS_PREPARE* = 0x03 R_TX_THS_ZERO* = 0x06				
tHS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	tTBIT = 1200Mbps R_TX_THS_TRAIL* = 0x0C	60+4*tTBIT	-	-	ns
		tTBIT = 600Mbps R_TX_THS_TRAIL* = 0x07				
tLPX	Transmitted length of any Low-Power state period.	tTBIT = 1200Mbps R_TX_TLPX* = 0x08	50	-	-	ns
		tTBIT = 600Mbps R_TX_TLPX* = 0x04				

12. Package



Unit: mm

13. Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. ("THine") is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.

3. This material contains THine's copyright, know-how or other intellectual property rights. Copying, reverse-engineer or disclosing to third parties the contents of this material without THine's prior written permission is prohibited.

4. THINE ACCEPTS NO LIABILITY FOR ANY DAMAGE OR LOSS IN CONNECTION WITH ANY DISPUTE RELATING TO INTELLECTUAL PROPERTY RIGHTS BETWEEN THE USER AND ANY THIRD PARTY, ARISING OUT OF THIS PRODUCT, EXCEPT FOR SUCH DAMAGE OR LOSS IN CONNECTION WITH DISPUTES SUCCESSFULLY PROVED BY THE USER THAT SUCH DISPUTES ARE DUE SOLELY TO THINE. NOTE, HOWEVER, EVEN IN THE AFOREMENTIONED CASE, THINE ACCEPTS NO LIABILITY FOR SUCH DAMAGE OR LOSS IF THE DISPUTE IS CAUSED BY THE USER'S INSTRUCTION.

5. This product is not designed for applications that require extremely high-reliability/safety such as aerospace device, nuclear power control device, or medical device related to critical care, excluding when this product is specified for automotive use by THine and used it for that purpose. THine accepts no liability whatsoever for any damages, claims or losses arising out of the uses set forth above.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently fail-safe design principles such as redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. This product may be permanently damaged and suffer from performance degradation or loss of mechanical functionality if subjected to electrostatic charge exceeding capacity of the ESD (Electrostatic Discharge) protection circuitry. Safety earth ground must be provided to anything in contact with the product, including any operator, floor, tester and soldering iron.

8. Please note that this product is not designed to be radiation-proof.

9. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.

10. This product must be stored according to storage method which is specified in this specifications. THine accepts no liability whatsoever for any damage or loss caused to the user due to any storage not according to above-mentioned method.

11. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act in Japan and the Export Administration Regulations in the United States of America on export or transit of this product. This product is prohibited for the purpose of developing military modernization, including the development of weapons of mass destruction (WMD), and the purpose of violating human rights.

12. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses. THine accepts no liability whatsoever for any damage or loss caused to the user due to use under a condition exceeding the limiting values.

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