THC63LVDM87

Low power Small package 28bits LVTTL/CMOS to 4ch LVDS Transmitter

General Description

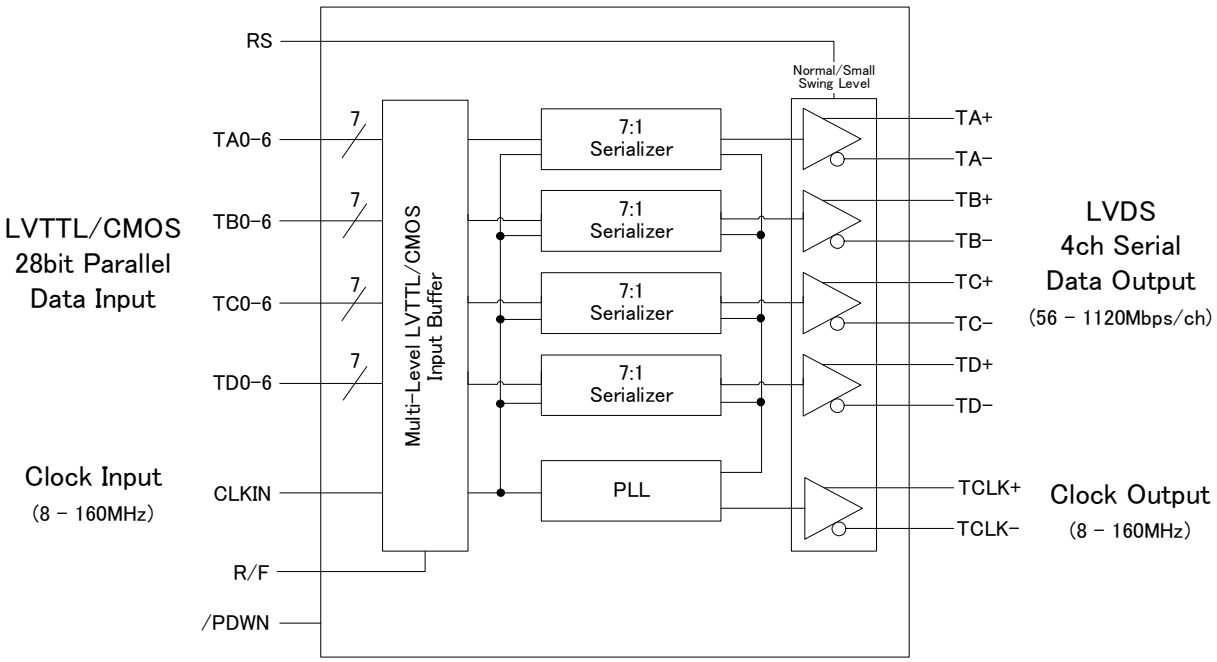
The THC63LVDM87 is a small, low-power LVDS serializer that can be used for flat panel interfaces and many other applications.

The THC63LVDM87 converts 28bits of LVTTL/CMOS parallel data into 4ch LVDS serial data stream.

Features

- Low power 1.8V CMOS design
- 5mm x 5mm/49pin 0.65mm pitch VFBGA Package
- Wide Input clock range: 8-160MHz
- Maximum total throughput 4.48Gbit/s@160MHz
- 3.3/2.5/1.8V LVTTL/CMOS inputs are supported by setting IOVCC=3.3/2.5/1.8V
- LVDS swing is reducible by RS-pin to reduce EMI and power consumption.
- PLL requires no external components.
- Spread Spectrum Clock input tolerant.
- Power down mode.
- Input clock triggering edge is selectable by R/F-pin.
- EU RoHS compliant

Block Diagram



Ball Out

TOP VIEW

	1	2	3	4	5	6	7
A	TA6	TA5	TA4	TA3	TA2	TA1	TA0
B	TB4	TD3	TD2	TD1	TD0	TA-	TA+
C	TB5	TB0	GND	VCC	RS	TB-	TB+
D	TB6	TB1	GND	IO VCC	LVDS VCC	TC-	TC+
E	TC0	TB2	GND	PLL VCC	R/F	TCLK-	TCLK+
F	TC1	TB3	TD4	TD5	TD6	TD-	TD+
G	TC2	TC3	TC4	TC5	TC6	CLKIN	/PDWN

Pin Description

Pin Name	Pin #	Type	Description
TA+, TA-	B7, B6	LVDS Output	4ch Serial Data Output
TB+, TB-	C7, C6		
TC+, TC-	D7, D6		
TD+, TD-	F7, F6		
TCLK+, TCLK-	E7, E6		Clock Output
TA0 ~ TA6	A7,A6,A5,A4,A3,A2,A1	3.3/2.5/1.8V LVTTL/CMOS Digital Input	28bit Parallel Data Input
TB0 ~ TB6	C2,D2,E2,F2,B1,C1,D1		
TC0 ~ TC6	E1,F1,G1,G2,G3,G4,G5		
TD0 ~ TD6	B5,B4,B3,B2,F3,F4,F5		
CLKIN	G6		Clock Input
/PDWN	G7		Power Down Control H: Normal operation L: Power Down (All output are Hi-Z.)
R/F	E5		Input Clock Triggering Edge Select H : Rising edge L : Falling edge
RS	C5		LVDS output swing level (VOD) select H : 350mV L : 200mV
VCC	C4	Power	Power Supply Pin for LVTTL/CMOS input and digital circuit.
IOVCC	D4		Power Supply Pins for CMOS IO Inputs
LVDSVCC	D5		Power Supply Pins for LVDS Outputs.
PLLVCC	E4		Power Supply Pin for PLL circuit.
GND	C3,D3,E3		Ground Pins for Common

Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (IOVCC)	-0.3	+4.0	V
Supply Voltage (VCC / LVDSVCC / PLLVCC)	-0.3	+2.1	V
LVTTL/CMOS Input Voltage	-0.3	IOVCC + 0.3	V
LVDS Transmitter Output Voltage	-0.3	LVDSVCC + 0.3	V
LVDS Total Output Current	-50	+50	mA
Junction Temperature	-	+125	°C
Storage Temperature	-55	+125	°C
Reflow Peak Temperature	-	+260	°C
Reflow Peak Temperature Time	-	10	sec
Maximum Power Dissipation @+25°C	-	1.3	W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (IOVCC)	1.62	1.8/2.5/3.3	3.6	V
Supply Voltage (VCC / LVDSVCC / PLLVCC)	1.62	1.8	1.98	V
Operating Ambient Temperature (Ta)	-40	25	+85	°C
Clock Frequency (CLKIN / TCLK)	8	-	160	MHz

Supply Current

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Typ[(a)]	Max[(b)]	Units
I_{TCCW}	Supply Current	RL=100Ω, CL=5pF, f=37MHz RS=VCC, (RS=GND)	25 (19)	33 (27)	mA
		RL=100Ω, CL=5pF, f=71MHz RS=VCC, (RS=GND)	30 (24)	46 (40)	mA
		RL=100Ω, CL=5pF, f=160MHz RS=VCC, (RS=GND)	44 (38)	79 (73)	mA
I_{TCCS}	Power Down Current		1	50	µA

(a) All Typ. Values are at VCC=1.8V, Ta=25°C. The 16 Grayscale Pattern (Figure 1.) inputs test for a typical display pattern

(b) All Max. Values are at VCC=1.98V, Ta=85°C. The Worst Case Pattern (Figure 2.) produces maximum switching frequency for all the LVDS outputs

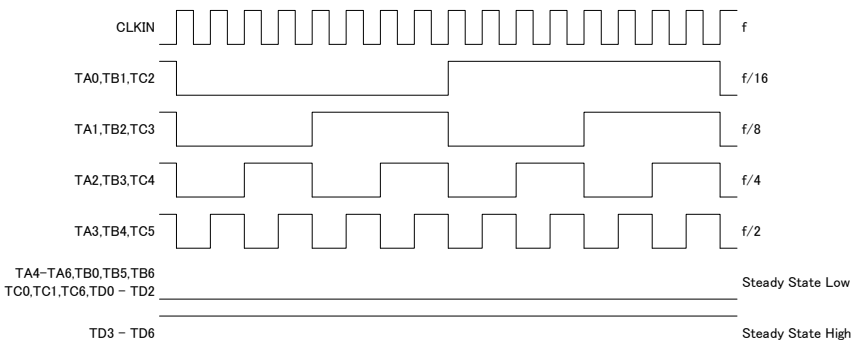


Figure 1. 16 Grayscale Pattern

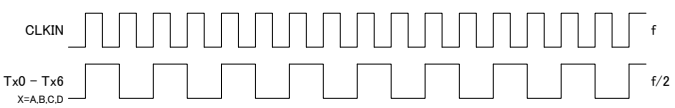


Figure 2. Worst Case Pattern

LVTTL/CMOS DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	IOVCC=1.62 ~ 1.98V	0.65 IOVCC	-	IOVCC	V
		IOVCC=2.3 ~ 2.7V	1.7	-	IOVCC	
		IOVCC=3.0 ~ 3.6V	2.0	-	IOVCC	
V_{IL}	Low Level Input Voltage	IOVCC=1.62 ~ 1.98V	GND	-	0.35IOVCC	V
		IOVCC=2.3 ~ 2.7V	GND		0.7	
		IOVCC=3.0 ~ 3.6V	GND	-	0.8	
I_{INC}	Input Current	GND ≤ V_{IN} ≤ IO VCC	-	-	±10	μA

LVDS DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOD	Differential Output Voltage	RS=VCC RL=100Ω	250	350	450	mV
		RS=GND RL=100Ω	140	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω	-	-	35	mV
VOC	Common Mode Voltage	RL=100Ω	1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states	RL=100Ω	-	-	35	mV
I_{OS}	Output Short Circuit Current	V_{OUT}=GND, RL=100Ω	-	-	100	mA
I_{OZ}	Output TRI-STATE Current	/PDWN=GND, V_{OUT}=GND to LVDSVCC	-	-	±20	μA

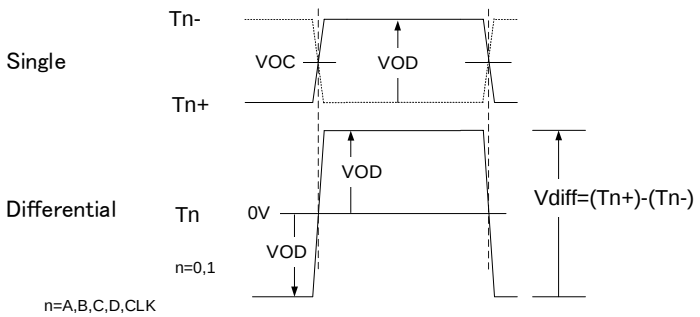


Figure 3. LVDS DC Specifications

LVTTL/CMOS AC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
t_{TCP}	CLKIN Period	6.25	T	125	ns
t_{TCH}	CLKIN High Time	0.35T	0.5T	0.65T	ns
t_{TCL}	CLKIN Low Time	0.35T	0.5T	0.65T	ns
t_{TS}	Tx0-6 Setup time to CLKIN	2.0	-	-	ns
t_{TH}	Tx0-6 Hold time to CLKIN	0.0	-	-	ns

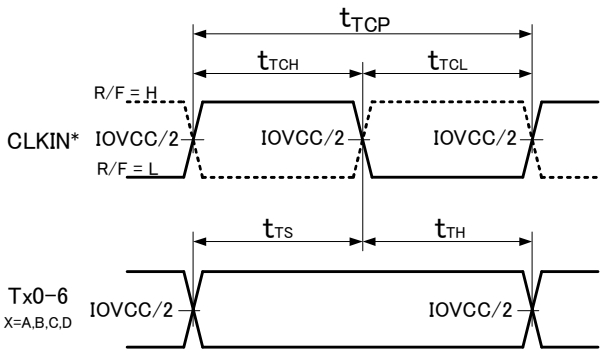


Figure 4. CLKIN and Tx0-6 Input Timings

LVDS AC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
t_{LVT}	LVDS Transition Time	-	0.6	1.5	ns
t_{TOP1}	Output Data Position0 (T=6.25ns ~ 20ns)	-0.15	0.0	+0.15	ns
t_{Top0}	Output Data Position1 (T=6.25ns ~ 20ns)	T/7-0.15	T/7	T/7+0.15	ns
t_{Top6}	Output Data Position2 (T=6.25ns ~ 20ns)	2T/7-0.15	2T/7	2T/7+0.15	ns
t_{Top5}	Output Data Position3 (T=6.25ns ~ 20ns)	3T/7-0.15	3T/7	3T/7+0.15	ns
t_{Top4}	Output Data Position4 (T=6.25ns ~ 20ns)	4T/7-0.15	4T/7	4T/7+0.15	ns
t_{Top3}	Output Data Position5 (T=6.25ns ~ 20ns)	5T/7-0.15	5T/7	5T/7+0.15	ns
t_{Top2}	Output Data Position6 (T=6.25ns ~ 20ns)	6T/7-0.15	6T/7	6T/7+0.15	ns

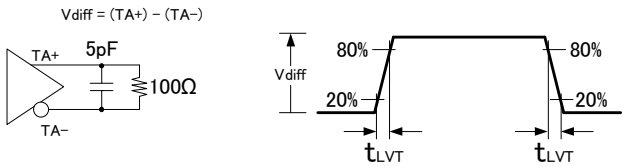


Figure 5. LVDS Output Load and Transmission Time

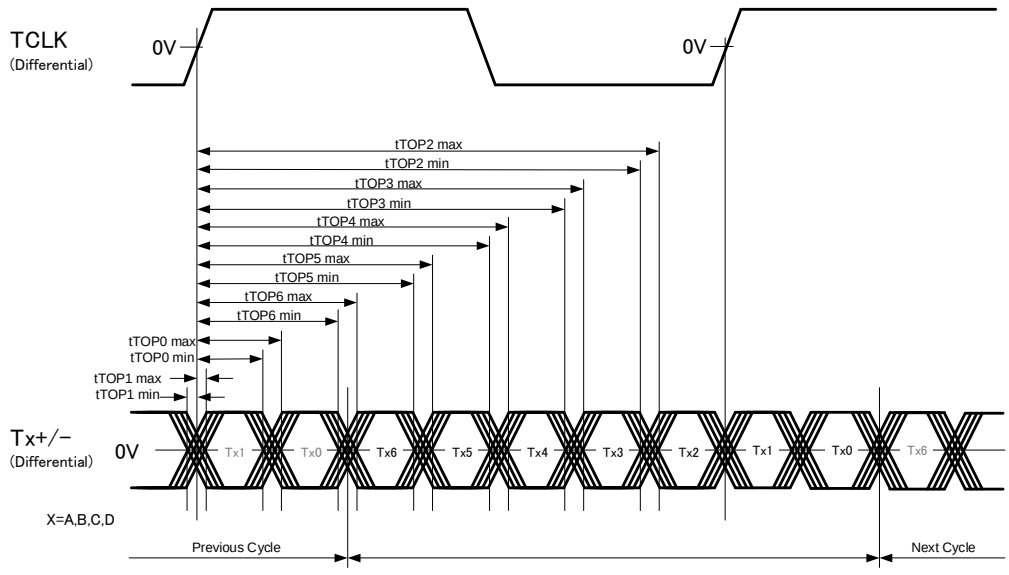


Figure 6. LVDS Output Data Position

Power On Sequence

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
t1	VCC to CLKIN	0	-	-	ms
t2	VCC to /PDWN	0	-	-	ms
t_{TPLL}*	Phase Lock Loop Set	-	-	10.0	ms
t_{TCD}	CLKIN to TCLK+/- Delay	5T+3.1	-	5T+8	ns

*The time until a stable TCLK is output starting from t1 or t2, whichever is later.

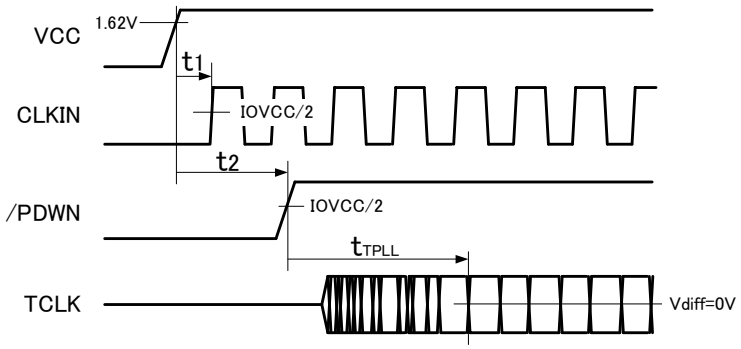


Figure 7. Power On Sequence

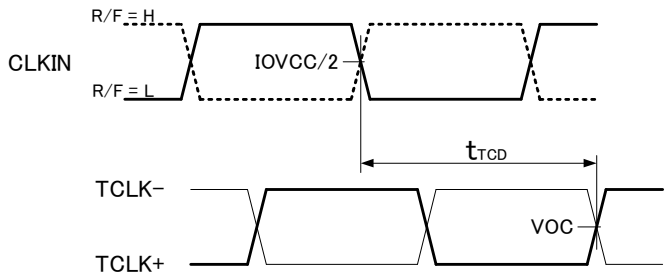


Figure 8. CLKIN to TCLK+/- Delay

Note

1) Cable Connection and Disconnection

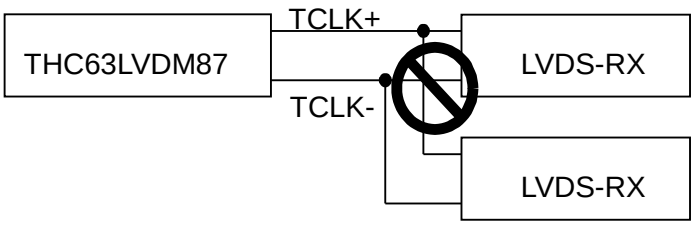
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection

Connect the each GND of the PCB which THC63LVDM83E and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

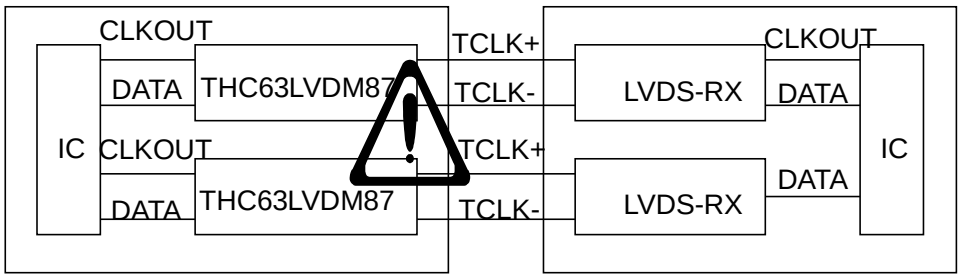
3) Multi Drop Connection

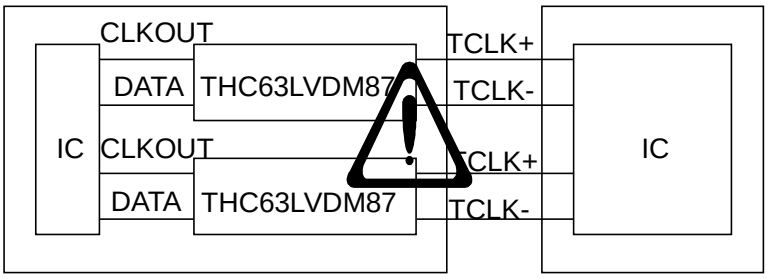
Multi drop connection is not recommended.



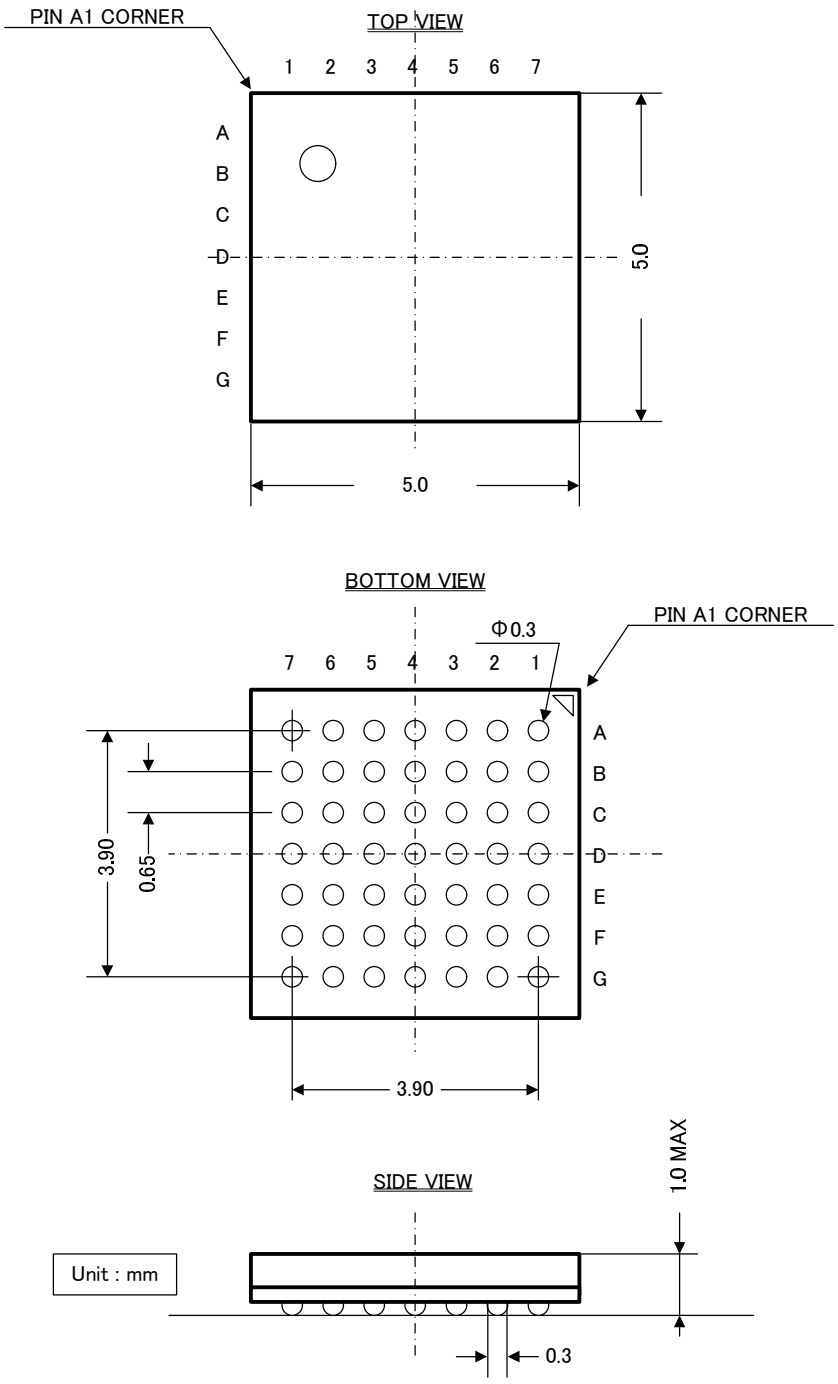
4) Asynchronous use

Asynchronous using such as following systems are not recommended.





Package


PIN A1 CORNER
TOP VIEW
1 2 3 4 5 6 7
A
B
C
D
E
F
G
5.0
5.0
BOTTOM VIEW
Φ0.3
PIN A1 CORNER
7 6 5 4 3 2 1
A
B
C
D
E
F
G
3.90
0.65
3.90
SIDE VIEW
1.0 MAX
Unit : mm
0.3

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