IQS7225A DATASHEET

6-channel device, self-capacitance, mutual-capacitance and inductive sensing modes, relative encoder UI, I²C communication interface, low-power mode options

1 Device Overview

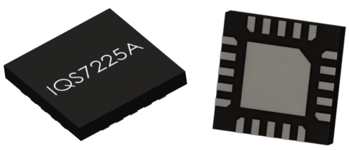
The IQS7225A ProxFusion® IC is a sensor fusion device that is mainly aimed at inductive sensing applications that require relative encoder inductive sensing and/or multiple inductive buttons. The device also has capacitive sensing capabilities that can be used to complement the inductive sensing applications, e.g. a capacitive wakeup channel. The sensor is fully I²C compatible and on-chip calculations enable the IC to respond effectively even in its lowest power modes.

1.1 Main Features

- Highly flexible ProxFusion® device
- 9 (QFN) external sensor pad connections
- Configure up to 6 channels using the external connections
- External sensor options:
  - Up to 6x self-capacitive buttons
  - Up to 6x mutual-capacitive buttons
  - Up to 6x inductive buttons
- Built-in basic functions:
  - Gray-coded relative Encoder
  - Selectable channel reference
    - LTA as reference
    - select channel to use as reference
    - fixed value as reference
  - Blocking channel
  - Automatic Tuning Implementation (ATI)
  - Noise filtering
  - Debounce & hysteresis
  - Dual direction trigger indication
- Built-in signal processing options:
  - Encoder angle
  - Encoder counter
  - Encoder state
- PC software for debugging and obtaining optimal settings and performance
- Programmed memory map settings for simplified integration
- Multi-level trigger implementation:
  - Adjustable number of trigger levels
  - Trigger event states
- Design simplicity
- Automated system power modes for optimal response vs consumption
- I²C communication interface with IRQ/RDY (up to fast plus – 1 MHz)
- I²C address selection using GPIO pin
- Event and streaming modes
- Customizable user interface due to programmable memory
- Supply voltage range:
  - 1.8 V to 3.5 V (F_{OSC} = 14 MHz)
  - 2.2 V to 3.5 V (F_{OSC} = 18 MHz)
- Small packages
  - QFN20 (3 x 3 x 0.5 mm) – 0.4 mm pitch

RoHS2
Compliant

QFN20 package
Representation only



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1.2 Applications

- Waterproof inductive dial/counter applications
- Integrated control panel (dial + buttons)
- Wearables
- Waterproof inductive buttons
- White goods user interface
- Smart home controllers

1.3 Block Diagram

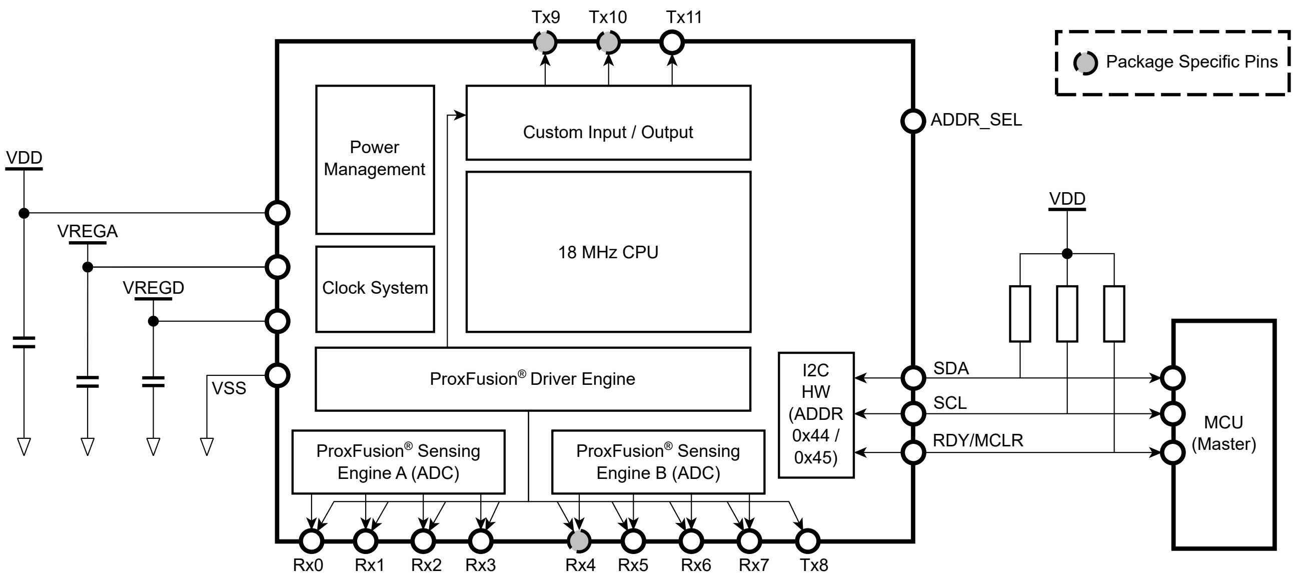

Figure 1.1: Functional Block Diagram

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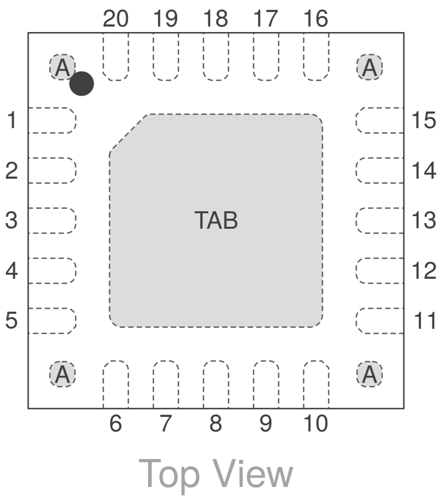
2 Hardware Connection

2.1 QFN20 Pin Diagram

Table 2.1: 20-pin QFN Package (Top View)



Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	Rx6/Tx6
2	VREGD	12	Rx7/Tx7
3	VSS	13	Tx8/VBias
4	VREGA	14	Tx9
5	Rx0/Tx0	15	Tx10
6	Rx1/Tx1	16	Tx11
7	Rx2/Tx2	17	ADDR
8	Rx3/Tx3	18	SCL
9	Rx4/Tx4	19	SDA
10	Rx5/Tx5	20	MCLR/RDY

Area name	Signal name
TAB[i]	Thermal pad (floating)
A[ii]	Thermal pad (floating)

2.2 Pin Attributes

Table 2.2: Pin Attributes

Pin no. QFN20	Signal name	Signal type	Buffer type	Power source
1	VDD	Power	Power	N/A
2	VREGD	Power	Power	N/A
3	VSS	Power	Power	N/A
4	VREGA	Power	Power	N/A
5	Rx0/Tx0	Analog		VREGA
6	Rx1/Tx1	Analog		VREGA
7	Rx2/Tx2	Analog		VREGA
8	Rx3/Tx3	Analog		VREGA
9	Rx4/Tx4	Analog		VREGA
10	Rx5/Tx5	Analog		VREGA
11	Rx6/Tx6	Analog		VREGA
12	Rx7/Tx7	Analog		VREGA
13	Tx8/VBias	Analog		VREGA
14	Tx9	Prox/Digital		VREGA/VDD
19	SDA	Digital		VDD
18	SCL	Digital		VDD
15	Tx10	Prox/Digital		VREGA/VDD
16	Tx11	Prox/Digital		VREGA/VDD
17	ADDR	Digital		VDD
20	MCLR/RDY	Digital		VDD

[i] It is recommended to connect the thermal pad (TAB) to VSS.
[ii] Electrically connected to TAB. These exposed pads are only present on *–QNR* order codes.

2.3 Signal Descriptions

Table 2.3: Signal Descriptions

Function	Signal name	Pin no. QFN20	Pin type[iii]	Description
ProxFusion®	Rx0/Tx0	5	IO	ProxFusion® channel
	Rx1/Tx1	6	IO	
	Rx2/Tx2	7	IO	
	Rx3/Tx3	8	IO	
	Rx4/Tx4	9	IO	
	Rx5/Tx5	10	IO	
	Rx6/Tx6	11	IO	
	Rx7/Tx7	12	IO	
	Tx8/VBias	13	O	Tx8/VBias pad
	Tx9	14	IO	Tx9 pad
	Tx10	15	IO	Tx10 pad
	Tx11	16	IO	Tx11 pad
GPIO	ADDR	17	I	ADDR pad
	MCLR/RDY	20	IO	Active pull-up, 200kΩ resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP.
I^2C	SDA	19	IO	I^2C data
	SCL	18	IO	I^2C clock
Power	VDD	1	P	Power supply input voltage
	VREGD	2	P	Internal regulated supply output for digital domain
	VSS	3	P	Analog/digital ground
	VREGA	4	P	Internal regulated supply output for analog domain

[iii] Pin Types: I = Input, O = Output, IO = Input or Output, P = Power.

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2.4 Reference Schematic

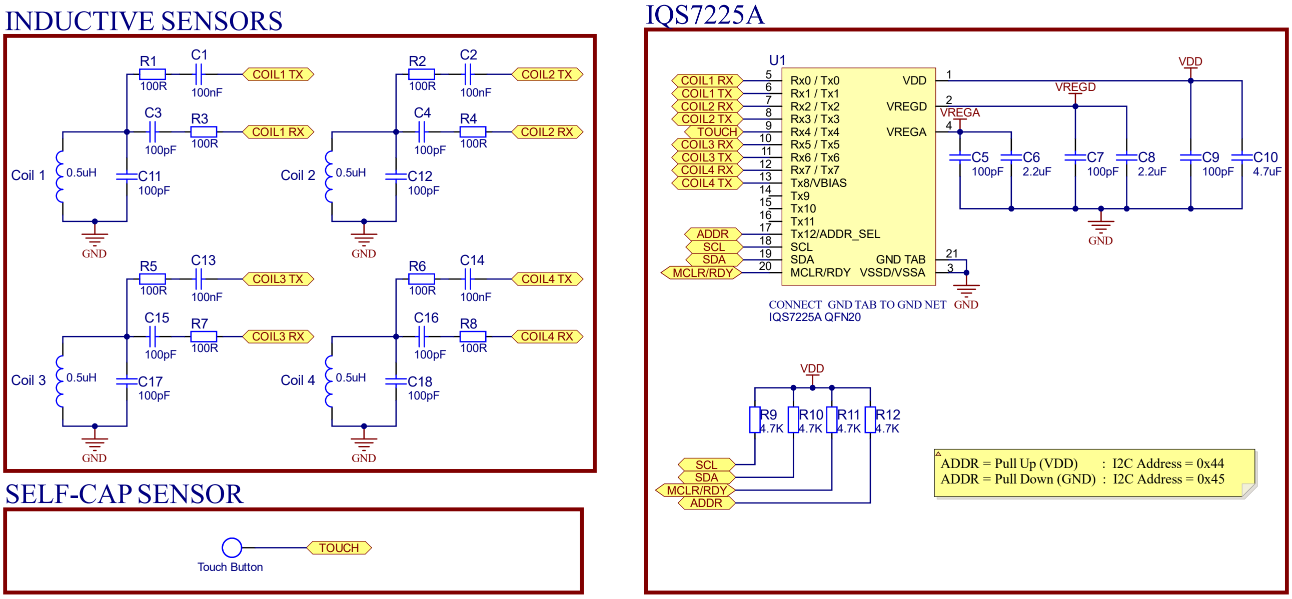

Figure 2.1: 4x Inductive Coils and 1x Self Capacitance Reference Schematic

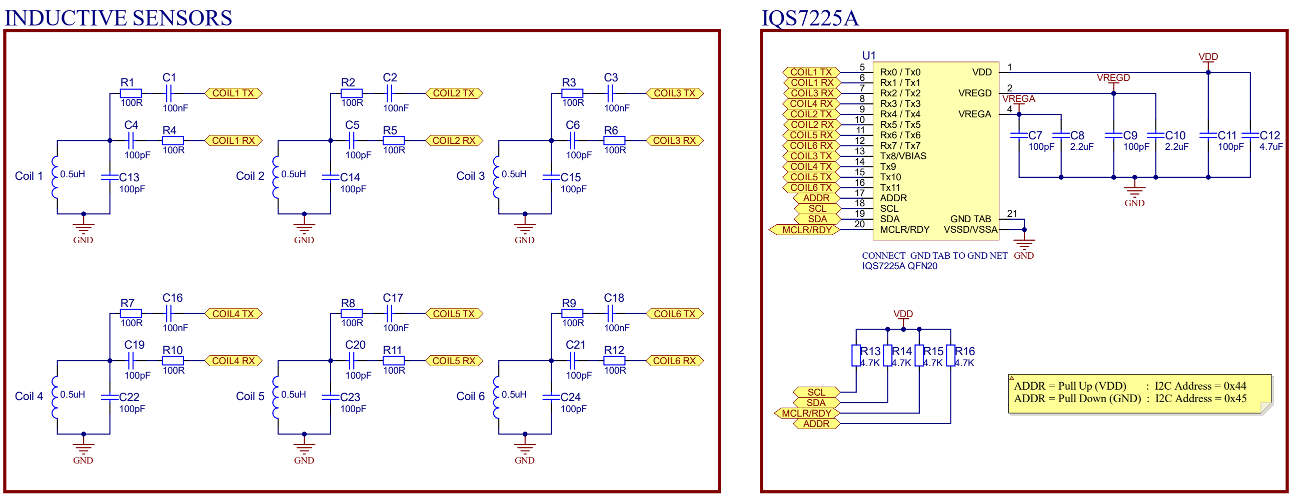

Figure 2.2: 6x Inductive Coils Reference Schematic

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3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.5	V
Voltage applied to any ProxFusion® pin (referenced to VSS)	−0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	−0.3	VDD + 0.3 (3.5 V max)	V
Storage temperature, T_{stg}	−40	85	°C

3.2 Recommended Operating Conditions

Table 3.2: Recommended Operating Conditions

		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: F_{OSC} = 14 MHz F_{OSC} = 18 MHz	 1.71 2.2		 3.5 3.5	V
VREGA	Internal regulated supply output for analog domain: F_{OSC} = 14 MHz F_{OSC} = 18 MHz	 1.49 1.7	 1.53 1.75	 1.57 1.79	V
VREGD	Internal regulated supply output for digital domain: F_{OSC} = 14 MHz F_{OSC} = 18 MHz	 1.56 1.75	 1.59 1.8	 1.64 1.85	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	−40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2\times C_{VREGA}$	$3\times C_{VREGA}$		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR$\leq$ 200 mΩ	2	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR$\leq$ 200 mΩ	2	4.7	10	µF
$Cx_{SELF-VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1		400[i]	pF
Cm_{Tx-Rx}	Capacitance between Receiving and Transmitting electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.2		9[i]	pF
Cp_{Rx-VSS}	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks Mutual-capacitance mode, f_{xfer} = 1 MHz Mutual-capacitance mode, f_{xfer} = 4 MHz			 100[i] 25[i]	pF
$\frac{Cp_{Rx-VSS}}{Cm_{Tx-Rx}}$	Capacitance ratio for optimal SNR in mutual-capacitance mode[ii]	10		20	n/a
$RCx_{Rx/Tx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[iii]	0.47	10[iv]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iii]	0.47	10[iv]	kΩ

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3.3 ESD Rating

Table 3.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[v]	±4000	V

[i]RCx = 0 Ω.
[ii]Please note that the maximum values for Cp and Cm are subject to this ratio.
[iii]Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.
[iv]Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6 \times f_{xfer})}$ where C is the pin capacitance to VSS.
[v]JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

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3.4 Current Consumption

Sensing Mode:	: Inductive
Number of Inductive Channels	: 6
Number of Cycles	: 6
ATI Target	: 256
ATI Base	: 256
Tx Frequency	: HFosc
Charge transfer frequency	: 4.50 MHz (HFosc = 18MHz) or 3.50 MHz (HFosc = 14MHz)
Tx Impedance	: 20kΩ
Interface Selection	: Event Mode

Table 3.4: Power Mode Current Consumption

Power mode	Report rate (sampling rate) [ms]	Typical current [μA]		
		Order code: 001[i] HFosc: 18MHz	Order code: 101 HFosc: 14MHz	Order code: 101 HFosc: 18MHz
Normal power / low-power	10	442	500	518
	16	244	257	260
	25	160	167	170
	50	81	85	87
	100	42	44	45
	150	28	30	31
Ultra low-power	150	-	20	10
	500+	-	7	4

[i]Please refer to product information notice PIN-230172 for more details.

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4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Typ	Max	Unit
V_{VDD}	Power-up/down level (Reset trigger) – slope > 100 V/s	1.040	1.353	1.568	V
V_{VREGD}	Power-up/down level (Reset trigger) – slope > 100 V/s	0.945	1.122	1.304	V

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS − 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

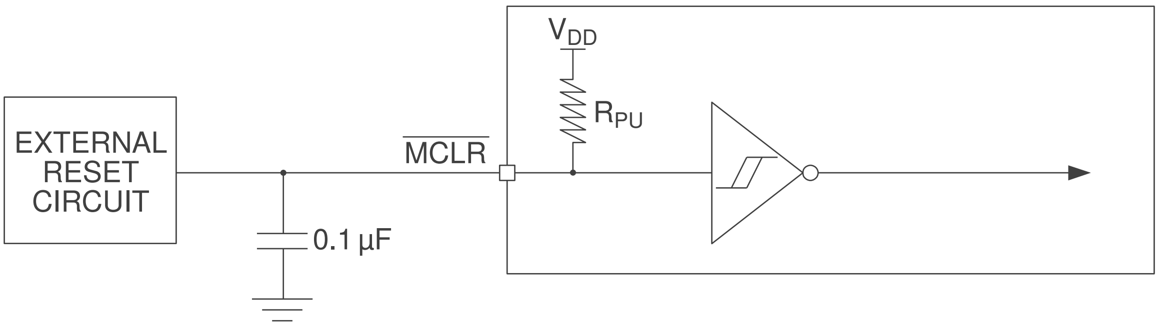

Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
f_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz
f_{OSC}	Master CLK frequency tolerance 18 MHz	17.1	18	19.54	MHz
f_{xfer}	Charge transfer frequency (derived from f_{OSC})	42	500 – 1500	4500	kHz

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4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OL}	SDA & SCL Output low voltage	I_{sink} = 20 mA			0.3	V
V_{OL}	GPIO[i] Output low voltage	I_{sink} = 10 mA			0.15	V
V_{OH}	Output high voltage	I_{source} = 20 mA	VDD − 0.2			V
V_{IL}	Input low voltage				VDD × 0.3	V
V_{IH}	Input high voltage		VDD × 0.7			V
C_{b_max}	SDA & SCL maximum bus capacitance				550	pF

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		VDD	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	1.8 V, 3.3 V			1000	kHz
$t_{HD,STA}$	Hold time (repeated) START	1.8 V, 3.3 V	0.26			µs
$t_{SU,STA}$	Setup time for a repeated START	1.8 V, 3.3 V	0.26			µs
$t_{HD,DAT}$	Data hold time	1.8 V, 3.3 V	0			ns
$t_{SU,DAT}$	Data setup time	1.8 V, 3.3 V	50			ns
$t_{SU,STO}$	Setup time for STOP	1.8 V, 3.3 V	0.26			µs
t_{SP}	Pulse duration of spikes suppressed by input filter	1.8 V, 3.3 V	0		50	ns

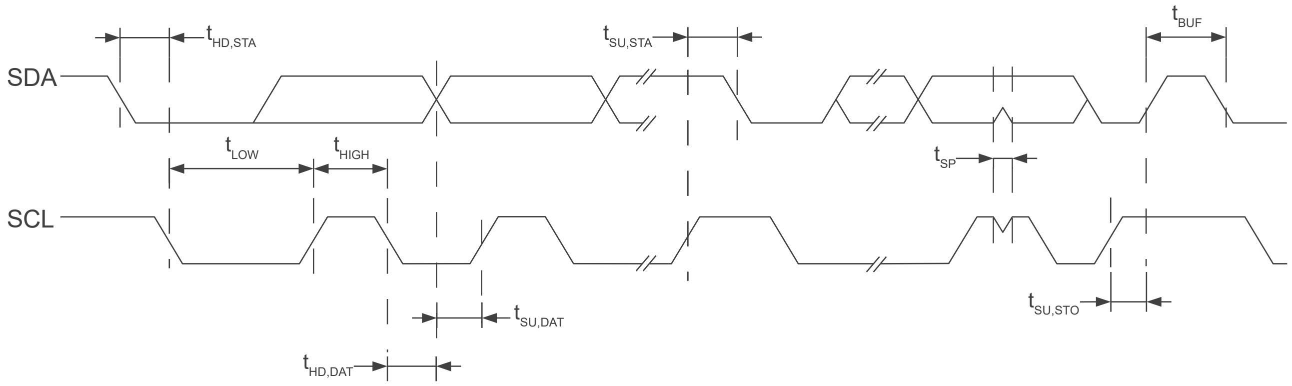

Figure 4.2: I²C Mode Timing Diagram

[i] Refers to Tx9, Tx10, Tx11, and ADDR pins.

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5 ProxFusion® Module

The IQS7225A contains dual ProxFusion® modules that use patented technology to measure and process the sensor data. Two modules ensure a rapid response from multichannel implementations. The different primary sensor outputs are proximity, touch, and deep touch. Other sensor outputs are the channel trigger levels, and the Encoder angle and counter.

5.1 Channel Options

Self-capacitance, mutual capacitance, reference tracking and inductive designs are possible with the IQS7225A.

- Sensor pad design overview: AZD125
- Mutual capacitance button layout guide: AZD125
- Inductive design layout guide: AZD115

5.2 Low-Power Options

The IQS7225A offers 4 power modes:

- Normal power mode (NP)
  - Flexible channel scan rate
- Low-power mode (LP)
  - Flexible channel scan rate
  - Typically set to a slower rate than NP
- Ultra-low power mode (ULP)[i]
  - Optimised firmware setup
  - Intended for rapid wake-up on a single channel (e.g. distributed proximity event), enabling immediate button response for an approaching user
  - Other sensor channels are typically sampled at a slower rate in order to optimise power consumption
- Halt power mode
  - Intended for use during shipping and storage of battery-operated assemblies
  - No conversions carried out on any of the channels

5.3 Count Value

The sensing measurement returns a *count value* for each channel. Count values are inversely proportional to capacitance/inductance, and all outputs are derived from this.

5.4 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value. The reference value/LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.

5.4.1 Channel Reseed

Since the *Reference* for a channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts,

[i]Note: device settings should not be written in ULP mode.

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and seeds the *reference/LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the corresponding bit (register 0x2000, bit3).

5.4.2 Encoder Fixed Reference

The IQS7225A encoder fixed reference refers to the LTA that is used for the encoder channels. If the value assigned to the encoder fixed reference is less than six, then the LTA of the channel with channel number equal to the assign value, is set as the encoder channel's LTA. If the value assigned is greater than or equal to six, then the encoder channel's LTA equals the assigned value multiplied by eight.

5.4.3 Count and LTA Reseed

The IQS7225A offers useful calibration features such as the channel count reseed and the channel LTA reseed. The channel count and LTA reseed command bits can be set as described in Table A.11. Setting the count reseed command bit to a '1' means that a reseed of the channel count filter will occur. Setting the channel LTA reseed command bit to a '1' means that the LTA overwrite value for the channel is used to seed the current LTA value.

5.5 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the new ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances and inductances, without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please contact Azoteq.

5.6 Automatic Re-ATI

5.6.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI compensation to be configured, since the user affects the capacitance or inductance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled. When a Re-ATI is performed on the IQS7225A, a status bit will be set momentarily to indicate that this has occurred.

5.6.2 Conditions for Re-ATI to activate

A Re-ATI is performed when the reference of a channel drifts outside of the acceptable range from the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in registers listed in Table A.24.

$$\textbf{Re-ATI Boundary= ATI target} \pm (\tfrac{1}{8}\textbf{ATI Target})$$

For example, assume that the ATI target is configured to 800 and the boundary value is $\frac{1}{8} \times 800 = 100$. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

$$\textbf{Reference} > \textbf{900 or Reference} < \textbf{700}$$

The ATI algorithm executes in a short time, so it goes unnoticed by the user.

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5.6.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if one of the following conditions is true for any channel after the ATI is completed:

- ATI Compensation = 0 (min value)
- ATI Compensation = 1023 (max value)
- Count is already outside the Re-ATI range upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set (*ATI Error*). The flag status is only updated again when a new ATI algorithm is performed.

Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI error timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. An ATI error should however not occur under normal circumstances.

5.7 Channel Outputs

5.7.1 Channel Proximity

A channel proximity event occurs when the channel proximity threshold has been reached. For inductive sensors this happens when a metal segment comes into close proximity with any of the coils. For a capacitive sensor this occurs when a user's finger, or a conductive object, comes into close proximity with the sensor. A channel proximity output is debounced (see Table A.16), and the proximity threshold configured is a delta value (see Table A.16) measuring how much a channel's count value has deviated from the reference/LTA value.

5.7.2 Channel Touch and Deep Touch

Channel touch and deep touch events occur when the touch and deep touch thresholds have been reached respectively. Touch and deep touch thresholds can be calculated as:

$$\textbf{Threshold} = \textbf{value} \times \frac{\textbf{LTA}}{\textbf{256}} \tag{1}$$

Here value refers to the value entered into the register and threshold refers to the number that is calculated from the underlinevalue and subsequently compared to the count delta to determine whether there is a touch/deep touch event. The touch and deep touch hysteresis values determine the corresponding touch and deep touch release thresholds. Release threshold can be calculated as:

$$\textbf{Release threshold} = \frac{\textbf{LTA}}{\textbf{256}} \times \textbf{(Threshold value - Hysteresis value)} \tag{2}$$

Here both threshold value and hysteresis value are configurable parameters in the memory map and release threshold is calculated from these values and compared to the count delta to determine whether a touch/deep touch event should be cleared.

5.7.3 Encoder Angle and Counter

The IQS7225A offers the ability to configure two inductive coils to provide additional encoder outputs such as:

(a) Encoder angle
(b) Encoder count

The encoder angle is a value between 0 and $360°$ representing integer multiples of the coil separation angle (θ_{coil}) as shown in Table 5.2. The encoder counter is incremented or decremented in steps of 1, representing the change in the position of the wheel metal target. The encoder coil separation and the number of positions per revolution depends on the number of wheel metal targets (see Table 5.2).

5.7.4 Multi-Level Triggers

The IQS7225A offers multi-level trigger settings with adjustable number of trigger levels for each channel. Trigger events are activated when there is a transition in the trigger levels on any channel. To setup multi-level triggers on a channel, the channel maximum delta value and the desired number of trigger levels must be selected. The channel output trigger level can be calculated as shown below.

$$\textbf{Channel output trigger level} = \frac{\textbf{Max delta}}{\textbf{Number of trigger levels}} \tag{3}$$

5.8 Power Mode Timeout

In order to optimise power consumption and performance, power modes are “stepped” by default in order to move to power efficient modes when no interaction has been detected for a certain (configurable) time, known as the “power mode timeout”.

5.9 Count Filter

5.9.1 IIR Filter

The IIR filter applied to the digitised raw input offers various damping options as defined in Table A.21 and Table A.22

$$\textbf{Damping factor} = \frac{\textbf{Beta}}{\textbf{256}} \tag{4}$$

Where Beta is a configurable register value.

5.10 Inductive Encoder Design

A simple relative encoder sensor is implemented by spacing coils at a specified angle along the outer diameter of a rotating dial. The dial has a metal target pattern that encodes unique inductive states of the coils. The encoded states of the coils are used to determine the relative rotation of the dial.

5.10.1 Basic Encoder Principle

The basic geometry of the encoder has 2 coils separated by angle $\theta_{coil} = 90°$ and a metal target that spans $2 \cdot \theta_{coil} = 180°$ as shown in Figure 5.1. This coil-target configuration is capable of discerning 4 discrete Gray encoded positions at $90°$ intervals (see Table 5.1). When the metal target is fully covering the coil, the state of the coil is represented by ‘1’ and when the metal target is completely clear of the coil the state of the coil is represented by ‘0’.

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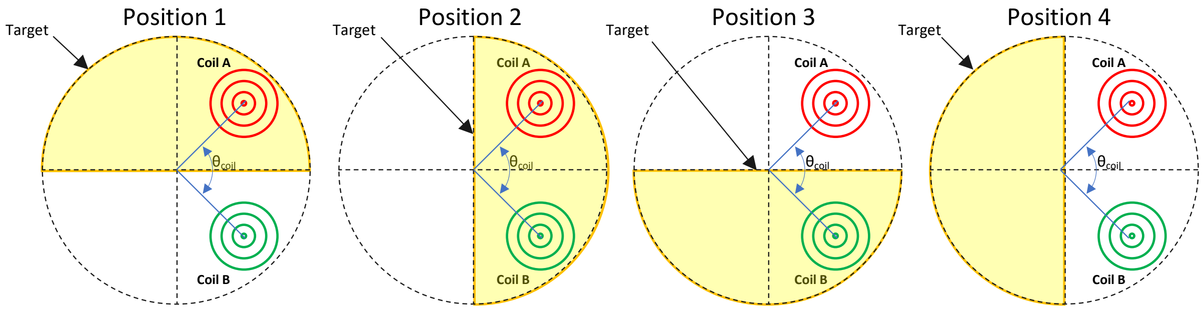

Figure 5.1: 4x Position Inductive Encoder

Table 5.1: Coil - Target Gray encoded states

Position	Angle	Gray Encoded State	
		Coil A	Coil B
1	0°	1	0
2	90°	1	1
3	180°	0	1
4	270°	0	0

5.10.2 Encoder Resolution

The configuration in Figure 5.1 has a resolution of 90°. Higher resolution encoders can be defined with a smaller θ_{coil}. By changing the coil separation angle (θ_{coil}) and the target span geometry ($2 \cdot \theta_{coil}$), the resolution of the encoder can be defined.

Table 5.2: Encoder resolution geometry

Positions per Rev	Coil Separation θ_{coil}	Target Span $2 \cdot \theta_{coil}$	Target Separation $2 \cdot \theta_{coil}$	Number of Targets
4	90°	180°	180°	1
8	45°	90°	90°	2
12	30°	60°	60°	3
16	22.5°	45°	45°	4
20	18°	36°	36°	5
24	15°	30°	30°	6
28	12.86°	25.71°	25.71°	7
32	11.25°	22.50°	22.50°	8
N	360°/N	2 · 360°/N	2 · 360°/N	N/4

5.10.3 32 Position Encoder Geometry

The following geometry defines a 32-position encoder:

- Coil separation = 11.25°

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- Target span = 22.50°
- Target separation = 22.50°
- Number of targets = 8

Each one of the target sections can discern 4 Gray encoded positions as shown in Figure 5.2. There are 8 target sections, thus for a full rotation of the dial there is a total of $4 \times 8 = 32$ positions.

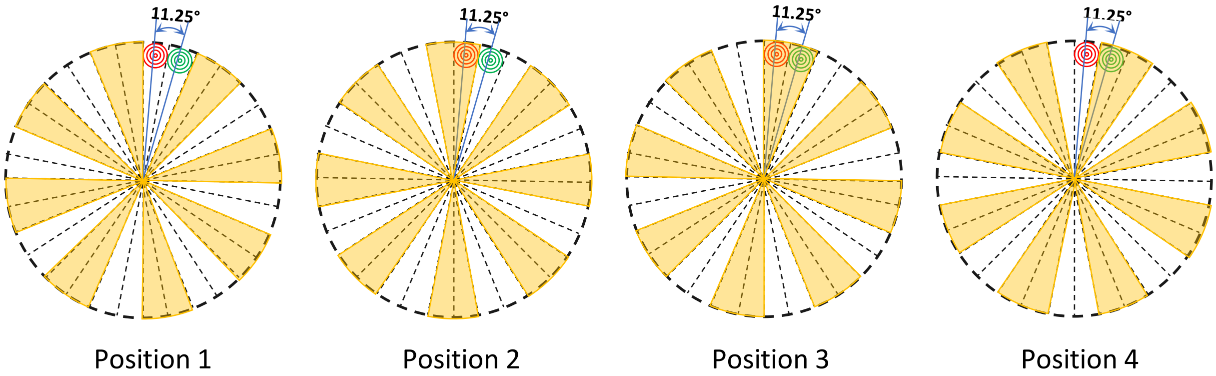

Figure 5.2: 32x Position Inductive Encoder

5.10.4 Equivalent Coil Position Geometry

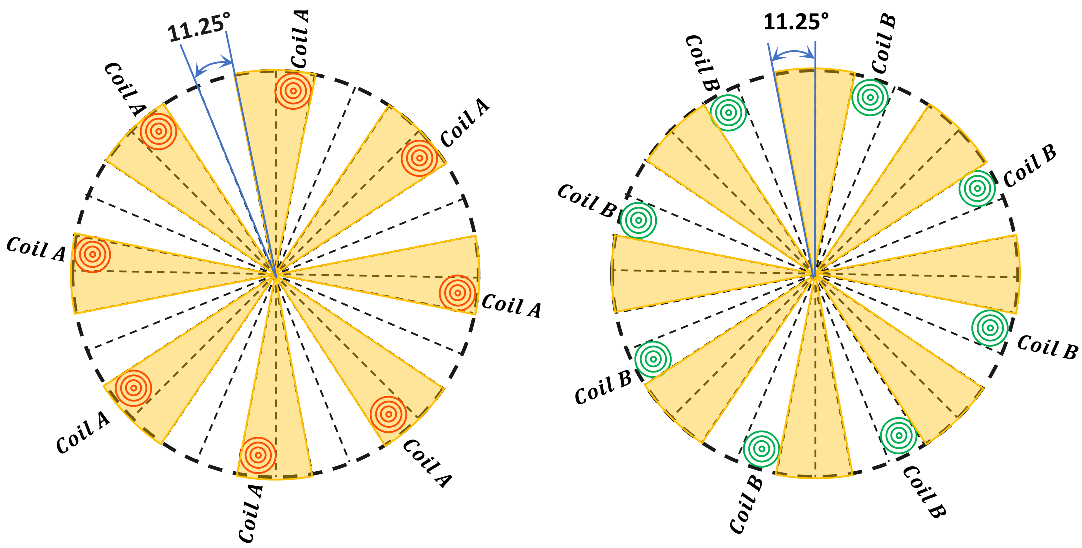

Figure 5.3: Coil A and Coil B equivalent positions

The geometrical positions of coil A and coil B have equivalent positions at every $4n \cdot \theta_{coil}$ interval. Placing the coil at any one of the equivalent positions will result in the correct encoding sequence.

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5.10.5 Reference Coils

Coil $\overline{A}$ and Coil $\overline{B}$ can be used as a reference to Coil A and Coil B respectively. The use of reference coils can improve the noise immunity and temperature stability for specific applications. Table 5.3 shows the encoded states for the 32-position encoder with reference coils. The position of the reference coils is such that the state of the reference coils is always the opposite of the non-reference coils.

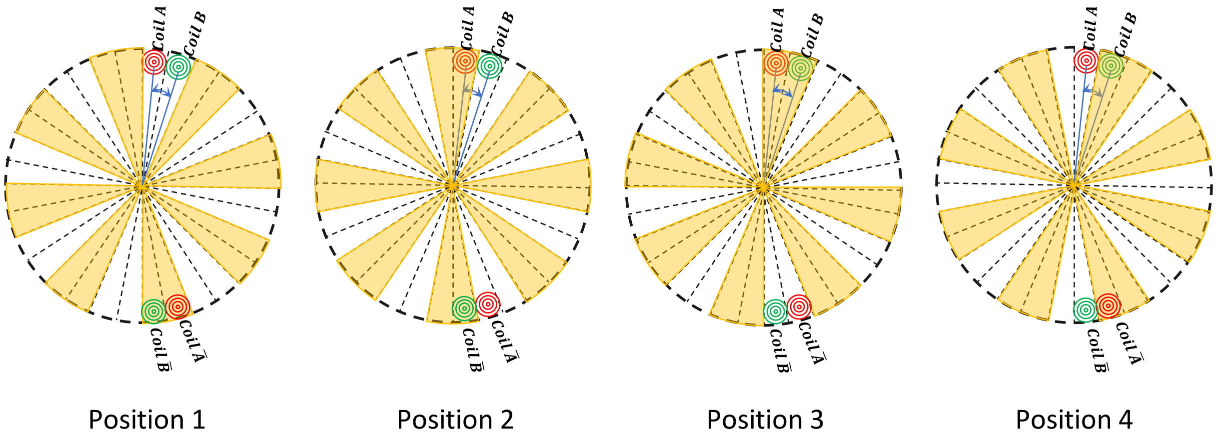

Figure 5.4: Encoder Reference Coils

Table 5.3: Gray encoder with reference channel

Positions	Angle	Gray Encoded State			
		Coil A	Coil $\overline{A}$	Coil B	Coil $\overline{B}$
1	0°	0	1	0	1
2	90°	1	0	0	1
3	180°	1	0	1	0
4	270°	0	1	1	0

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6 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed. Some are described below. The other hardware parameters are not discussed as they should only be adjusted under the guidance of Azoteq support engineers.

6.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the product GUI, and the relative parameters (Charge Transfer Frequency) will be provided. For high resistance sensors, it might be necessary to decrease f_{xfer}. Increasing f_{xfer} for the different sensing modes will increase the channel counts and decreasing f_{xfer} will decrease the channel counts. For inductive setups with f_{xfer} greater than 2MHz, make sure that the ATI compensation registers are cleared by writing a zero to the ATI compensation registers 0x5003, 0x5103, 0x5203, 0x5303, 0x5403, and 0x5503. For more information about the usage of f_{xfer} for an inductive resonant tank design, see Appendix B.

6.2 Reset

6.2.1 Reset Indication

After a reset, the *Device Reset* bit will be set by the system to indicate that the reset event occurred. This bit is cleared when the master sets the *Ack Reset*. If it becomes set again, the master will know that a reset has occurred, and can react appropriately.

While the *Device Reset* bit remains set:

- The device will not be able to enter into I^2C event mode operation (i.e. streaming communication behaviour will be maintained until the Reset bit is cleared)
- During the period of ATI execution, the device will provide communication windows continuously resulting in much longer time to finish the ATI routine

6.2.2 Software Reset

The IQS7225A can be reset by means of an I^2C command (*Reset*).

6.2.3 Hardware Reset

The MCLR pin (active low) can be used to hard reset the device. MCLR functionality is disabled when the I^2C window is opened (RDY/MCLR pin is low) and it is re-enabled when the I^2C window is closed (RDY/MCLR pin is high). For more details see Figure 6.1 and Section 4.2.

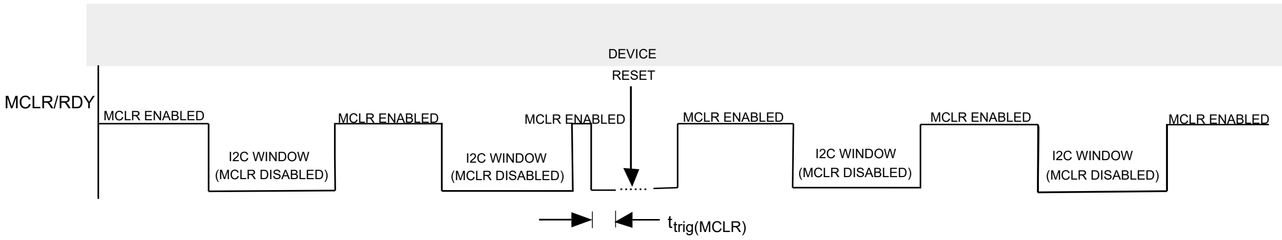

Figure 6.1: DEVICE RESET AND MCLR FUNCTIONALITY[i]

[i]The MCLR/RDY pin is pulled low by the IC for I^2C communication. The MCU pulls the MCLR/RDY pin low to reset the device.

7 Additional Features

7.1 Setup Defaults

The supplied GUI can be utilised to configure the optimal settings. The design specific settings are exported and can be written to the device by the master after every power-on reset.

7.2 RF Immunity

The IQS7225A has immunity to high power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DD}.

Place a 100pF in parallel with the 2.2 µF ceramic on V_{REG}. Also, place a 100pF in parallel with the 4.7 µF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sensing pads. Normally these are in the range of 470 Ω – 1 kΩ. PCB ground planes also improve noise immunity. For more info, see AZD115.

7.3 Blocking Channel

The IQS7225A can be configured to use blocking channels. The concept of a blocking channel can be described as follows: Suppose there are two channels, channel 0 and channel 1. Channel 1 can be configured as the blocking channel for channel 0. In this configuration, channel 0 will be able to detect an event, or be used in a post-processing step such as forming part of an encoder calculation, only if channel 1 detects a touch or deep touch event.

7.4 Number of Events

The IQS7225A channel number of events feature is used to control the primary sensor outputs that are displayed for each channel. The configuration is as shown below.

- 0: No event
- 1: Proximity event only
- 2: Proximity and touch events only
- 3: Proximity, touch, and deep touch events.

Note - For the encoder channels, the number of events is set to one and the coil enter threshold is used to activate a touch event when the wheel metal segment is over the coil.

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8 I²C Interface

8.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of a RDY (ready interrupt) line. The communications interface of the IQS7225A supports the following:

- *Fast-mode-plus* standard I²C up to 1MHz.
- Streaming data as well as event mode.
- The provided interrupt line (RDY) is an open-drain active-low implementation and indicates a communication window.

The IQS7225A implements 16-bit addressing with 2 data bytes at each address. Two consecutive 8-bit read or write operations are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" (least significant byte) and "byte 1" (most significant byte).

8.2 I²C Address

When GPIO5/ADDR is pulled up to VDD the 7-bit I²C device address is 0x44 ('1000100') and the full address byte will thus be 0x89 (read) or 0x88 (write). When GPIO5/ADDR is pulled low to GND the 7-bit I²C device address is 0x45 ('1000101') and the full address byte will thus be 0x8B (read) or 0x8A (write).

Other address options exist on special request. Please contact Azoteq.

8.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

8.4 Memory Map Addressing

8.4.1 16-bit Address

Device settings are addressed with 16-bit memory addresses. When reading device settings, it is possible to address each memory block as an 8-bit address and then continue to clock into the next address locations. For example, the procedure depicted below is followed to read the values from the hypothetical address 0xE000 to 0xE003:

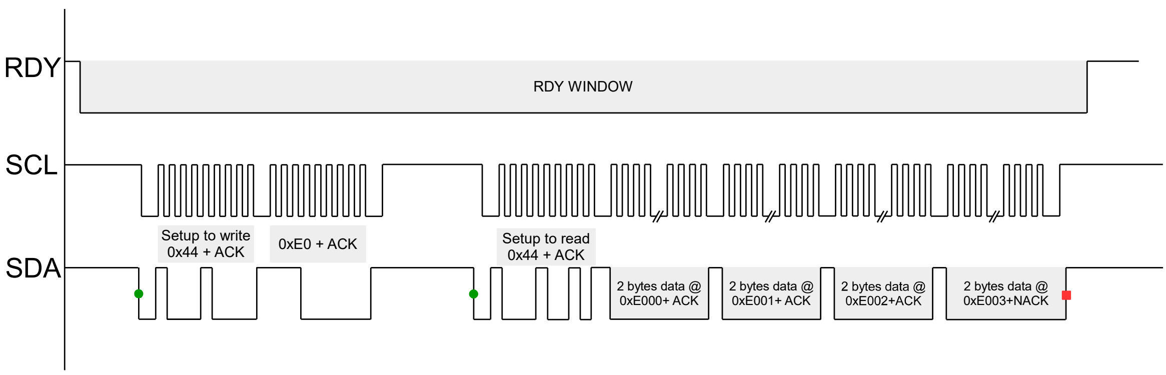

Figure 8.1: 8-bit Addressing for Continuous Block

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However, if you need to address a specific memory address or write to a memory address, then you will need to address using the full 16-bit address (note the 16-bit address is high byte first, unlike the data which is low byte first):

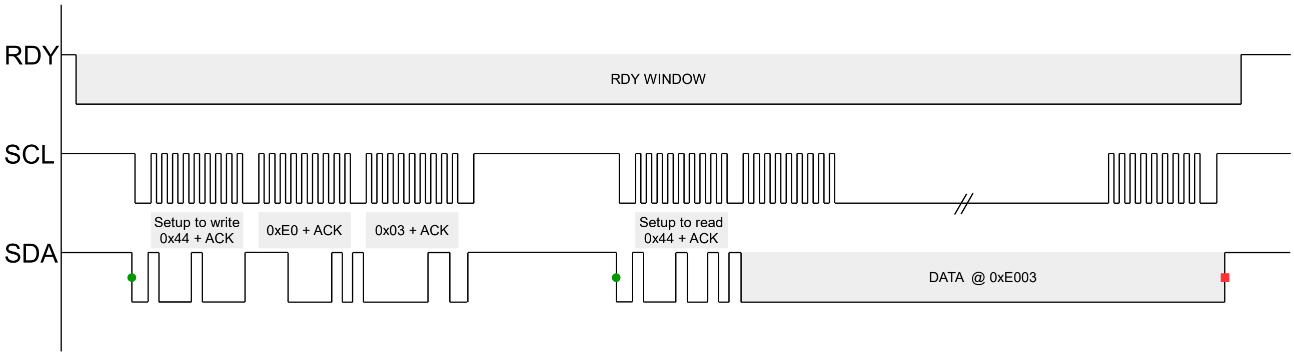

Figure 8.2: Extended 16-bit Addressing for a Specific Register

8.5 Data

The memory map implements a 16-bit addressing scheme with 16-bit words, meaning that each address contains 2 bytes of data. For example, address 0x2300 will provide two bytes, then the next two bytes read/written will be for address 0x2301.

The 16-bit data is sent in little endian byte order (least significant byte first).

The H-File generated by the GUI will display the start address of each block of data, with each address containing 2 bytes. The data of all the addresses can be written consecutively in a single block of data or the entire memory map, (refer to Figure 8.1), or data can be written explicitly to a specific address (refer to Figure 8.2). An example of the h-file exported by the GUI and the order of the data, is shown in Figure 8.3.

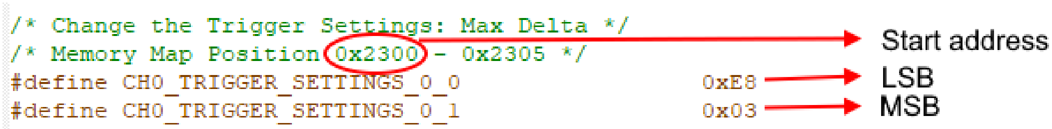

Figure 8.3: Example of an H-File Exported by the GUI

8.6 I²C Timeout

If the communication window is not serviced within the I²C timeout period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the corresponding data was missed/lost, and this should be avoided. The default I²C timeout period is set to 500ms and can be adjusted in register 0x2002.

8.7 Terminate Communication

A standard I²C STOP ends the current communication window.

If the stop bit disable (bit 0 register 0x2003) is set, the device will not terminate the window on a

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I²C STOP. The communication window must be terminated using the end communications command (0xFF).

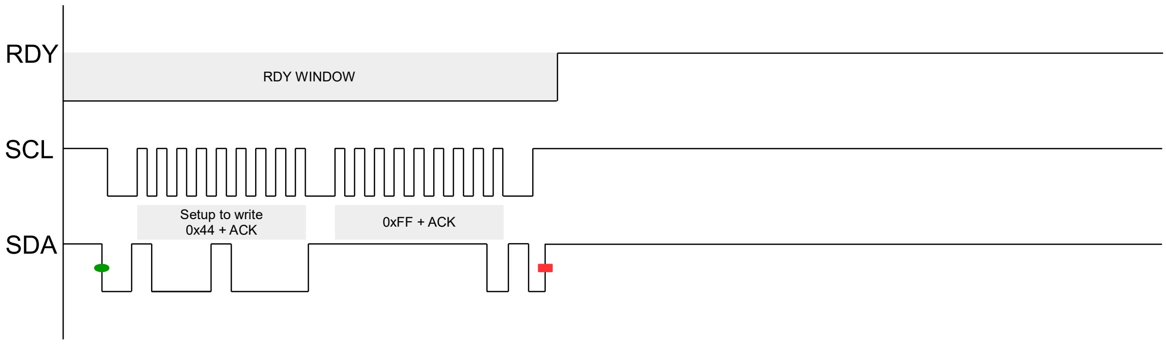

Figure 8.4: Force Stop Communication Sequence

8.7.1 Force Communication

In streaming mode, the IQS7225A I²C will provide RDY windows at intervals specified in the power mode report rate. Ideally, communication with the IQS7225A should only be initiated in a Ready window, but a communication request described in Figure 8.5 below will force a Ready window to open. In event mode Ready windows are only provided when an event is reported and a Ready window must be requested to write or read settings outside of this window. The minimum and maximum time between the communication request and the opening of a Ready window (t_{wait}), is application specific, but the average values are $0.1\text{ms} \leq t_{wait} \leq 45\text{ms}$ [i].

The communication request sequence is shown in figure 8.5 below.

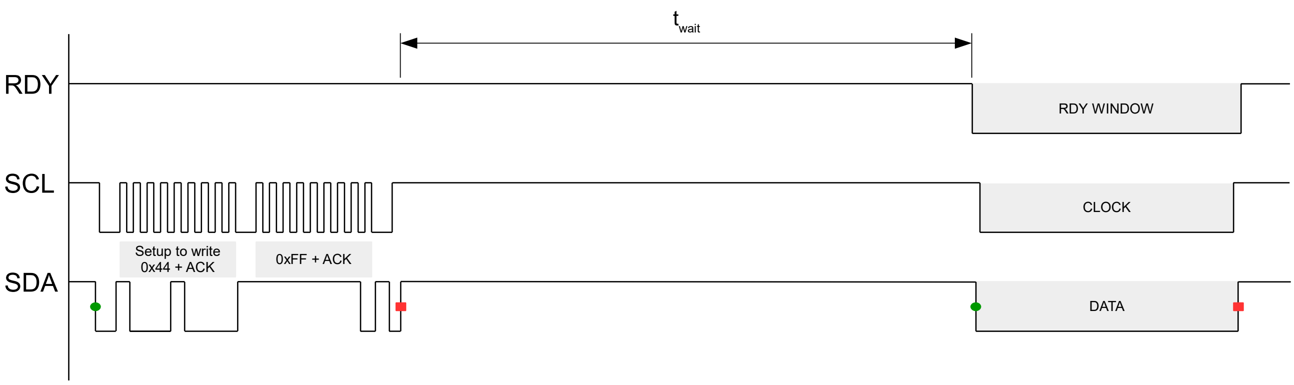

Figure 8.5: Force Communication Sequence

8.8 RDY/IRQ

The IC has an open-drain active-low RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and obtain the data accordingly. It is also useful to allow the master MCU to enter low-power/sleep and allowing wake-up from low-power/sleep when user presence is detected. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

[i] Please contact Azoteq for an application specific value of t_{wait}

8.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e. while RDY = high)

8.10 I^{2}C Mode

The IQS7225A has three *I^{2}C interface options*, as described in the sections below.

8.10.1 I^{2}C Streaming

I^{2}C Streaming mode refers to constant data reporting at the relevant power mode report rate specified in register *0x2103* (normal power), register *0x2105* (low power) and register *0x2107* (ultra low power) respectively.

8.10.2 I^{2}C Event Mode

The device can be set up to bypass the communication window when no activity is sensed (EVENT MODE). This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred. The communication will resume (RDY will indicate available data) if an enabled event occurs.

8.10.3 I^{2}C Stream in Touch Mode

Stream in touch is a hybrid I^{2}C mode between streaming mode and event mode. The device follows event mode I^{2}C protocol, but when a touch is registered on any channel, the device enters streaming mode until the touch is released.

The hybrid I^{2}C interface is specifically aimed at the use of sliders where data needs to be received and processed for the duration of a touch.

8.11 Event Mode Communication

Event mode can only be entered if the following requirements are met:

- *Reset* bit must be cleared by acknowledging the device reset condition occurrence through writing *Ack Reset* bit to clear the system status flag.
- Events must be serviced by reading from the *Events* register 0x1001 to ensure all events flags are cleared, otherwise continuous reporting (RDY interrupts) will persist after every conversion cycle similar to streaming mode.

8.11.1 Events

Numerous events can be individually enabled to trigger communication, bit definitions can be found in Table A.4, A.5 and Table A.6:

- Power mode change events
- ATI events
- Proximity events

- Touch events
- Deep touch events

9 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions

Address Read Only	Data (16bit)	Notes
0x0000	Application Version Info	See Table A.1
0x0001		
0x0002		
0x0003		
0x0004		
0x0100	ROM Version Info	See Table A.2
0x0101		
0x0102		
0x0103		
0x0104		
Read Only	**Device Status**	
0x1000	System Status	See Table A.3
0x1001	Events	See Table A.4
0x1002	Proximity and Touch Event Status	See Table A.5
0x1003	Deep Touch Event Status	See Table A.6
0x1004	Encoder Gray States	See Table A.7
0x1005	Encoder Angle	Value $\in [0, 360)$
0x1006	Encoder Counter	Value $\in [-32\,767, 32\,767]$
0x1007	Channel 0 Trigger Level	Value $\in [0, 2047]$
0x1008	Channel 1 Trigger Level	Value $\in [0, 2047]$
0x1009	Channel 2 Trigger Level	Value $\in [0, 2047]$
0x100A	Channel 3 Trigger Level	Value $\in [0, 2047]$
0x100B	Channel 4 Trigger Level	Value $\in [0, 2047]$
0x100C	Channel 5 Trigger Level	Value $\in [0, 2047]$
Read Only	**Channel Counts**	
0x1100	Channel 0 Counts	Value $\in [0, 2047]$
0x1101	Channel 1 Counts	
0x1102	Channel 2 Counts	
0x1103	Channel 3 Counts	
0x1104	Channel 4 Counts	
0x1105	Channel 5 Counts	
Read Only	**Channel LTA**	
0x1200	Channel 0 LTA	Value $\in [0, 2047]$
0x1201	Channel 1 LTA	
0x1202	Channel 2 LTA	
0x1203	Channel 3 LTA	
0x1204	Channel 4 LTA	
0x1205	Channel 5 LTA	
Read Only	**Channel Delta**	
0x1300	Channel 0 Delta	Value $\in [-2047, 2047]$
0x1301	Channel 1 Delta	
0x1302	Channel 2 Delta	
0x1303	Channel 3 Delta	
0x1304	Channel 4 Delta	
0x1305	Channel 5 Delta	

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	Start of Read-Write registers	
Read-Write	**Channel LTA Overwrite**	
0x1400	Channel 0 LTA Overwrite	Value $\in [0, 2047]$
0x1401	Channel 1 LTA Overwrite	
0x1402	Channel 2 LTA Overwrite	
0x1403	Channel 3 LTA Overwrite	
0x1404	Channel 4 LTA Overwrite	
0x1405	Channel 5 LTA Overwrite	
Read-Write	**PMU and System Settings**	
0x2000	System Control Settings	See Table A.8
0x2001	Event Mask	See Table A.9
0x2002	I^2C Window Timeout	16-bit value (ms)
0x2003	I^2C Configuration	See Table A.10
Read-Write	**Report Rates and Timeouts**	
0x2100	ATI Error Timeout	16-bit value * 0.5s
0x2101	ATI Report Rate	16-bit value (ms)
0x2102	Normal Power Mode Timeout	16-bit value (ms)
0x2103	Normal Power Mode Report Rate	16-bit value (ms)
0x2104	Low Power Mode Timeout	16-bit value (ms)
0x2105	Low Power Mode Report Rate	16-bit value (ms)
0x2106	Ultra Low Power Mode Timeout	16-bit value (ms)
0x2107	Ultra Low Power Mode Report Rate	16-bit value (ms)
Read-Write	**Counts & LTA Reseed**	
0x2200	Channel 0 Counts & LTA Reseed	See Table A.11
0x2201	Channel 1 Counts & LTA Reseed	
0x2202	Channel 2 Counts & LTA Reseed	
0x2203	Channel 3 Counts & LTA Reseed	
0x2204	Channel 4 Counts & LTA Reseed	
0x2205	Channel 5 Counts & LTA Reseed	
Read-Write	**Channel Max Delta**	
0x2300	Channel 0 Max Delta	Value $\in [0, 2047]$
0x2301	Channel 1 Max Delta	
0x2302	Channel 2 Max Delta	
0x2303	Channel 3 Max Delta	
0x2304	Channel 4 Max Delta	
0x2305	Channel 5 Max Delta	
Read-Write	**Channel Number of Threshold**	
0x2400	Channel 0 Number of Trigger Levels	Value $\in [0, 255]$
0x2401	Channel 1 Number of Trigger Levels	
0x2402	Channel 2 Number of Trigger Levels	
0x2403	Channel 3 Number of Trigger Levels	
0x2404	Channel 4 Number of Trigger Levels	
0x2405	Channel 5 Number of Trigger Levels	
Read-Write	**Cycle Setup**	
0x3000	Cycle Setup 0	See Table A.12
0x3001		See Table A.13
0x3002		See Table A.14
0x3100	Cycle Setup 1	See Table A.12
0x3101		See Table A.13
0x3102		See Table A.14
0x3200	Cycle Setup 2	See Table A.12

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0x3201		See Table A.13
0x3202		See Table A.14
0x3300	Cycle Setup 3	See Table A.12
0x3301		See Table A.13
0x3302		See Table A.14
0x3400	Cycle Setup 4	See Table A.12
0x3401		See Table A.13
0x3402		See Table A.14
0x3500	Cycle Setup 5	See Table A.12
0x3501		See Table A.13
0x3502		See Table A.14
Read-Write	**Engine Channel Select**	
0x3600	Cycle 0 Engine-Channel Select	See Table A.15
0x3601	Cycle 1 Engine-Channel Select	
0x3602	Cycle 2 Engine-Channel Select	
0x3603	Cycle 3 Engine-Channel Select	
0x3604	Cycle 4 Engine-Channel Select	
0x3605	Cycle 5 Engine-Channel Select	
	Button Setup	
Read-Write	**Channel 0**	
0x4000	Proximity Event Setup	See Table A.16
0x4001	Touch Event Setup	See Table A.17
0x4002	Deep Touch Event Setup	See Table A.18
0x4003	Channel Output Timeouts	See Table A.19
0x4004	General Button Settings	See Table A.20
0x4005	Beta Filters	See Table A.21
0x4006	Fast Beta Filters	See Table A.22
0x4007	Engine Setup Delay	See Table A.23
Read-Write	**Channel 1**	
0x4100	Proximity Event Setup	See Table A.16
0x4101	Touch Event Setup	See Table A.17
0x4102	Deep Touch Event Setup	See Table A.18
0x4103	Channel Output Timeouts	See Table A.19
0x4104	General Button Settings	See Table A.20
0x4105	Beta Filters	See Table A.21
0x4106	Fast Beta Filters	See Table A.22
Read-Write	**Channel 2**	
0x4200	Proximity Event Setup	See Table A.16
0x4201	Touch Event Setup	See Table A.17
0x4202	Deep Touch Event Setup	See Table A.18
0x4203	Channel Output Timeouts	See Table A.19
0x4204	General Button Settings	See Table A.20
0x4205	Beta Filters	See Table A.21
0x4206	Fast Beta Filters	See Table A.22
Read-Write	**Channel 3**	
0x4300	Proximity Event Setup	See Table A.16
0x4301	Touch Event Setup	See Table A.17
0x4302	Deep Touch Event Setup	See Table A.18
0x4303	Channel Output Timeouts	See Table A.19
0x4304	General Button Settings	See Table A.20
0x4305	Beta Filters	See Table A.21

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0x4306	Fast Beta Filters	See Table A.22
Read-Write	**Channel 4**	
0x4400	Proximity Event Setup	See Table A.16
0x4401	Touch Event Setup	See Table A.17
0x4402	Deep Touch Event Setup	See Table A.18
0x4403	Channel Output Timeouts	See Table A.19
0x4404	General Button Settings	See Table A.20
0x4405	Beta Filters	See Table A.21
0x4406	Fast Beta Filters	See Table A.22
Read-Write	**Channel 5**	
0x4500	Proximity Event Setup	See Table A.16
0x4501	Touch Event Setup	See Table A.17
0x4502	Deep Touch Event Setup	See Table A.18
0x4503	Channel Output Timeouts	See Table A.19
0x4504	General Button Settings	See Table A.20
0x4505	Beta Filters	See Table A.21
0x4506	Fast Beta Filters	See Table A.22
	Sensor Setup	
Read-Write	**Channel 0**	
0x5000	Rx Select and General Channel Settings	See Table A.24
0x5001	ATI Base and Target	See Table A.25
0x5002	ATI Fine and Coarse Mirrors	See Table A.26
0x5003	ATI Compensation	See Table A.27
Read-Write	**Channel 1**	
0x5100	Rx Select and General Channel Settings	See Table A.24
0x5101	ATI Base and Target	See Table A.25
0x5102	ATI Fine and Coarse Mirrors	See Table A.26
0x5103	ATI Compensation	See Table A.27
Read-Write	**Channel 2**	
0x5200	Rx Select and General Channel Settings	See Table A.24
0x5201	ATI Base and Target	See Table A.25
0x5202	ATI Fine and Coarse Mirrors	See Table A.26
0x5203	ATI Compensation	See Table A.27
Read-Write	**Channel 3**	
0x5300	Rx Select and General Channel Settings	See Table A.24
0x5301	ATI Base and Target	See Table A.25
0x5302	ATI Fine and Coarse Mirrors	See Table A.26
0x5303	ATI Compensation	See Table A.27
Read-Write	**Channel 4**	
0x5400	Rx Select and General Channel Settings	See Table A.24
0x5401	ATI Base and Target	See Table A.25
0x5402	ATI Fine and Coarse Mirrors	See Table A.26
0x5403	ATI Compensation	See Table A.27
Read-Write	**Channel 5**	
0x5500	Rx Select and General Channel Settings	See Table A.24
0x5501	ATI Base and Target	See Table A.25
0x5502	ATI Fine and Coarse Mirrors	See Table A.26
0x5503	ATI Compensation	See Table A.27

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Read-Write	Encoder Setup	
0x6000	Number of Metal Targets	See Table A.28
0x6100	Coil A Channel/Fixed Reference	See Table A.29
0x6101	Coil A Enter Threshold	See Table A.30
0x6102	Coil A Exit Threshold	See Table A.31
0x6200	Coil B Channel/Fixed Reference	See Table A.29
0x6201	Coil B Enter Threshold	See Table A.30
0x6202	Coil B Exit Threshold	See Table A.31

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10 Implementation and Layout

10.1 Layout Fundamentals

NOTE

Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 4.7 µF plus a 100 pF low-ESR ceramic decoupling capacitor between the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimetres).

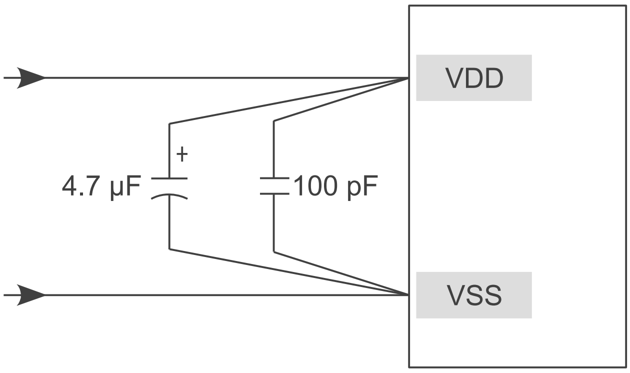

Figure 10.1: Recommended Power Supply Decoupling

10.1.2 VREG

The VREG pin requires a 2.2 µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the microcontroller. The figure below shows an example layout where the capacitor is placed close to the IC.

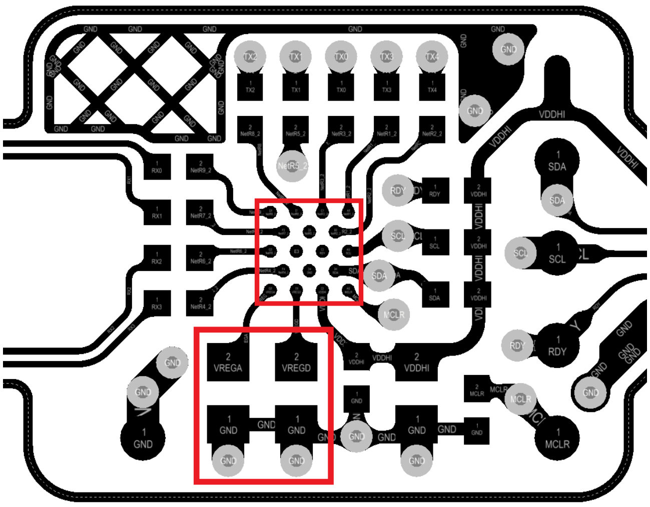

Figure 10.2: VREG Capacitor Placement Close to IC

11 Ordering Information

11.1 Ordering Code

IQS7225A zzz ppb

IC NAME	IQS722xy	=	IQS7225A	
POWER-ON CONFIGURATION	zzz	=	001[i]	6 button self-capacitance on startup. Configurable via I^{2}C. F_{OSC} = 18MHz (fixed/always)
			101	6 button self capacitance on startup. Configurable via I^{2}C. F_{OSC} = 14MHz / 18MHz (Configurable)
PACKAGE TYPE	pp	=	QN QF	QFN-20 package - Default option QFR-20 package - Custom option
BULK PACKAGING	b	=	R	QFN-20/QFR-20 Reel 2000pcs/reel

Figure 11.1: Order Code Description

11.2 Top Marking

11.2.1 QFN20 Package Marking Option 1

IQS
7225A
pppxx

Product Name
ppp = product code
xx = batchcode

11.2.2 QFN20 Package Marking Option 2

IQS
722xy
pppxx

Product Name
ppp = product code
xx = batchcode

[i] Please refer to product information notice PIN-230172 for more details.

12 Package Specification

12.1 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.

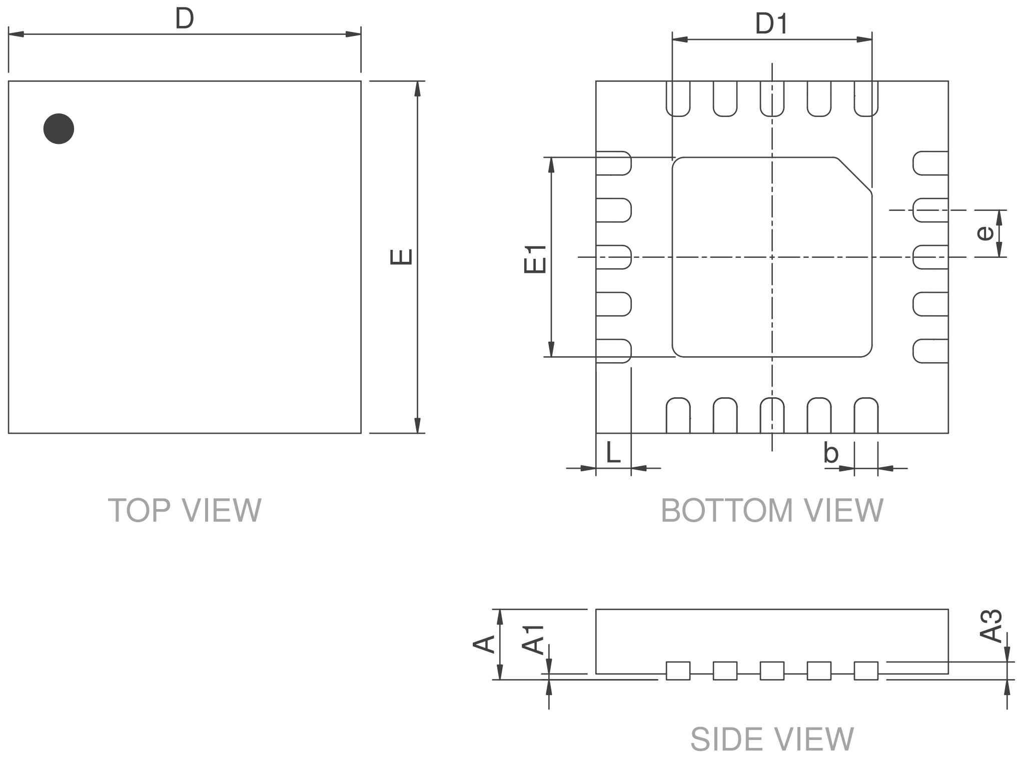

Figure 12.1: QFN (3x3)-20 (QFR) Package Outline Visual Description

Table 12.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

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12.2 Package Outline Description – QFN20 (QNR)

This package outline is specific to order codes ending in *QNR*.

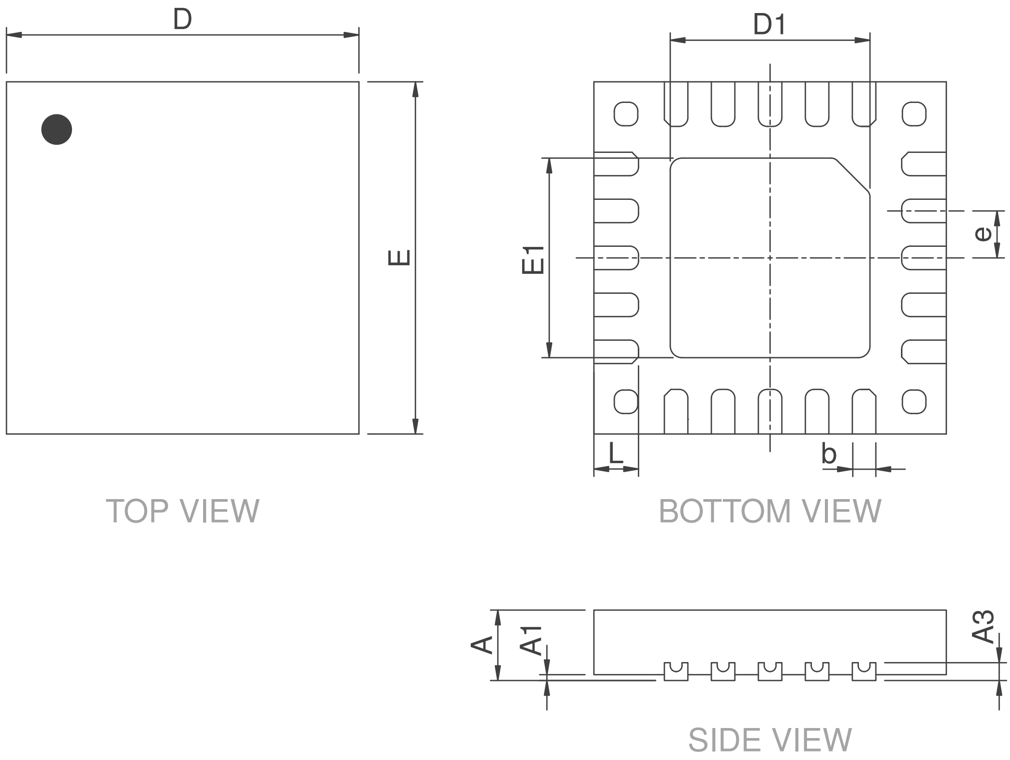

Figure 12.2: QFN (3x3)-20 (QNR) Package Outline Visual Description

Table 12.2: QNR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0		0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
e		0.40 BSC	
L	0.33	0.38	0.43

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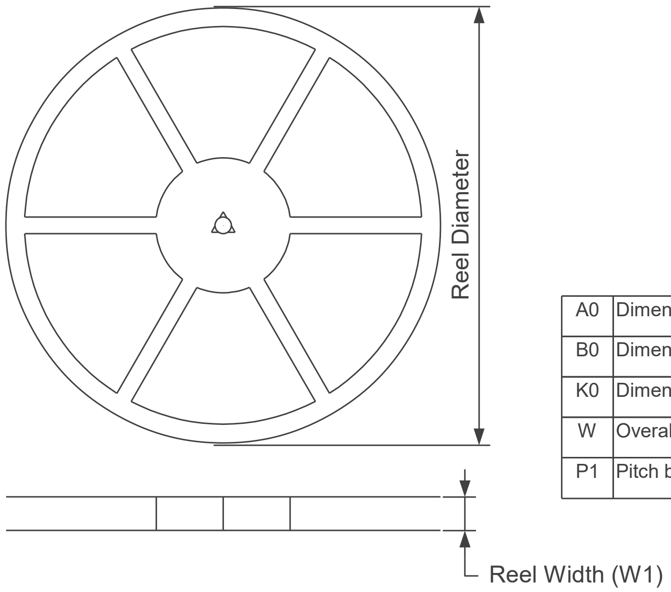
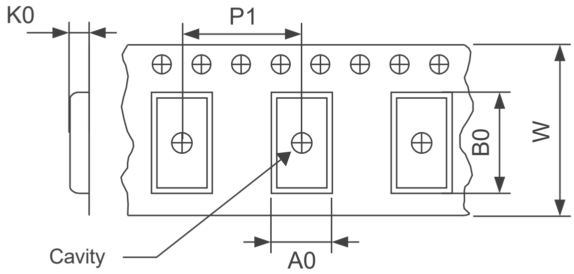
12.3 Tape and Reel Specifications

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

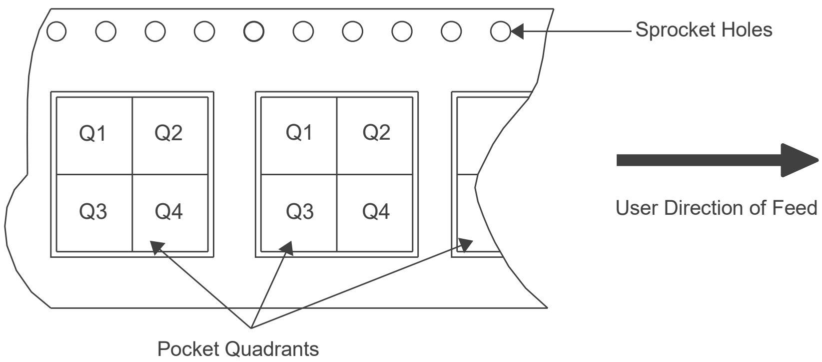


Figure 12.3: Tape and Reel Specification

Table 12.3: Tape and Reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2

12.4 Moisture Sensitivity Levels

Package	MSL
QFN20	1

12.5 Reflow Specifications

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A Memory Map Descriptions

Table A.1: Version Information

Register: 0x0000 - 0x0004

Address	Category	Name	Value	
0x0000	Application Version Info	Product Number	791	16-bit value
0x0001		Major Version	2	
0x0002		Minor Version	1[i]	
			2[ii]	
0x0003		Patch Number (commit hash)	Reserved	
0x0004				

Table A.2: ROM Version Information

Register: 0x0100 - 0x0104

Address	Category	Name	Value
0x0100	ROM Library Version Info	Library Number	Reserved
0x0101		Major Version	Reserved
0x0102		Minor Version	Reserved
0x0103		Patch Number (commit hash)	Reserved
0x0104			

Table A.3: System Status

Register: 0x1000

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Global Halt	Reserved	Power Mode		Reset	Proximity De-bounce	ATI Error	ATI Active

- Bit 7: **Global Halt**
  - 0: Global halt not active
  - 1: Global halt active
- Bit 5-4: **Power Mode**
  - 00: Normal power mode
  - 01: Low power mode
  - 10: Ultra-low power mode
- Bit 3: **Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 2: **Proximity Debounce**
  - 0: Proximity debounce inactive
  - 1: Proximity debounce active
- Bit 1: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 0: **ATI Active**
  - 0: ATI not active
  - 1: ATI active

Table A.4: Events

Register: 0x1001

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH5 Trigger	CH4 Trigger	CH3 Trigger	CH2 Trigger	CH1 Trigger	CH0 Trigger	Power Event	ATI Event	Reserved					Deep Touch Event	Touch Event	Proximity Event

- Bit 15: **CH5 Trigger Event**
  - 0: No CH5 Trigger event occurred
  - 1: CH5 Trigger event occurred

[i] Order code 001. Please refer to product information notice PIN-230172 for more details.
[ii] Order code 101.

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- Bit 14: **CH4 Trigger Event**
  - 0: No CH4 Trigger event occurred
  - 1: CH4 Trigger event occurred
- Bit 13: **CH3 Trigger Event**
  - 0: No CH3 Trigger event occurred
  - 1: CH3 Trigger event occurred
- Bit 12: **CH2 Trigger Event**
  - 0: No CH2 Trigger event occurred
  - 1: CH2 Trigger event occurred
- Bit 11: **CH1 Trigger Event**
  - 0: No CH1 Trigger event occurred
  - 1: CH1 Trigger event occurred
- Bit 10: **CH0 Trigger Event**
  - 0: No CH0 Trigger event occurred
  - 1: CH0 Trigger event occurred
- Bit 9: **Power Event**
  - 0: No power event occurred
  - 1: Power event occurred
- Bit 8: **ATI Event**
  - 0: No ATI event occurred
  - 1: ATI event occurred
- Bit 2: **Deep Touch Event**
  - 0: No deep touch event occurred
  - 1: Deep touch event occurred
- Bit 1: **Touch Event**
  - 0: No touch event occurred
  - 1: Touch event occurred
- Bit 0: **Proximity Event**
  - 0: No proximity event occurred
  - 1: Proximity event occurred

Table A.5: Proximity and Touch Event Status

Register: 0x1002

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Touch CH5	Touch CH4	Touch CH3	Touch CH2	Touch CH1	Touch CH0	Reserved		Proximity CH5	Proximity CH4	Proximity CH3	Proximity CH2	Proximity CH1	Proximity CH0

- Bit 5-0: **Proximity Channel Event Status**
  - 0: No proximity event occurred on channel
  - 1: Proximity event occurred on channel
- Bit 13-8: **Touch Channel Event Status**
  - 0: No touch event occurred on channel
  - 1: Touch event occurred on channel

Table A.6: Deep Touch Event Status

Register: 0x1003

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved										Deep Touch CH5	Deep Touch CH4	Deep Touch CH3	Deep Touch CH2	Deep Touch CH1	Deep Touch CH0

- Bit 5-0: **Deep Touch Channel Event Status**
  - 0: No deep touch event occurred on channel
  - 1: Deep touch event occurred on channel

Table A.7: Encoder Gray States

Register: 0x1004

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved														Coil B Active	Coil A Active

- Bit 1-0: **Gray Encoded State**

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- 00: No Coil active
- 01: Only Coil A active
- 11: Coil A and Coil B active
- 10: Only Coil B active

Table A.8: System Control Settings

Register: 0x2000

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I²C Interface		Power Mode			Auto Mode		ULP Mode	Reserved	Reserved	Software WDT	Hfosc Select	Reseed	Re-ATI	Reset	ACK Reset

- Bit 15-14: **I²C Interface**
  - 00: I²C streaming mode
  - 01: I²C event mode
  - 10: I²C streaming in touch mode
- Bit 13-11: **Power Mode**
  - 000: Normal Power Mode
  - 001: Low-Power Mode
  - 010: Ultra-Low Power Mode
  - 011: Halt Power Mode
  - 100: Automatic Switching Power Mode
- Bit 10-9: **Auto Mode**
  Number of autonomous conversions on cycle 0 before a ULP conversion is executed
  - 00: 4 autonomous conversions
  - 01: 8 autonomous conversions
  - 10: 16 autonomous conversions
  - 11: 32 autonomous conversions
- Bit 8: **ULP Mode**
  - 0: ULP mode disabled
  - 1: ULP mode enabled
- Bit 5: **Software WDT**
  - 0: Software WDT disabled
  - 1: Software WDT enabled
- Bit 4: **HFosc Select**
  - 0: 14MHz
  - 1: 18MHz
- Bit 3: **Reseed (set only, will clear when done)**
  - 1: Reseed LTA for all channels
- Bit 2: **Re-ATI (set only, will clear when done)**
  - 1: Re-ATI all channels
- Bit 1: **Reset (set only, will clear when done)**
  - 1: Perform a software reset
- Bit 0: **ACK Reset (set only, will clear when done)**
  - 1: Acknowledge device reset

Table A.9: Event Mask

Register: 0x2001

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH5 Trigger	CH4 Trigger	CH3 Trigger	CH2 Trigger	CH1 Trigger	CH0 Trigger	Power	ATI	Reserved					Deep Touch	Touch	Proximity

- Bit 15: **CH5 Trigger Event Mask**
  - 0: CH5 trigger event disabled
  - 1: CH5 trigger event enabled
- Bit 14: **CH4 Trigger Event Mask**
  - 0: CH4 trigger event disabled
  - 1: CH4 trigger event enabled
- Bit 13: **CH3 Trigger Event Mask**
  - 0: CH3 trigger event disabled
  - 1: CH3 trigger event enabled
- Bit 12: **CH2 Trigger Event Mask**
  - 0: CH2 trigger event disabled

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- 1: CH2 trigger event enabled

- Bit 11: **CH1 Trigger Event Mask**
  - 0: CH1 trigger event disabled
  - 1: CH1 trigger event enabled
- Bit 10: **CH0 Trigger Event Mask**
  - 0: CH0 trigger event disabled
  - 1: CH0 trigger event enabled
- Bit 9: **Power Mode Event Mask**
  - 0: Power mode event disabled
  - 1: Power mode event enabled
- Bit 8: **ATI Event Mask**
  - 0: ATI event disabled
  - 1: ATI event enabled
- Bit 2: **Deep Touch Event Mask**
  - 0: Deep touch event disabled
  - 1: Deep touch event enabled
- Bit 1: **Touch Event Mask**
  - 0: Touch event disabled
  - 1: Touch event enabled
- Bit 0: **Proximity Event Mask**
  - 0: Proximity event disabled
  - 1: Proximity event enabled

Table A.10: I²C Communication

Register: 0x2003

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved														RW Check Disable	Stop Bit Disable

- Bit 1: **RW Check Disable**
  - 0: Read-only registers (0x1000 – 0x1305) cannot be overwritten.
  - 1: Allows writing to read-only registers (0x1000 – 0x1305).
- Bit 0: **Stop Bit Disable**
  - 0: I²C communication window terminated by stop bit
  - 1: I²C communication window not terminated by stop bit, send 0xFF to slave address to terminate window

Table A.11: Channel Counts & LTA Reseed

Register: 0x2200 – 0x2205

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved														LTA Reseed	Counts Reseed

- Bit 1: **LTA Reseed (set only, will clear when done)**
  - 1: Reseed LTA filter for channel
- Bit 0: **Counts Reseed (set only, will clear when done)**
  - 1: Reseed Count filter for channel

Table A.12: Cycle Setup0

Register: 0x3000,0x3100,0x3200,0x3300,0x3400,0x3500

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Frequency Period								Conversion Frequency Fraction							

- Bit 15-8: **Conversion Frequency Period**
  - Range: 0 - 127
- Bit 7-0: **Conversion Frequency Fraction**
  - $256 * \frac{f_{xfer}}{f_{osc}}$
  - Range: 0 - 255
- Note: with deadtime either disabled/enabled, the following values for the conversion frequency periods (at fraction = 127) will result in the corresponding charge transfer frequencies (in MHz):

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Fraction	Period[i]	Dead-time disabled		Dead-time enabled	
		F_{OSC} = 18MHz	F_{OSC} = 14MHz	F_{OSC} = 18MHz	F_{OSC} = 14MHz
127	0	9.00	7.00	6.00	4.66
	1	4.50	3.50	3.60	2.80
	2	3.00	2.33	2.57	2.00
	3	2.25	1.75	2.00	1.55
	5	1.50	1.15	1.38	1.07
	8	1.00	0.77	0.95	0.74
	17	0.50	3.88	0.48	0.38

Table A.13: Cycle Setup1

Register: 0x3001, 0x3101, 0x3201, 0x3301, 0x3401, 0x3501

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PXS Mode								Reserved				GND Inactive Rx	Dead-time Enabled	F_{OSC} TX Freq	Vbias Enable

- Bit 15-8: **PXS Mode**
  - 00000000: None
  - 00000001: Self-capacitive
  - 00000010: Projected capacitance
  - 00000011: Inductive[ii]
- Bit 3: **GND Inactive Rx**
  - 0: Inactive Rx pins floating
  - 1: Inactive Rx pins grounded
- Bit 2: **Deadtime Enabled**
  - 0: Deadtime disabled
  - 1: Deadtime enabled
- Bit 1: **F_{OSC} Tx Freq**
  - 0: TX frequency configured by *Cycle Setup0* (F_{xfer} *Period* & *Fraction*)
  - 1: TX frequency set to F_{OSC} Enabled
- Bit 0: **Vbias Enabled**
  - 0: Vbias on Tx8 disabled
  - 1: Vbias on Tx8 enabled

Table A.14: Cycle Setup2

Register: 0x3002, 0x3102, 0x3202, 0x3302, 0x3402, 0x3502

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				Tx11	Tx10	Tx9	Tx8	Tx7	Tx6	Tx5	Tx4	Tx3	Tx2	Tx1	Tx0

- Bit 11: **Tx11**
  - 0: Tx11 disabled
  - 1: Tx11 enabled
- Bit 10: **Tx10**
  - 0: Tx10 disabled
  - 1: Tx10 enabled
- Bit 9: **Tx9**
  - 0: Tx9 disabled
  - 1: Tx9 enabled
- Bit 8: **Tx8**
  - 0: Tx8 disabled

[i]Charge transfer frequency not applicable for the 001 order code when conversion frequency period is equal to zero.
[ii]For inductive mode, set target value equal to base value.

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- 1: Tx8 enabled

- Bit 7: **Tx7**
  - 0: Tx7 disabled
  - 1: Tx7 enabled
- Bit 6: **Tx6**
  - 0: Tx6 disabled
  - 1: Tx6 enabled
- Bit 5: **Tx5**
  - 0: Tx5 disabled
  - 1: Tx5 enabled
- Bit 4: **Tx4**
  - 0: Tx4 disabled
  - 1: Tx4 enabled
- Bit 3: **Tx3**
  - 0: Tx3 disabled
  - 1: Tx3 enabled
- Bit 2: **Tx2**
  - 0: Tx2 disabled
  - 1: Tx2 enabled
- Bit 1: **Tx1**
  - 0: Tx1 disabled
  - 1: Tx1 enabled
- Bit 0: **Tx0**
  - 0: Tx0 disabled
  - 1: Tx0 enabled

Table A.15: Engine Channel Select

Register: 0x3600, 0x3601, 0x3602, 0x3603, 0x3604, 0x3605

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Engine B Channel Select								Engine A Channel Select							

- Bit 15-8: **Engine B Channel Select**
  - D’0’: Channel 0
  - D’1’: Channel 1
  - D’2’: Channel 2
  - D’3’: Channel 3
  - D’4’: Channel 4
  - D’5’: Channel 5
  - D’255’: None
- Bit 7-0: **Engine A Channel Select**
  - D’0’: Channel 0
  - D’1’: Channel 1
  - D’2’: Channel 2
  - D’3’: Channel 3
  - D’4’: Channel 4
  - D’5’: Channel 5
  - D’255’: None

Table A.16: Proximity Event Setup

Register: 0x4000, 0x4100, 0x4200, 0x4300, 0x4400, 0x4500

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Proximity Debounce Exit Threshold				Proximity Debounce Enter Threshold				Proximity Threshold							

- Bit 15-12: **Proximity Debounce Exit Threshold**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 11-8: **Proximity Debounce Enter Threshold**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 7-0: **Proximity Threshold**
  - 8-bit value
  - value $\times \frac{LTA}{256}$

Table A.17: Touch Event Setup

Register: 0x4001, 0x4101, 0x4201, 0x4301, 0x4401, 0x4501

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Hysteresis								Touch Threshold							

- Bit 15-8: **Touch Hysteresis**
  - Touch hysteresis value determines the release threshold. Release threshold can be determined as follows:
    $\frac{LTA}{256} \times (\text{Threshold value} - \text{Hysteresis value})$
  - 8 bit value
- Bit 7-0: **Touch Threshold**
  - 8 bit value
    value $\times \frac{LTA}{256}$

Table A.18: Deep Touch Event Setup

Register: 0x4002, 0x4102, 0x4202, 0x4302, 0x4402, 0x4502

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Deep Touch Hysteresis								Deep Touch Threshold							

- Bit 15-8: **Deep Touch Hysteresis**
  - Deep Touch hysteresis value determines the release threshold. Release threshold can be determined as follows:
    $\frac{LTA}{256} \times (\text{Threshold value} - \text{Hysteresis value})$
  - 8 bit value
- Bit 7-0: **Deep Touch Threshold**
  - 8 bit value
    value $\times \frac{LTA}{256}$

Table A.19: Channel Output Timeouts

Register: 0x4003, 0x4103, 0x4203, 0x4303, 0x4403, 0x4503

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch and 2 Timeout								Proximity Timeout							

- Bit 15-8: **Touch and Deep Touch Timeout**
  - 8-bit value * 500ms
- Bit 7-0: **Proximity Timeout**
  - 8-bit value * 500ms

Table A.20: General Button Settings

Register: 0x4004, 0x4104, 0x4204, 0x4304, 0x4404, 0x4504

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Blocking Channel								Reserved				Number of Events		Reserved	Linearise Counts

- Bit 15-8: **Blocking Channel**
  - D'0': Channel 0
  - D'1': Channel 1
  - D'2': Channel 2
  - D'3': Channel 3
  - D'4': Channel 4
  - D'5': Channel 5
  - D'255': None
- Bit 3-2: **Number of Events**
  - 00: None
    - Note exception for *None*:
      - The LTA will permanently halt and remain static without updating / tracking the counts.
      - Reseed or manually overwrite channel LTA as necessary.
  - 01: Proximity events enabled
  - 10: Proximity and touch events enabled
  - 11: Proximity, touch and deep touch events enabled
- Bit 0: **Linearise Counts**

- 0: Linearise Counts Disabled
- 1: Linearise Counts Enabled ($Counts_{linearised}$ = $Target^2$ / Counts)

Table A.21: Beta Filters

Register: 0x4005, 0x4105, 0x4205, 0x4305, 0x4405, 0x4505

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Low Power LTA Beta Filter				Normal Power LTA Beta Filter				Low Power Counts Beta Filter				Normal Power Counts Beta Filter			

- Bit 15-12: **Low Power LTA Beta**
  - 4 bit value
- Bit 11-8: **Normal Power LTA Beta**
  - 4 bit value
- Bit 7-4: **Low Power Counts Beta**
  - 4 bit value
- Bit 3-0: **Normal Power Counts Beta**
  - 4 bit value

Table A.22: Fast Beta Filters

Register: 0x4006, 0x4106, 0x4206, 0x4306, 0x4406, 0x4506

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LTA Fast Beta Filter Bound								Low Power LTA Fast Beta Filter				Normal Power LTA Fast Beta Filter			

- Bit 15-8: **LTA Fast Beta Filter Bound**
  - 8 bit value
- Bit 7-4: **Low Power LTA Fast Beta**
  - 4 bit value
- Bit 3-0: **Normal Power LTA Fast Beta**
  - 4 bit value

Table A.23: Engine Setup Delay

Register: 0x4007

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Prox Engine Setup Delay							

- Bit 7-0: **Prox Engine Setup Delay**
  - 8 bit value

Table A.24: Rx Select and General Channel Settings

Register: 0x5000, 0x5100, 0x5200, 0x5300, 0x5400, 0x5500

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		ATI Band		Global Halt	Invert	Dual	Channel Enable	RX3/7	RX2/6	RX1/5	RX0/4	Cs Size	Vref 0v5	Projected Bias Select	

- Bit 13-12: **ATI Band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Global Halt**
  - 0: Global halt disabled
  - 1: Global halt enabled
- Bit 10: **Invert**
  - 0: Channel output detection occurs when Counts $<$ LTA
  - 1: Channel output detection occurs when Counts $>$ LTA
- Bit 9: **Dual-Directional**
  - 0: Channel output detection occurs in the direction specified by the 'Invert' option
  - 1: Channel output detection occurs when Counts $<$ LTA and when Counts $>$ LTA
- Bit 8: **Channel Enable**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **Rx3/7**

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- 0: Rx3/7 disabled
- 1: Rx3/7 enabled

> Bit 6: **Rx2/6**
- 0: Rx2/6 disabled
- 1: Rx2/6 enabled

> Bit 5: **Rx1/5**
- 0: Rx1/5 disabled
- 1: Rx1/5 enabled

> Bit 4: **Rx0/4**
- 0: Rx0/4 disabled
- 1: Rx0/4 enabled

> Bit 3: **Cs Size**
- 0: 40pF
- 1: 80pF

> Bit 2: **Vref 0v5**
- 0: 0.5V reference voltage disabled
- 1: 0.5V reference voltage enabled

> Bit 1-0: **Projected Bias Select**
- 00: 2μA
- 01: 5μA
- 10: 7μA
- 11: 10μA

Table A.25: ATI Base and Target

Register: 0x5001, 0x5101, 0x5201, 0x5301, 0x5401, 0x5501

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI Target								ATI Base					ATI Mode		

> Bit 15-8: **ATI Target**
- 8-bit value * 8

> Bit 7-3: **ATI Base**
- 5-bit value * 16

> Bit 2-0: **ATI Mode**
- 000: ATI disabled
- 001: Compensation only
- 010: ATI from compensation divider
- 011: ATI from fine fractional divider
- 100: ATI from coarse fractional divider
- 101: Full ATI

Table A.26: ATI Fine and Coarse Fractional Mirrors

Register: 0x5002, 0x5102, 0x5202, 0x5302, 0x5402, 0x5502

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Fractional Divider					Coarse Fractional Multiplier				Coarse Fractional Divider				

> Bit 13-9: **Fine Fractional Divider**
- 5-bit value

> Bit 8-5: **Coarse Fractional Multiplier**
- 4-bit value

> Bit 4-0: **Coarse Fractional Divider**
- 5-bit value

Table A.27: ATI Compensation

Register: 0x5003, 0x5103, 0x5203, 0x5303, 0x5403, 0x5503

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Divider					Res	Compensation Selection									

> Bit 15-11: **Compensation Divider**
- 5-bit value

> Bit 9-0: **Compensation Selection**
- 10-bit value

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Table A.28: Encoder angle resolution

Register: 0x6000

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Number of metal target segments															

- Bit 15-0: **Number of Metal Target Segments**
  - 16-bit value
  - Encoder angular resolution = $\frac{360^{\circ}}{4 \times \text{Number of metal target segments}}$

Table A.29: Encoder coil channel and reference select

Register: 0x6001, 0x6004

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Encoder coil channel/fixed reference								Encoder coil channel select							

- Bit 15-8: **Encoder Coil Channel/Fixed Reference**
  - D'0': Channel 0 reference
  - D'1': Channel 1 reference
  - D'2': Channel 2 reference
  - D'3': Channel 3 reference
  - D'4': Channel 4 reference
  - D'5': Channel 5 reference
  - Fixed reference if value > 5 (value*8)
- Bit 7-0: **Encoder Coil Channel**
  - D'0': Channel 0
  - D'1': Channel 1
  - D'2': Channel 2
  - D'3': Channel 3
  - D'4': Channel 4
  - D'5': Channel 5
  - Fixed reference if value > 5 (value*8)

Table A.30: Encoder coil channel enter threshold

Register: 0x6002, 0x6005

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Enter threshold															

- Bit 15-0: **Enter Threshold**
  - 16-bit signed value

Table A.31: Encoder coil channel exit threshold

Register: 0x6003, 0x6006

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Exit threshold															

- Bit 15-0: **Exit Threshold**
  - 16-bit signed value

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B Inductive Resonant Tank Design Guideline

Described below are the steps to design the inductive resonant tank with a certain resonant frequency.

1. For a given inductance L and T_x frequency (f_{tx}), calculate the capacitor C_{calc} for a resonant frequency $f_{tx} \times 1.05$ ($\pm 5\%$ tolerance on f_{tx}).
2. Select a capacitor C_{sel} such that ($C_{\text{sel}} \times 1.10$) $\leq C_{\text{calc}}$ (assuming a $\pm 10\%$ tolerance on the capacitor).
3. For better safety, 10pF can be removed from parallel tank capacitors less than or equal to 200pF, to account for the T_x and R_x pad capacitance.

Example:

- Given L =1.1uH, use f_{tx} from f_{osc} =18MHz. Determine C_{calc}:

  f_{resonant}= 18MHz + 5% = 18.9MHz

  $$\implies 18.9 \times 10^6 = \frac{1}{2\pi\sqrt{1.1x10^{-6} \times C_{\text{calc}}}}$$

  $$\implies C_{\text{calc}} = 64.46\text{pF}$$

- Next, determine C_{sel} such that $1.1 \times C_{\text{sel}} \leq C_{\text{calc}}$

  $$\implies C_{\text{sel}} \leq 58.6\text{pF}$$

- Subtract 10pF from C_{sel} since $C_{\text{sel}} < 200$pF

  $$\implies C_{\text{sel}} = 48.6\text{pF}$$

- Using $\pm 10\%$ tolerance on C_{sel} and $f_{\text{resonant}} = \frac{1}{2\pi\sqrt{L \times C}} = \frac{1}{2\pi\sqrt{1.1x10^{-6} \times C_{\text{sel}}}}$, we get the results below and the summary of the result shown in Figure B.1.

  $C_{\text{sel}} = 48.6\text{pF} \implies f_{\text{resonant}} = 21.76\text{MHz}$
  $C_{\text{sel}} = 48.6\text{pF} + 10\% \implies f_{\text{resonant}} = 20.75\text{MHz}$
  $C_{\text{sel}} = 48.6\text{pF} - 10\% \implies f_{\text{resonant}} = 22.9\text{MHz}$

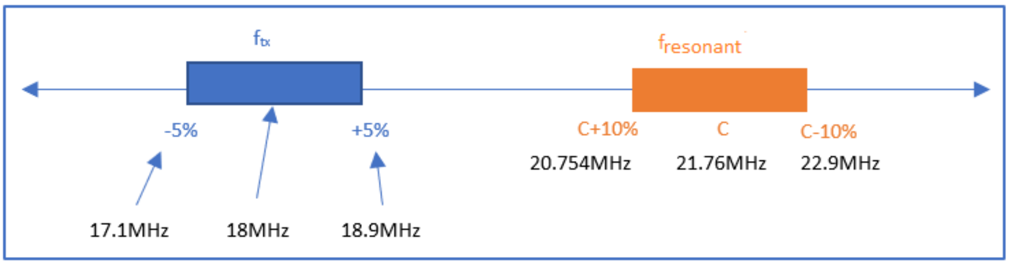

Figure B.1: Inductive Resonant Tank Design

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C Revision History

Release	Date	Changes
v 1.1	Dec/2021	Initial release
v 1.3	Jan/2022	Minor updates and corrections
v 1.4	Jul/2022	Minor updates and corrections
v 1.5	Dec/2022	Memory map update for device FW version 2.1
v 1.6	Feb/2023	Minor updates and corrections
v 1.7	Mar/2023	Minor updates and corrections
v 1.8	July/2023	Minor updates and corrections

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Contact Information

	USA	Asia	South Africa
Physical Address	11940 Jollyville Suite 120-S Austin TX 78759 USA	Room 501A, Block A T-Share International Centre Taoyuan Road, Nanshan District Shenzhen, Guangdong, PRC	1 Bergsig Avenue Paarl 7646 South Africa
Postal Address	11940 Jollyville Suite 120-S Austin TX 78759 USA	Room 501A, Block A T-Share International Centre Taoyuan Road, Nanshan District Shenzhen, Guangdong, PRC	PO Box 3534 Paarl 7620 South Africa
Tel	+1 512 538 1995	+86 755 8303 5294 ext 808	+27 21 863 0033
Email	info@azoteq.com	info@azoteq.com	info@azoteq.com

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